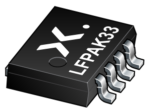


BUK6M61-60P

60 V, P-channel Trench MOSFET

2 September 2024 — Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an LFPAK33 package using Trench MOSFET technology.

This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Reverse polarity protection
- Power management
- High-side load switch
- Motor drive

4. Quick reference data

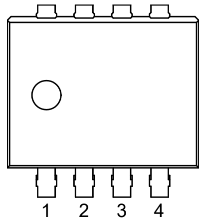
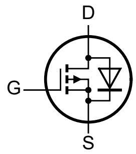
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-60	V
V_{GS}	gate-source voltage		[1]	-20	-	20	V
I_D	drain current	V_{GS} = -10 V; T_{mb} = 25 °C		-	-	-27	A
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	-	99	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -7 A; T_j = 25 °C		-	48	61	mΩ

[1] V_{GS} = -20 V/+5 V according AEC-Q101 at T_j = 175 °C; V_{GS} = -20 V/+16 V according AEC-Q101 at T_j = 150 °C

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	 017aaa094
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6M61-60P	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6M61-60P	66160P

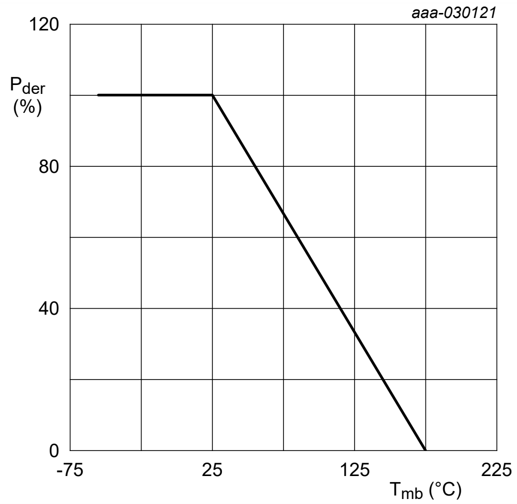
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

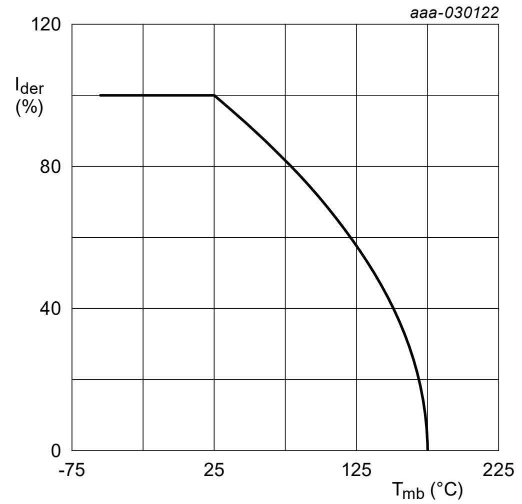
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-60	V
V_{GS}	gate-source voltage		[1]	-20	20	V
I_D	drain current	V_{GS} = -10 V; T_{mb} = 25 °C		-	-27	A
		V_{GS} = -10 V; T_{mb} = 100 °C		-	-17	A
I_{DM}	peak drain current	T_{mb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-108	A
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	99	W
T_j	junction temperature			-55	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	-27	A
I_{SM}	peak source current	T_{mb} = 25 °C, single pulse; t_p ≤ 10 µs		-	-108	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	800	V
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{sup} ≤ -60 V; V_{GS} = -10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; I_D = -19.5 A; unclamped	[3]	-	36	mJ
		V_{sup} ≤ -60 V; V_{GS} = -10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; I_D = -4.6 A; unclamped	[3]	-	142	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(init)}$ = 25 °C	[3]	-	-19.5	A

[1] V_{GS} = -20 V/+5 V according AEC-Q101 at T_j = 175 °C; V_{GS} = -20 V/+16 V according AEC-Q101 at T_j = 150 °C
[2] Measured between all pins.
[3] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig. 2. Normalized continuous drain current as a function of mounting base temperature

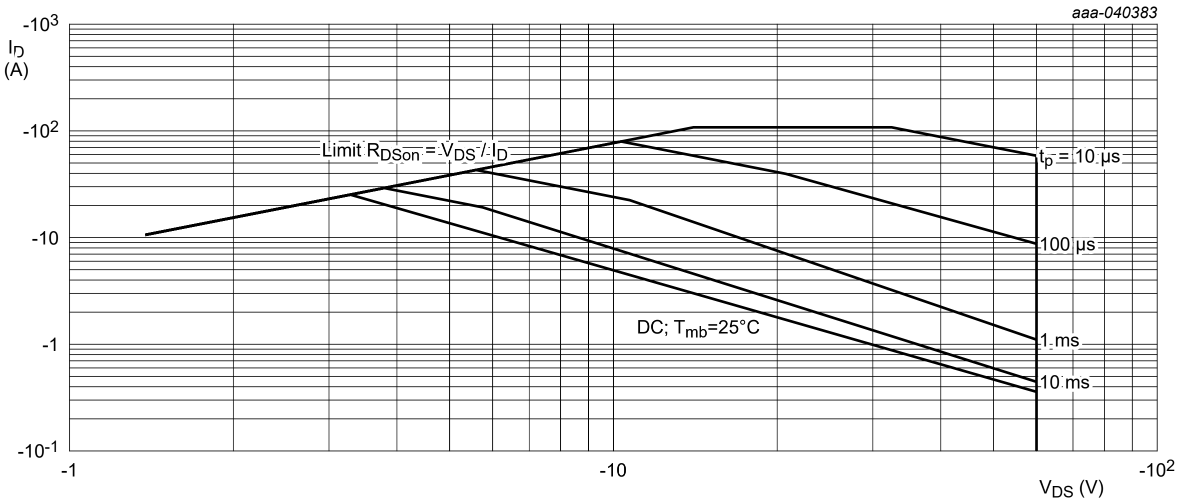


Fig. 3. Safe operating area; junction to mounting base; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	1.38	1.52	K/W

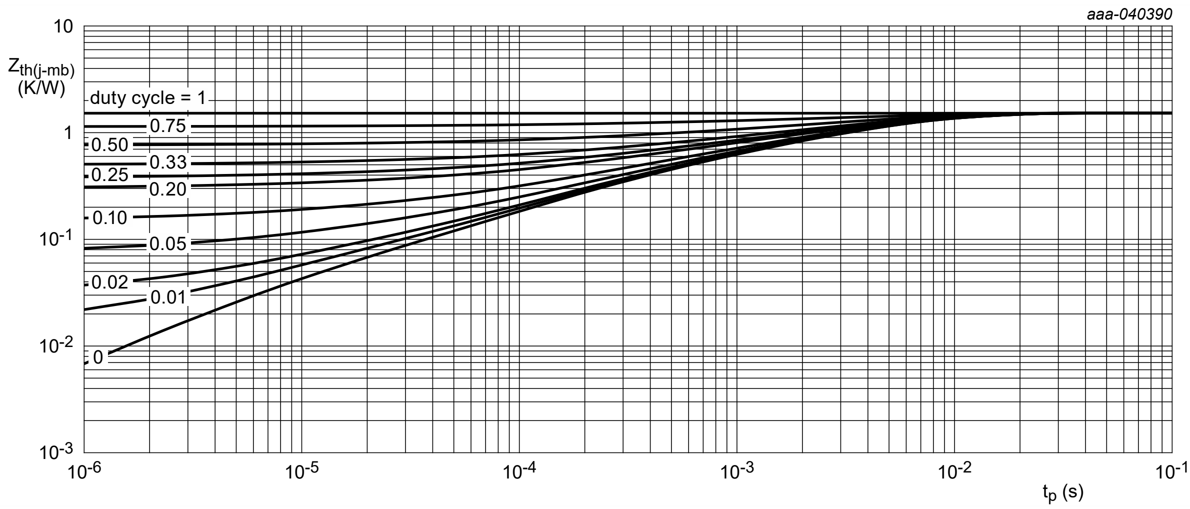
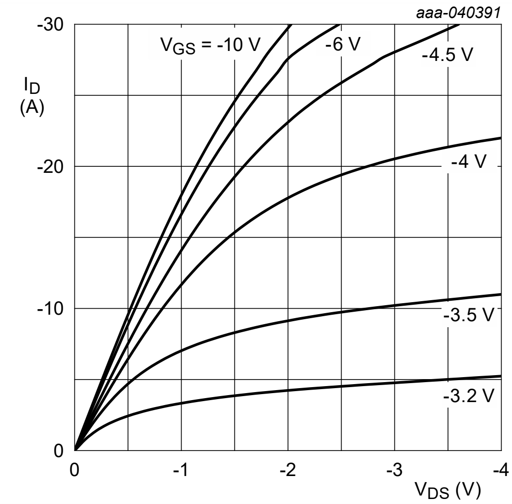


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

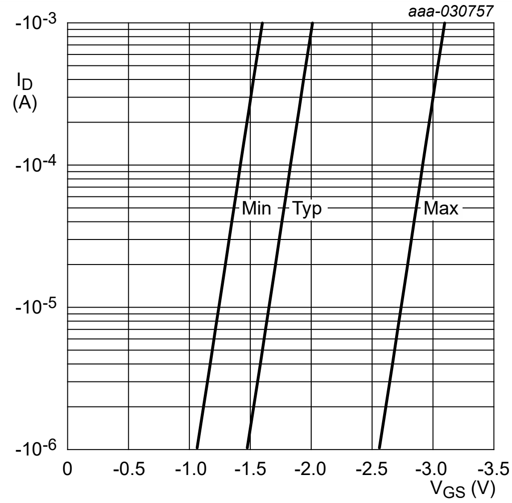
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C		-60	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C		-1.5	-2	-3	V
I_{DSS}	drain leakage current	V_{DS} = -60 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-1	µA
		V_{DS} = -60 V; V_{GS} = 0 V; T_j = 125 °C		-	-	-10	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -7 A; T_j = 25 °C		-	48	61	mΩ
		V_{GS} = -10 V; I_D = -7 A; T_j = 175 °C		-	100	130	mΩ
		V_{GS} = -4.5 V; I_D = -6 A; T_j = 25 °C		-	62	93	mΩ
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -4 A; T_j = 25 °C		-	65	-	S
R_G	gate resistance	f = 1 MHz		-	12	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -30 V; I_D = -7 A; V_{GS} = -10 V; T_j = 25 °C		-	19	29	nC
Q_{GS}	gate-source charge			-	3.6	-	nC
Q_{GD}	gate-drain charge			-	4.3	-	nC
C_{iss}	input capacitance	V_{DS} = -30 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	1060	-	pF
C_{oss}	output capacitance			-	85	-	pF
C_{rss}	reverse transfer capacitance			-	49	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -30 V; I_D = -7 A; V_{GS} = -10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	3	-	ns
t_r	rise time			-	6	-	ns
$t_{d(off)}$	turn-off delay time			-	35	-	ns
t_f	fall time			-	144	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = -5 A; V_{GS} = 0 V; T_j = 25 °C		-	-0.8	-1.2	V
t_{rr}	reverse recovery time	I_S = -5 A; dI_S/dt = 100 A/µs; V_{GS} = -10 V; V_{DS} = -30 V; T_j = 25 °C		-	27	-	ns
Q_r	recovered charge			-	29	-	nC



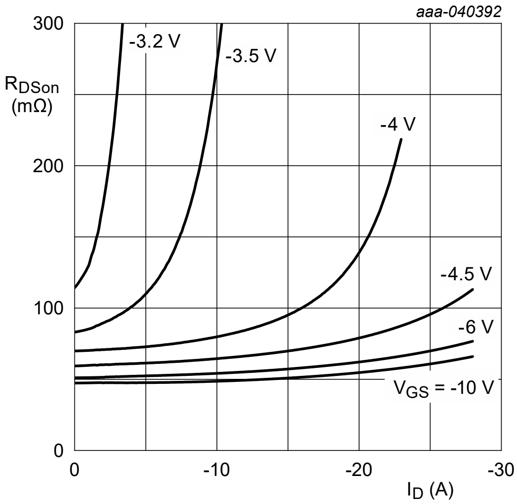
T_j = 25 °C

Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values



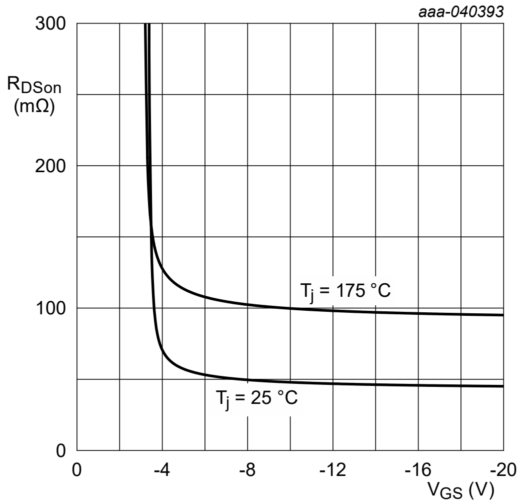
V_{DS} = -5 V; T_j = 25 °C

Fig. 6. Sub-threshold drain current as a function of gate-source voltage



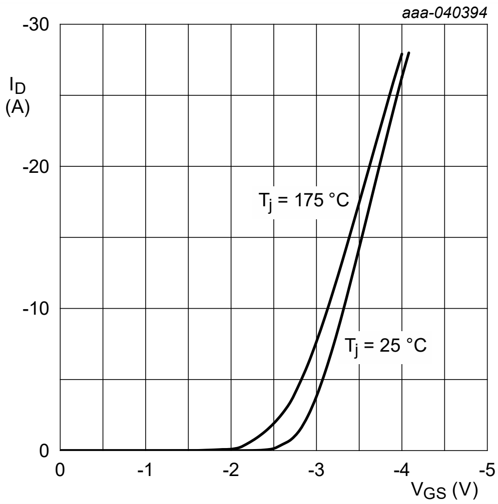
T_j = 25 °C

Fig. 7. Drain-source on-state resistance as a function of drain current; typical values



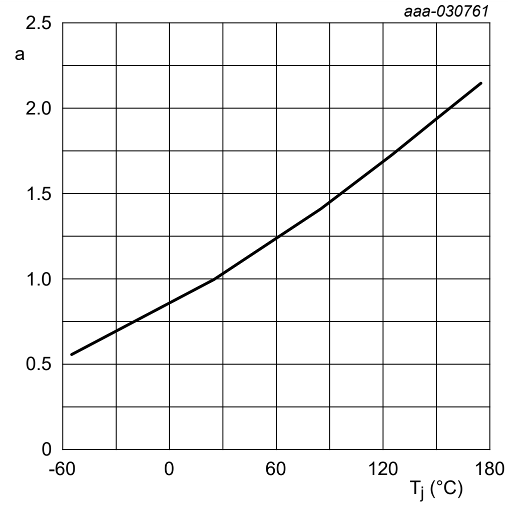
I_D = -7 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



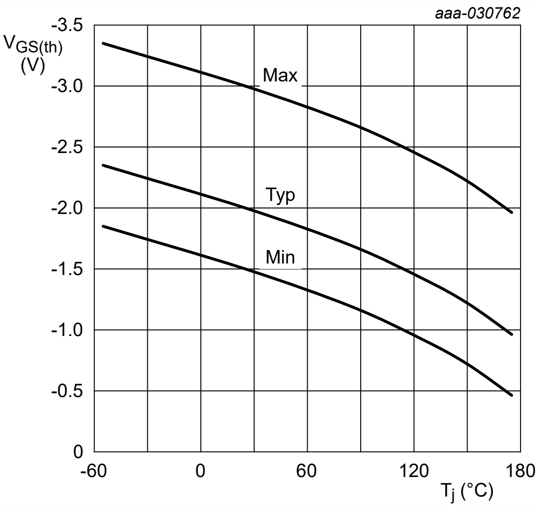
V_{DS} = -10 V

Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



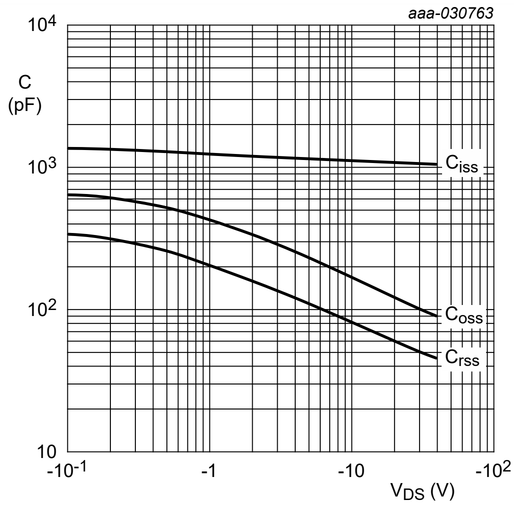
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values



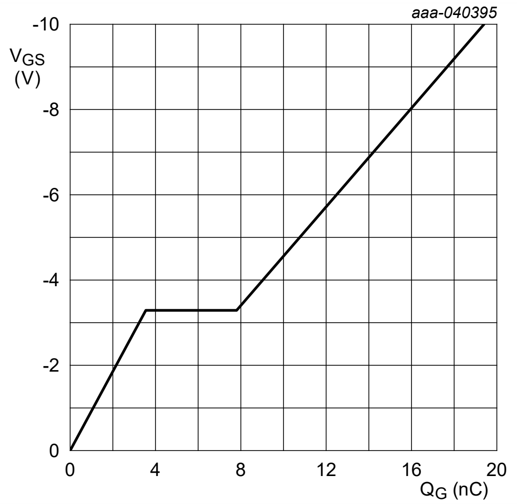
I_D = -250 µA; V_{DS} = V_{GS}

Fig. 11. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{DS} = -30 V; I_D = -7 A; T_j = 25 °C

Fig. 13. Gate-source voltage as a function of gate charge; typical values

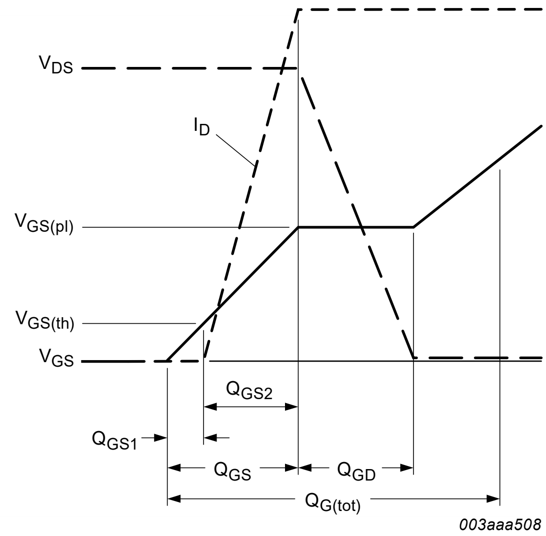
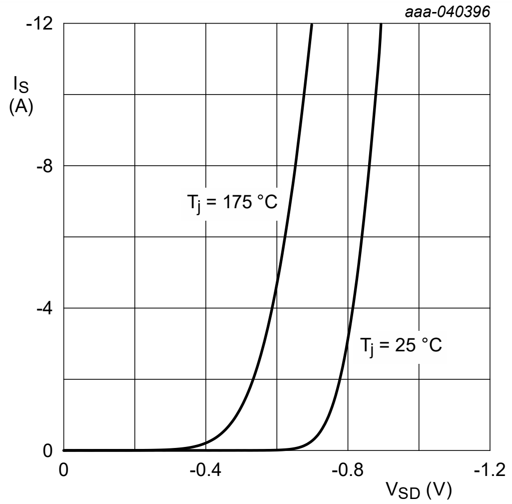


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 15. Source current as a function of source-drain voltage; typical values

11. Test information

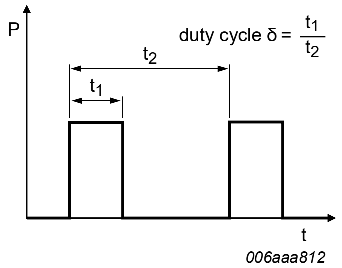


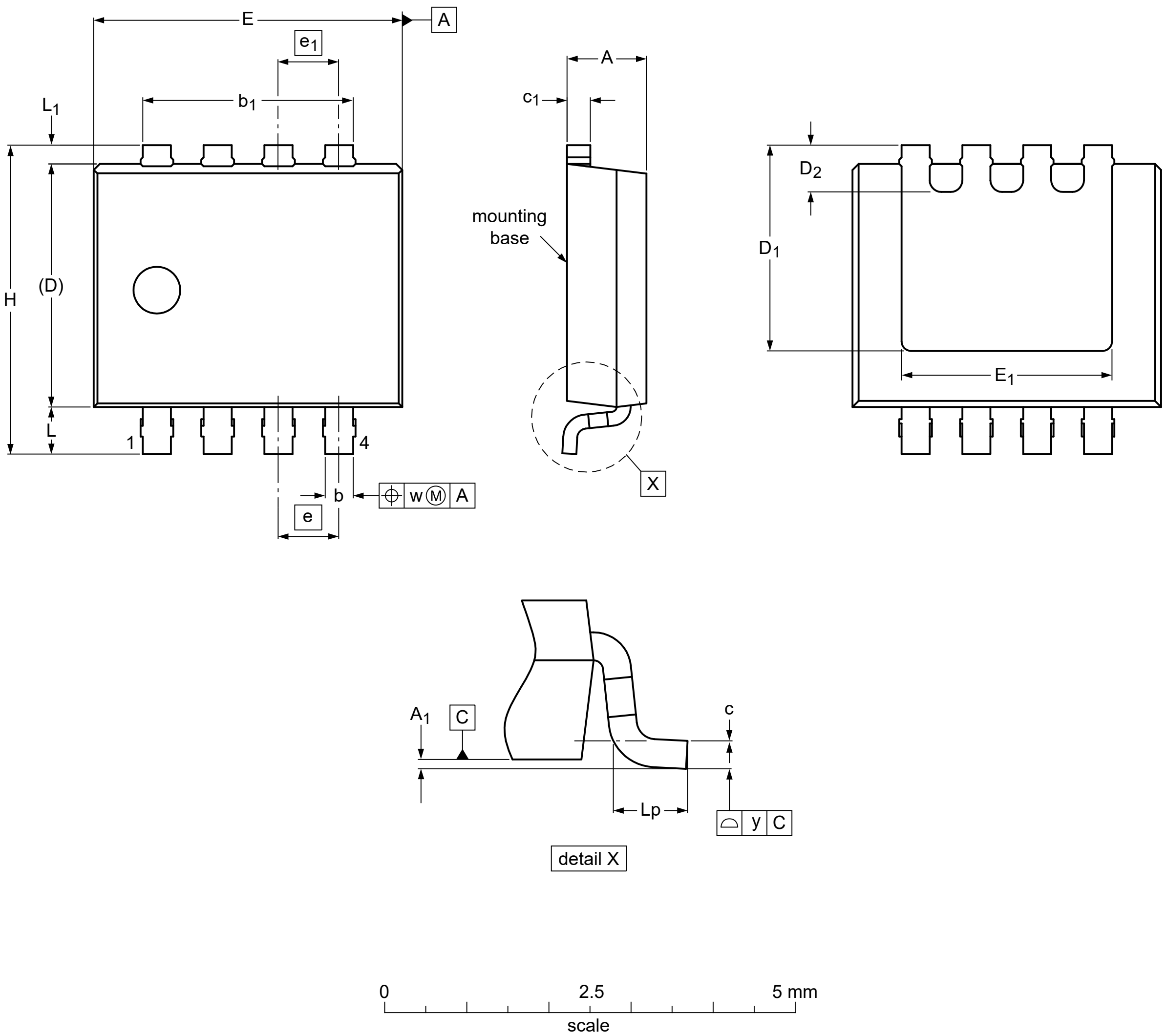
Fig. 16. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit(1)		A	A_1	b(1)	b_1(1)	c	c_1	D ref	D_1	D_2	E(1)	E_1	e	e_1	H	L	L_1	L_p	w	y
mm	max	0.90	0.10	0.35	2.4	0.20	0.30		2.35		3.40	2.45			3.40	0.65	0.25	0.50		
	nom							2.60		0.50			0.65	0.65					0.20	0.10
	min	0.80	0.00	0.25	2.2	0.10	0.20		1.90		3.20	2.00			3.20	0.45	0.13	0.30		

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~14-04-25~~ 16-08-09

Fig. 17. Package outline LFPAK33 (SOT1210)

13. Soldering

Footprint information for reflow soldering of LFPAK33 package **SOT1210**

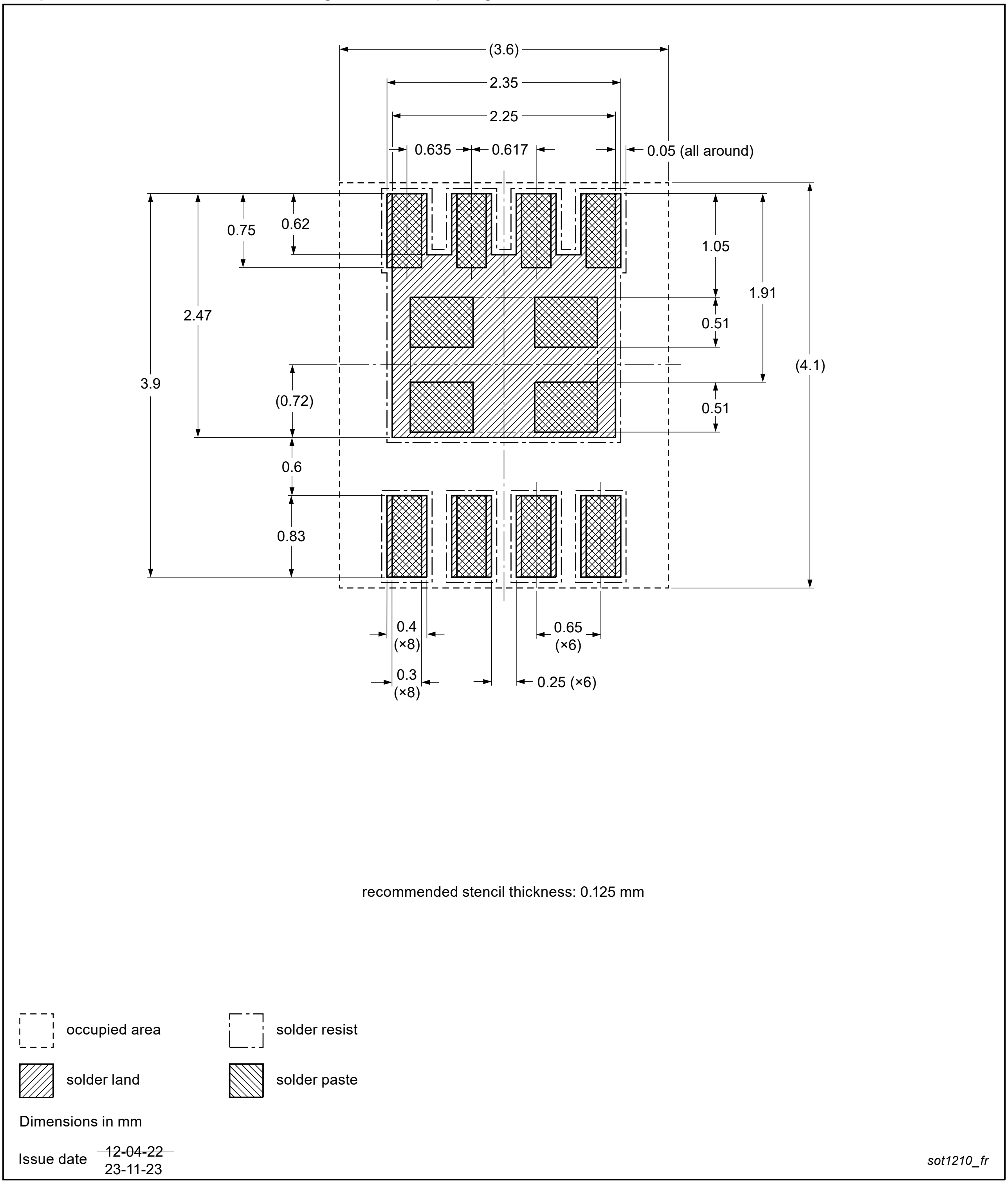


Fig. 18. Reflow soldering footprint for LFPAK33 (SOT1210)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6M61-60P v.1	20240902	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 2 September 2024