

BUK71/7905-40AIE

TrenchPLUS standard level FET

Rev. 04 — 6 February 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance, TrenchPLUS current sensing and diodes for ESD protection.

1.2 Features

- ESD protection
- Q101 compliant
- Integrated current sensor
- Standard level compatible.

1.3 Applications

- Variable Valve Timing for engines
- Electrical Power Assisted Steering.

1.4 Quick reference data

- $V_{DS} \leq 40$ V
- $R_{DSon} = 4.5$ m Ω (typ)
- $I_D \leq 155$ A
- $I_D/I_{sense} = 500$ (typ).

2. Pinning information

Table 1: Pinning - SOT426 and SOT263B, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	I_{sense} (I_s)		
3	drain (d)		
4	Kelvin source		
5	source (s)		
mb	mounting base; connected to drain (d)	<p style="text-align: center;">SOT426 (D²-PAK) SOT263B (TO-220)</p>	



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
BUK7105-40AIE	D ² -PAK	Plastic single-ended surface mounted package (Philips version of D ² -PAK); 5 leads (one lead cropped)	SOT426
BUK7905-40AIE	TO-220	Plastic single ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220	SOT263B

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage (DC)		-	40	V
V _{DGR}	drain-gate voltage (DC)	R _{GS} = 20 kΩ	-	40	V
V _{GS}	gate-source voltage (DC)		-	±20	V
I _D	drain current (DC)	T _{mb} = 25 °C; V _{GS} = 10 V; Figure 2 and 3	[1] -	155	A
		T _{mb} = 100 °C; V _{GS} = 10 V; Figure 2	[2] -	75	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Figure 3	-	620	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Figure 1	-	272	W
I _{GS(CL)}	gate-source clamping current	continuous	-	10	mA
		t _p = 5 ms; δ = 0.01	-	50	mA
T _{stg}	storage temperature		-55	+175	°C
T _j	junction temperature		-55	+175	°C

Source-drain diode

I _{DR}	reverse drain current (DC)	T _{mb} = 25 °C	[1] -	155	A
			[2] -	75	A
I _{DRM}	peak reverse drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs	-	620	A

Avalanche ruggedness

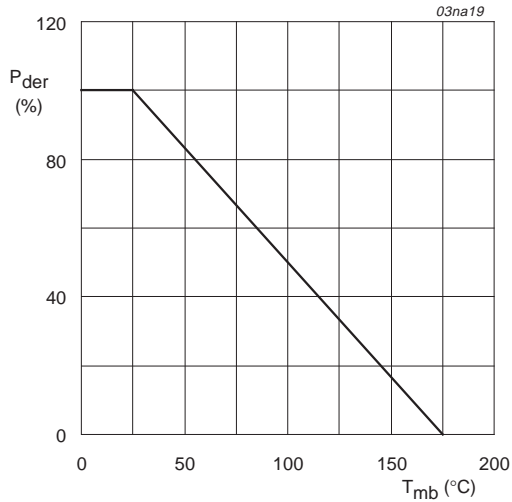
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	unclamped inductive load; I _D = 75 A; V _{DS} ≤ 40 V; V _{GS} = 10 V; R _{GS} = 50 Ω; starting T _j = 25 °C	-	1.46	J
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Electrostatic discharge

V _{esd}	electrostatic discharge voltage; all pins	Human Body Model; C = 100 pF; R = 1.5 kΩ	-	6	kV
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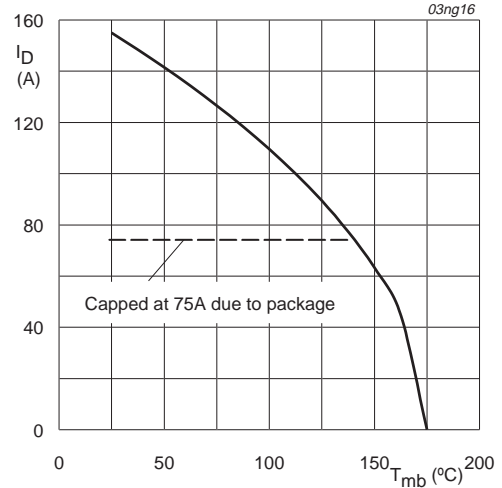
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



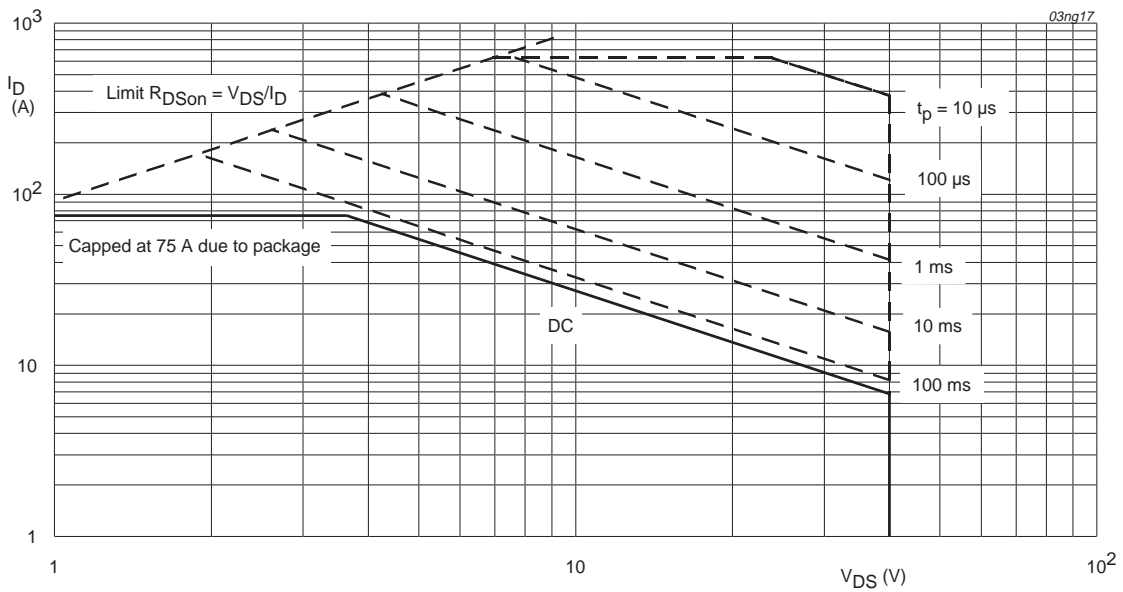
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10\text{ V}$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^\circ C$; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air				
	SOT263B		-	60	-	K/W
	SOT426	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.55	K/W

5.1 Transient thermal impedance

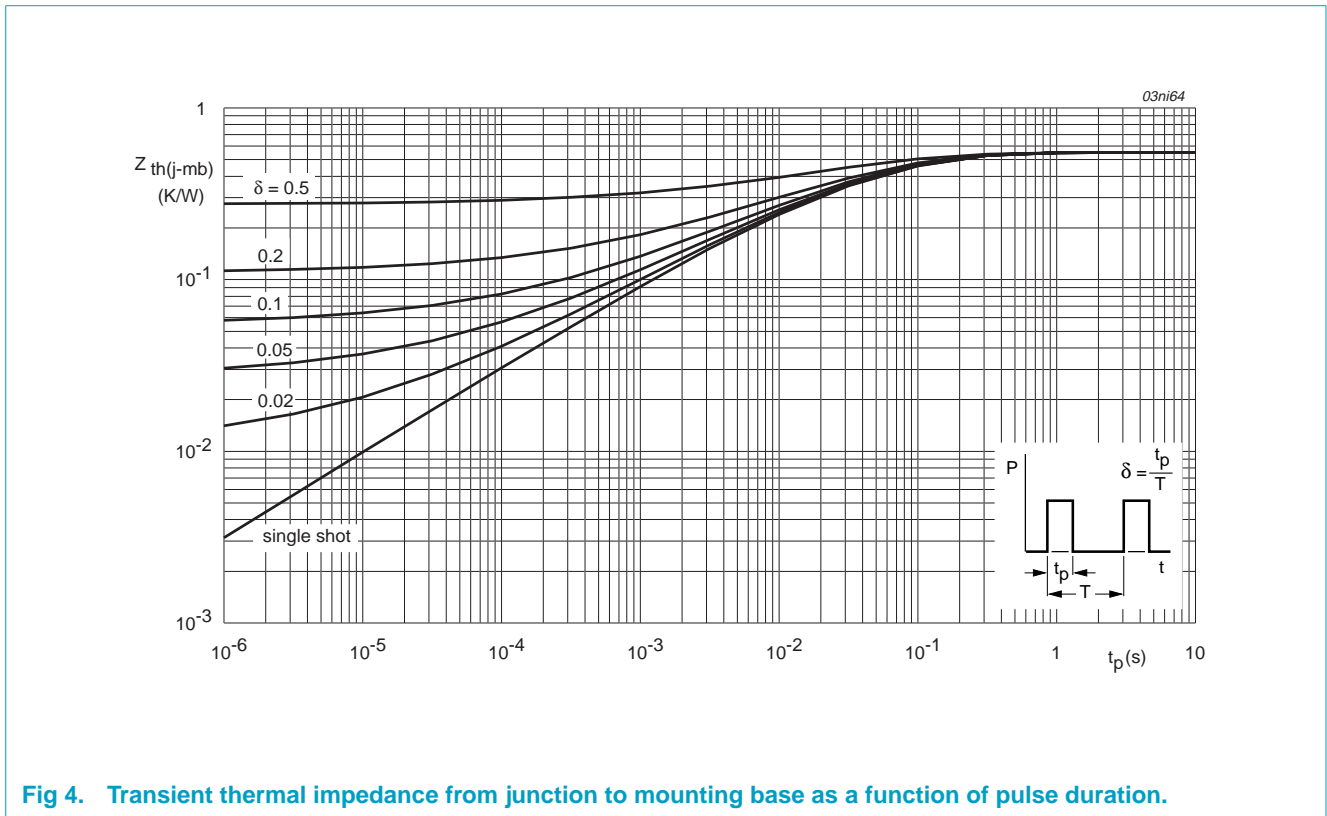


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

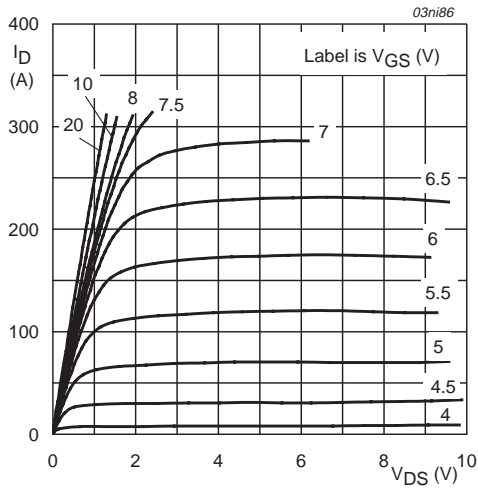
Table 5: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	40	-	-	V
		$T_j = -55\text{ °C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 40\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.1	10	μA
		$T_j = 175\text{ °C}$	-	-	250	μA
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$ $-55\text{ °C} < T_j < 175\text{ °C}$	20	22	-	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	22	1000	nA
		$T_j = 175\text{ °C}$	-	-	10	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 50\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	4.5	5	m Ω
		$T_j = 175\text{ °C}$	-	-	9.5	m Ω
$R_{D(Is)on}$	drain- I_{sense} on-state resistance	$V_{GS} = 10\text{ V}; I_D = 100\text{ mA};$ Figure 16				
		$T_j = 25\text{ °C}$	0.98	1.08	1.18	Ω
		$T_j = 175\text{ °C}$	1.86	2.05	2.24	Ω
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} > 10\text{ V};$ $-55\text{ °C} < T_j < 175\text{ °C}$	450	500	550	
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; V_{DS} = 32\text{ V};$	-	120	127	nC
Q_{gs}	gate-source charge	$I_D = 25\text{ A};$ Figure 14	-	19	22	nC
Q_{gd}	gate-drain (Miller) charge		-	50	60	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$	-	4300	5000	pF
C_{oss}	output capacitance	$f = 1\text{ MHz};$ Figure 12	-	1400	1670	pF
C_{rss}	reverse transfer capacitance		-	820	1100	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$	-	35	-	nS
t_r	rise time	$V_{GS} = 10\text{ V}; R_G = 10\text{ }\Omega$	-	115	-	nS
$t_{d(off)}$	turn-off delay time		-	155	-	nS
t_f	fall time		-	110	-	nS

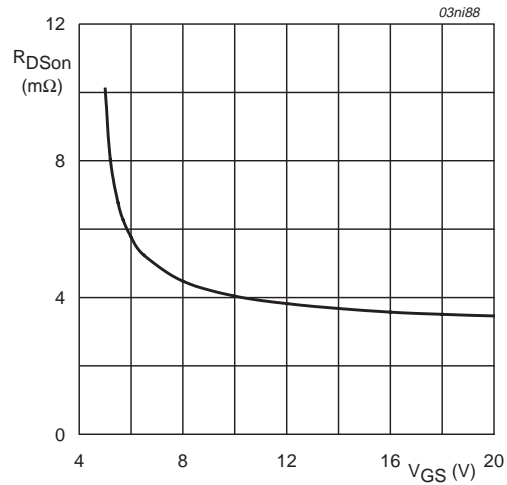
Table 5: Characteristics...continued*T_j = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L _d	internal drain inductance	measured from upper edge of drain mounting base to center of die	-	2.5	-	nH
L _s	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 40 A; V _{GS} = 0 V; Figure 17	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs	-	96	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V	-	224	-	nC



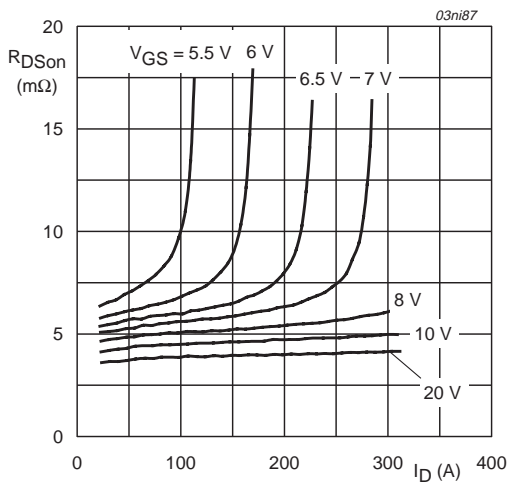
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



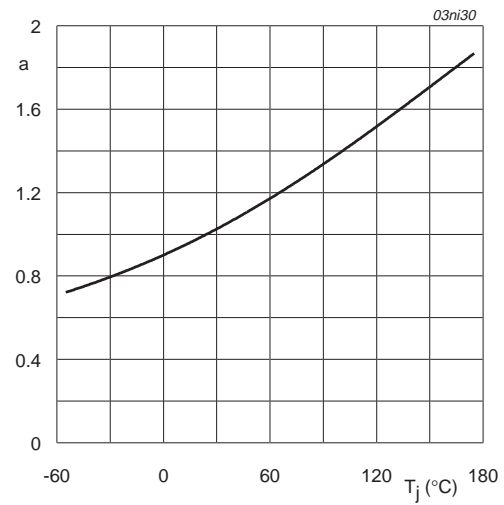
$T_j = 25\text{ }^\circ\text{C}; I_D = 50\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



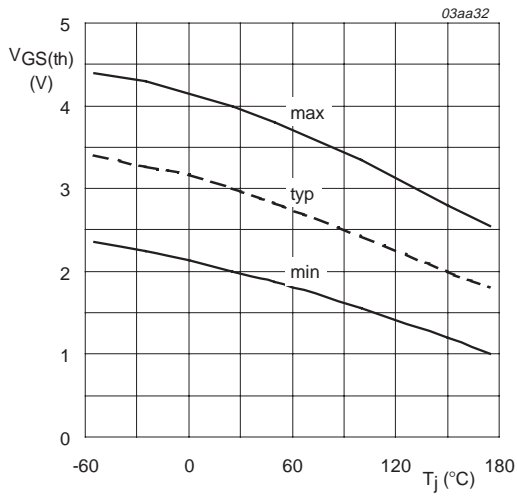
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



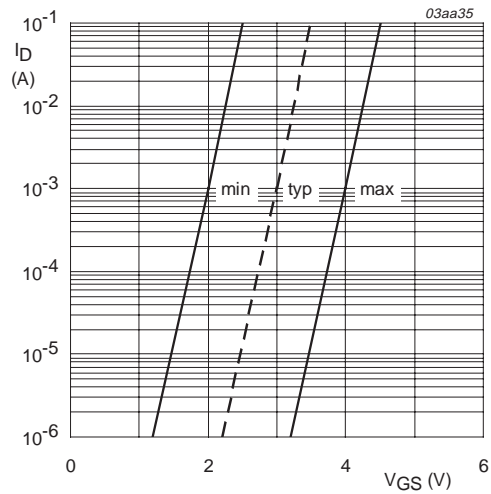
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



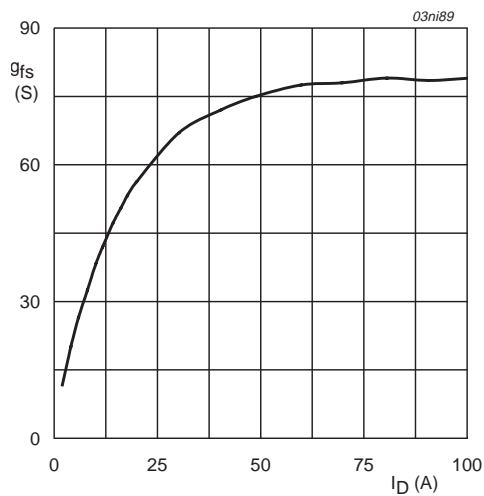
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



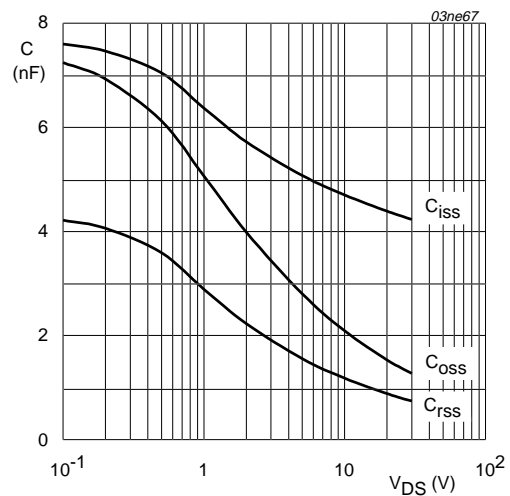
$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



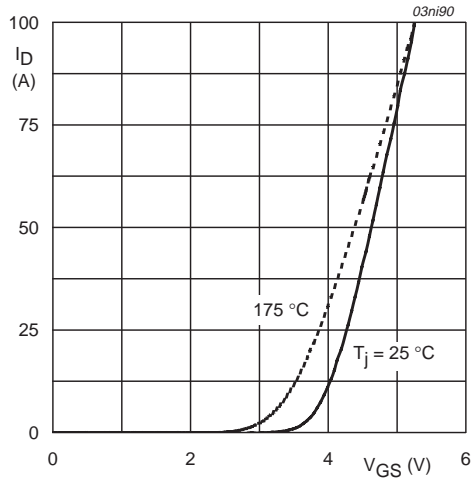
$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



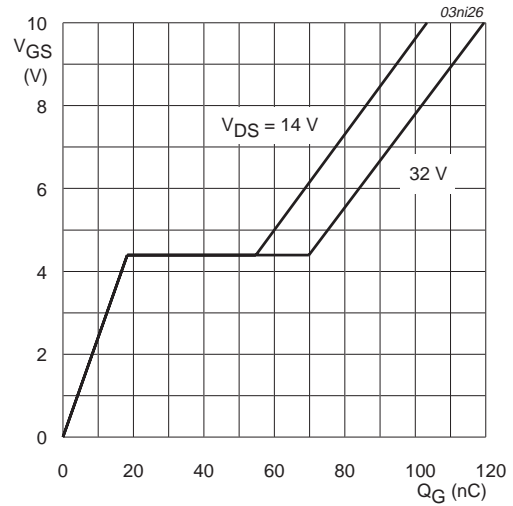
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



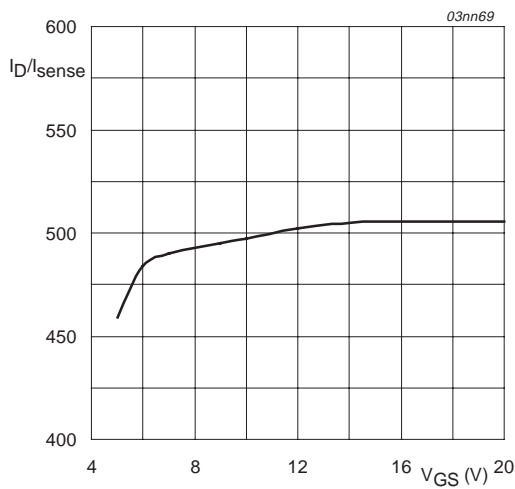
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



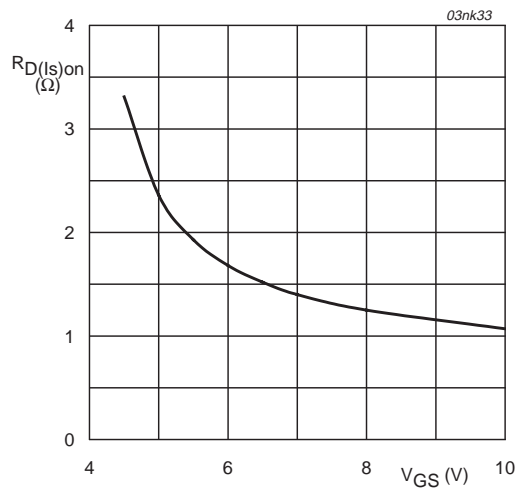
$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



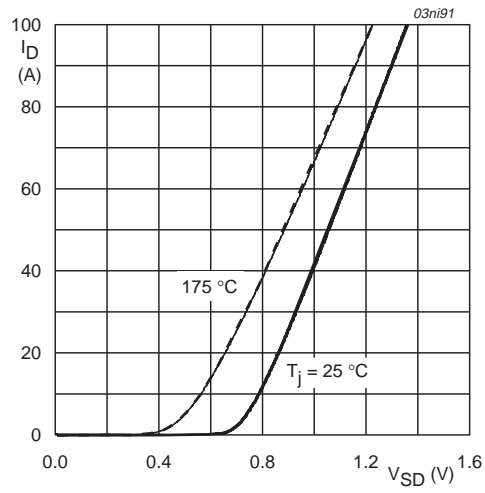
$I_D = 50\text{ A}$

Fig 15. Drain-sense current ratio as a function of gate-source voltage; typical values.



$I_{sense} = 25\text{ mA}$

Fig 16. Drain- I_{sense} on-state resistance as a function of gate-source voltage; typical values.



$V_{GS} = 0\text{ V}$

Fig 17. Drain current as a function of source-drain diode voltage; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK); 5 leads (one lead cropped)

SOT426

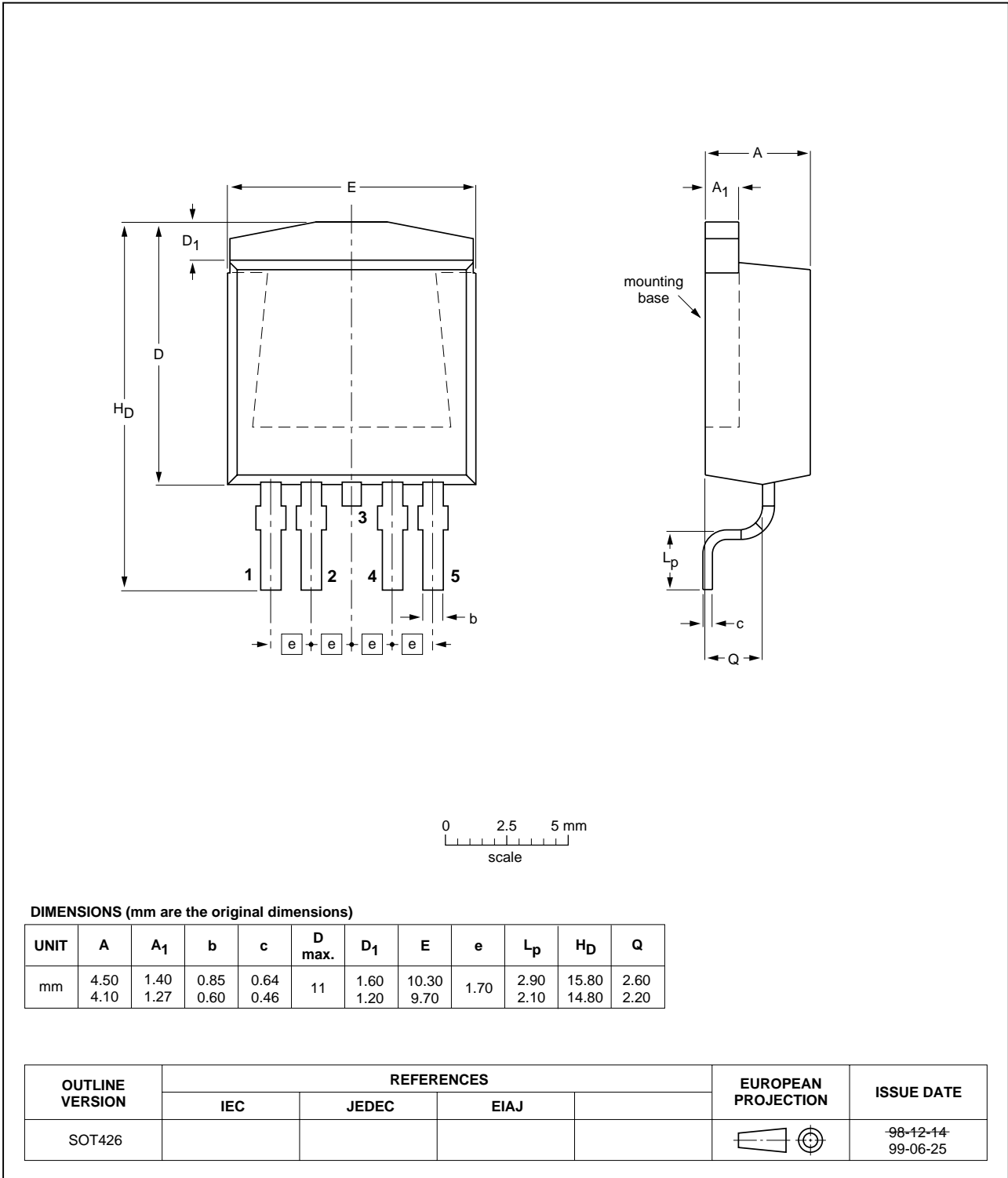


Fig 18. SOT426 (D²-PAK).

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220

SOT263B

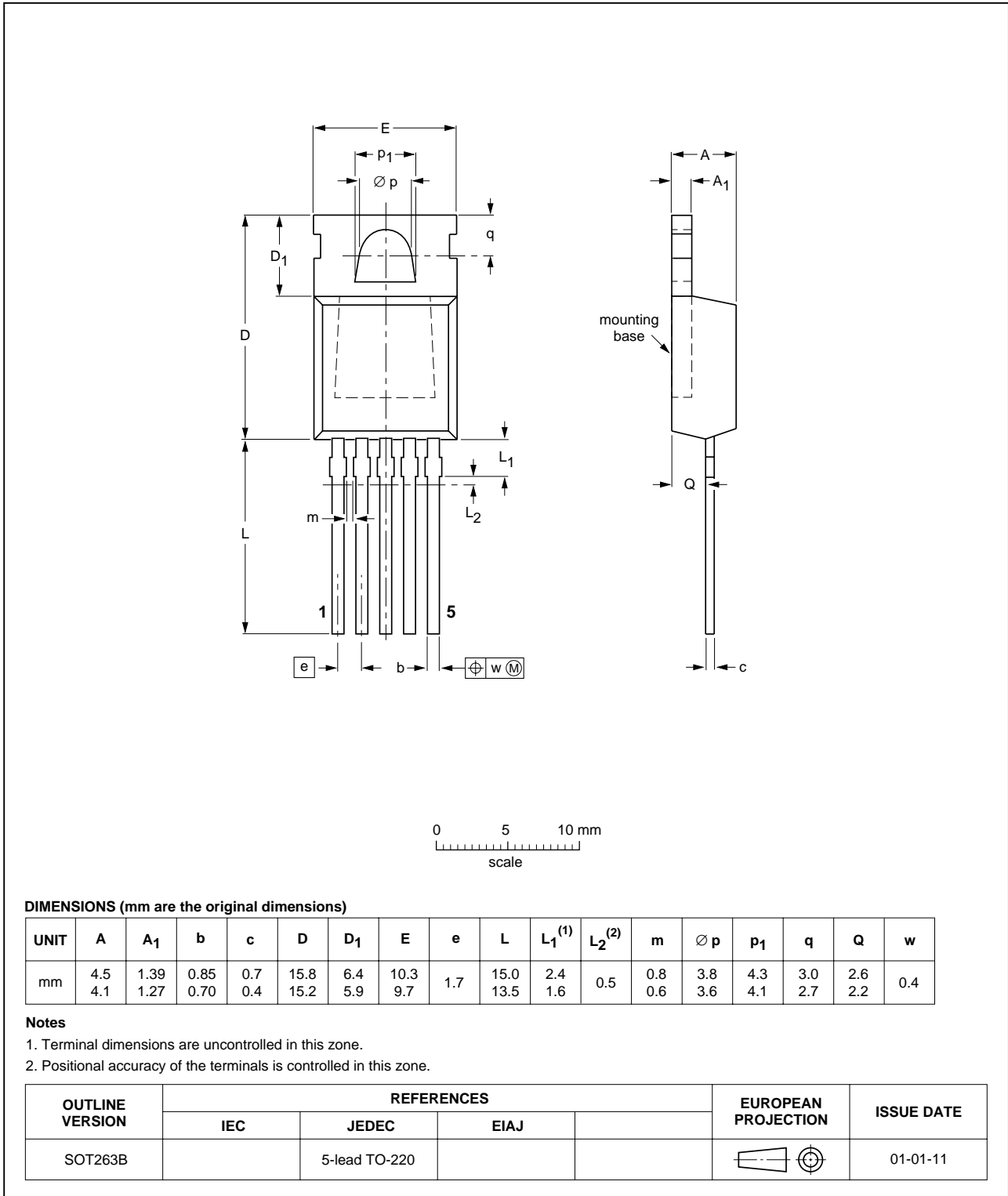
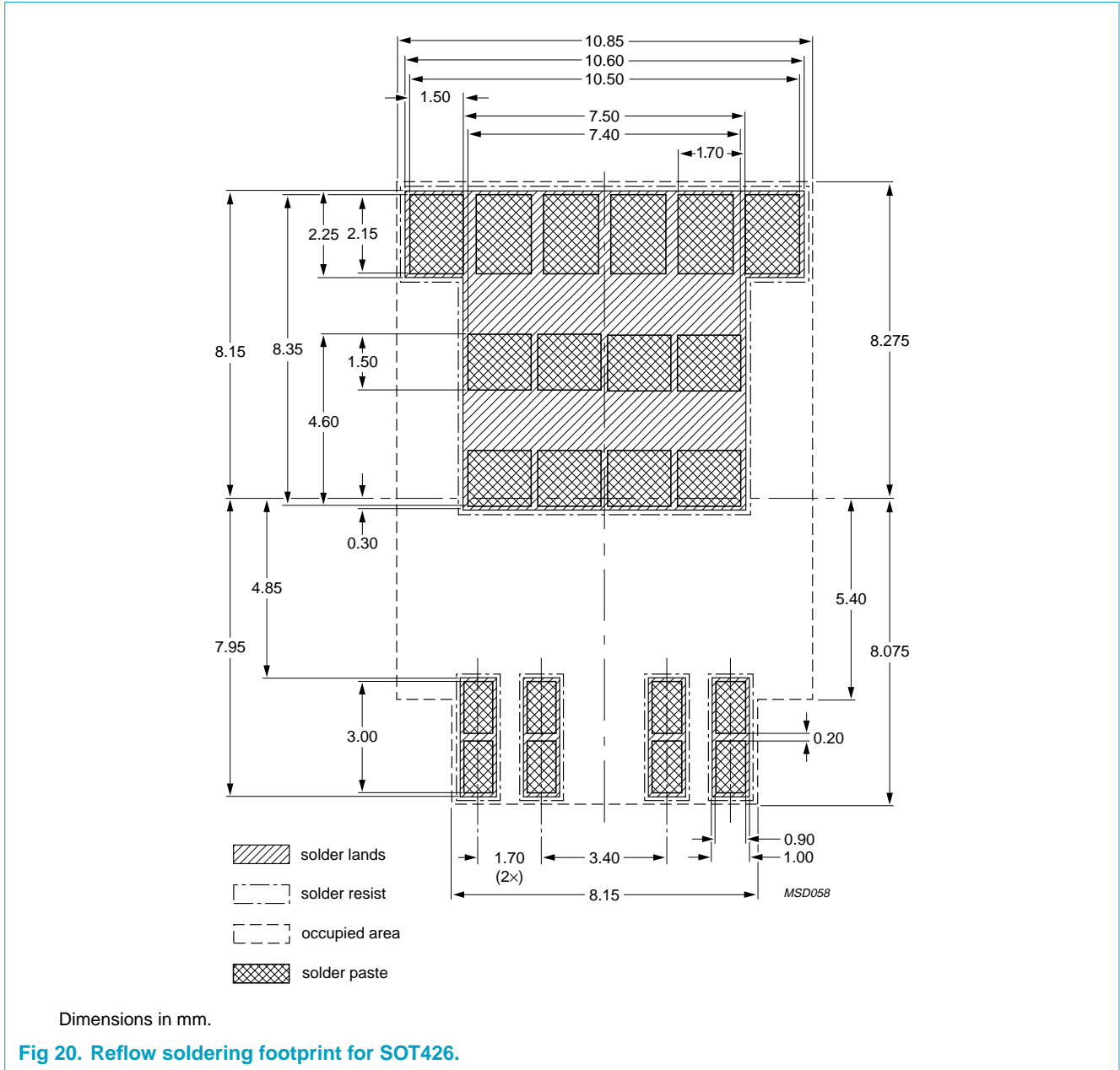


Fig 19. SOT263B (TO-220).

8. Soldering



9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
04	20040206	-	Product data (9397 750 12341) Modifications: <ul style="list-style-type: none">• $Q_{g(\text{tot})}$, Q_{gs}, Q_{gd} values changed in Table 5• C_{iss}, C_{oss}, C_{rss} values changed in Table 5• Section 3 "Ordering information" added
03	20030523	-	Product data (9397 750 11366)
02	20021001	-	Product data (9397 750 10284)
01	20020725	-	Product data (9397 750 09871)

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

11. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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