

# BUK725R0-40C

N-channel TrenchMOS standard level FET

Rev. 01 — 23 March 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high performance automotive applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Avalanche robust
- Suitable for standard level gate drive
- Suitable for thermally demanding environment up to 175°C rating

### 1.3 Applications

- 12V Motor, lamp and solenoid loads
- High performance automotive power systems
- High performance Pulse Width Modulation (PWM) applications

### 1.4 Quick reference data

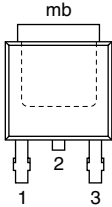
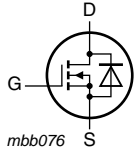
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ;	[1]	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	157	W
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	-	240	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 15</a>	-	27	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	4.1	5	m $\Omega$

[1] Current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;"><b>SOT428</b> (SC-63; DPAK)</p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK725R0-40C	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	40	V	
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ;	[1]	-	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>	[1]	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s};$ pulsed; see <a href="#">Figure 3</a>	-	490	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	157	W	
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C};$	[2]	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C}$	-	490	A	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}; V_{sup} \leq 40\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V};$ $T_{j(init)} = 25\text{ °C};$ unclamped	-	240	mJ	
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see <a href="#">Figure 4</a>	[3][4] [5]	-	J	

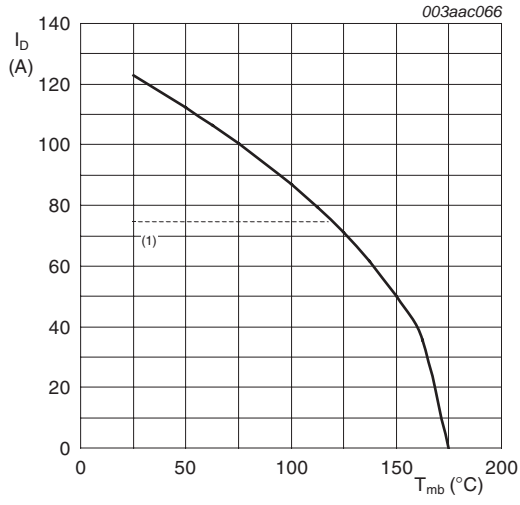
[1] Current is limited by package.

[2] Continuous current is limited by package.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

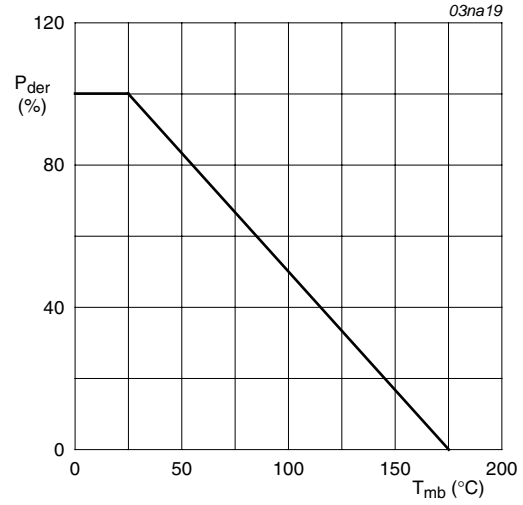
[4] Repetitive avalanche rating limited by average junction temperature of 170 °C.

[5] Refer to application note AN10273 for further information.



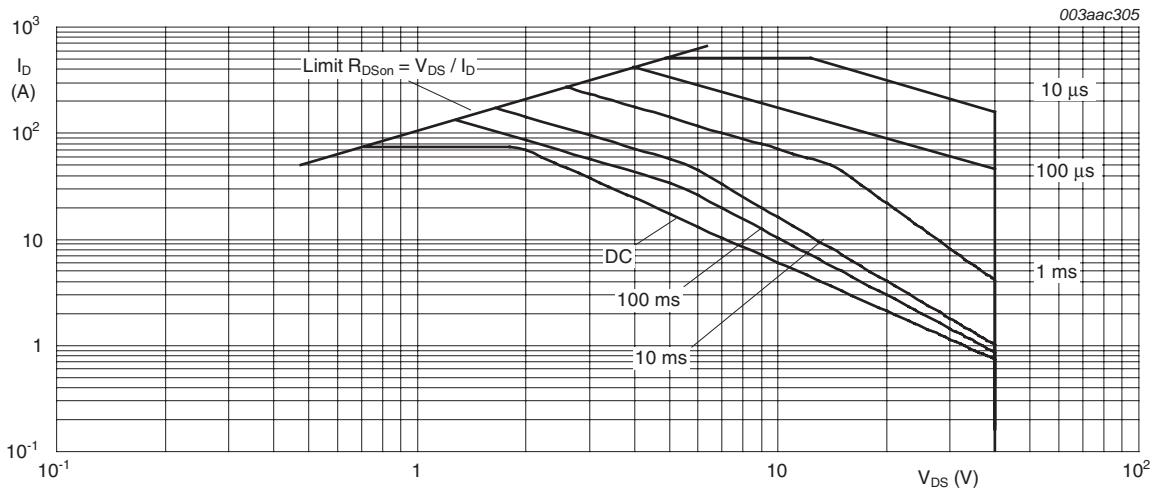
$V_{GS} \geq 10V$   
 (1) Capped at 75 A due to package.

**Fig 1. Continuous drain current as a function of mounting base temperature**



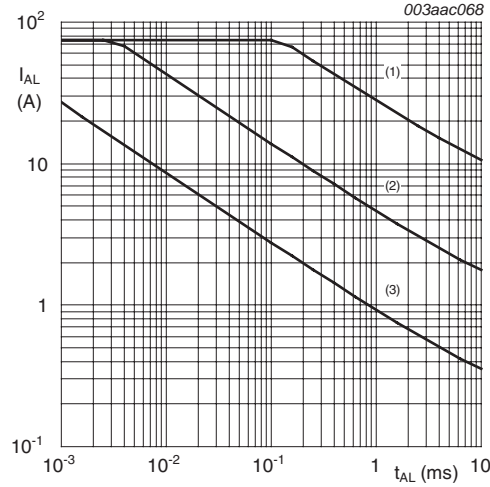
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



$T_{mb} = 25^\circ C; I_{DM}$  is single pulse  
 Capped at 75 A due to package.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



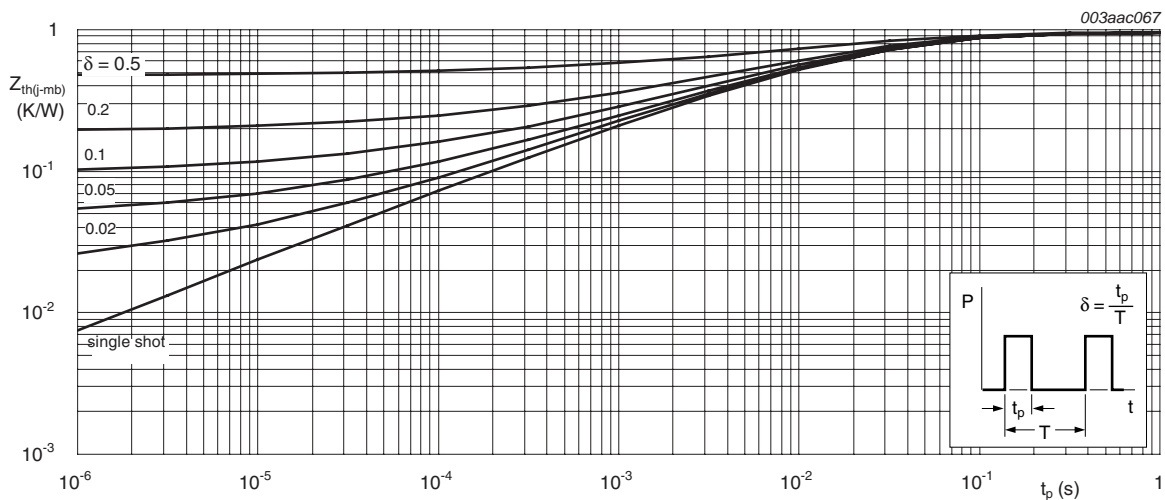
- (1) Single-pulse;  $T_j = 25\text{ }^\circ\text{C}$ .
- (2) Single-pulse;  $T_j = 150\text{ }^\circ\text{C}$ .
- (3) Repetitive.

**Fig 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	0.65	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; mounted on a printed circuit board; minimum foot-print	-	70	-	K/W

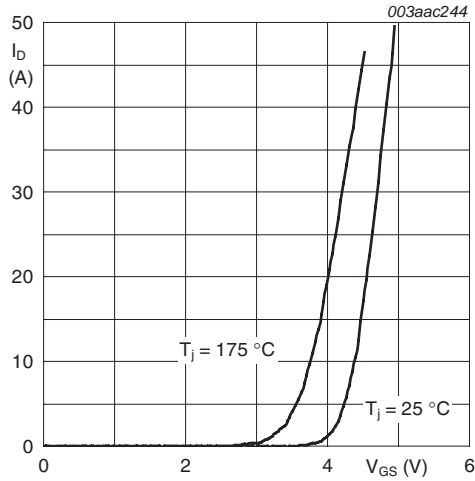


**Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

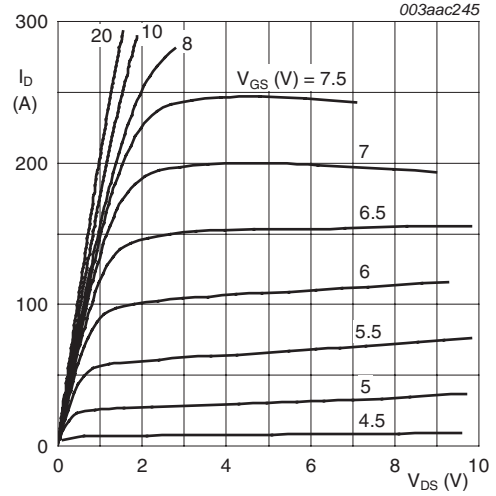
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	40	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	-	4.4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	9.5	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	4.1	5	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-	60	-	nC
$Q_{GS}$	gate-source charge		-	12	-	nC
$Q_{GD}$	gate-drain charge		-	27	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	2870	3820	pF
$C_{oss}$	output capacitance		-	540	650	pF
$C_{rss}$	reverse transfer capacitance		-	350	490	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ }^\Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 10 \text{ }^\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	27	-	ns
$t_r$	rise time		-	73	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
$t_f$	fall time		-	63	-	ns
$L_D$	internal drain inductance	measured from drain to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
$L_S$	internal source inductance	measured from source lead to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V};$ $V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	50	-	ns
$Q_r$	recovered charge		-	25	-	nC



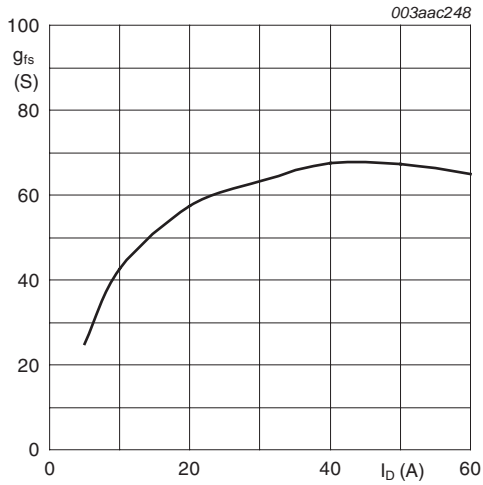
$V_{DS} = 25\text{ V}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



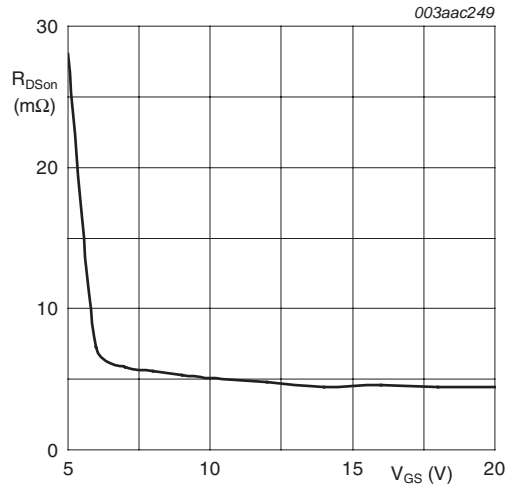
$T_j = 25^\circ\text{C}$

**Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values**



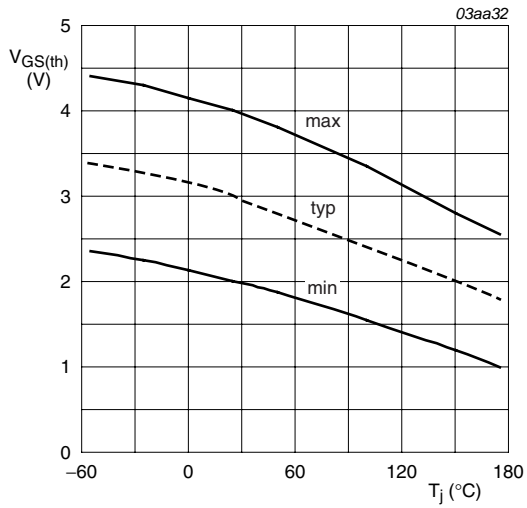
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{ V}$

**Fig 8. Forward transconductance as a function of drain current; typical values**



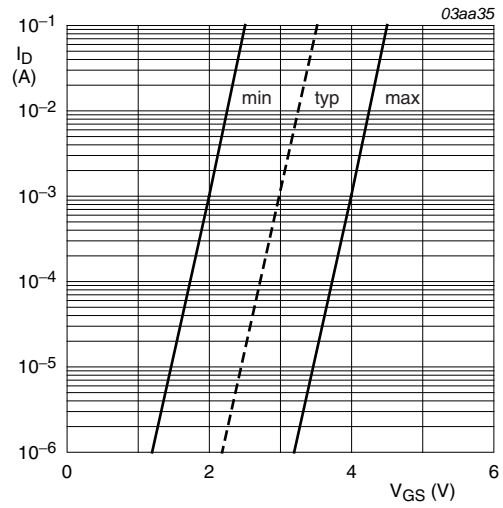
$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

**Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



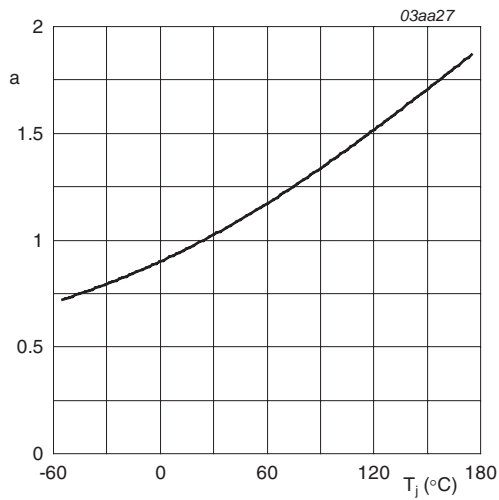
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**



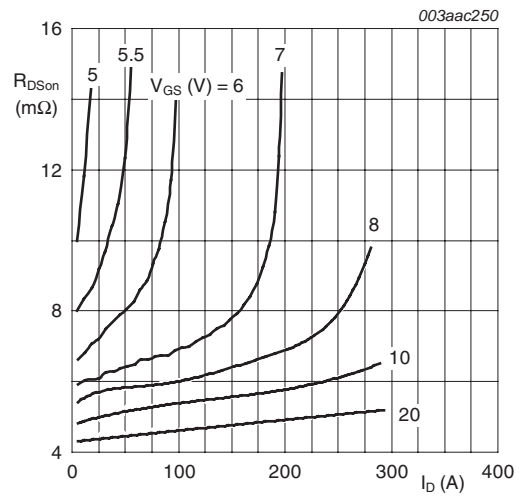
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$$

**Fig 11. Sub-threshold drain current as a function of gate-source voltage**



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

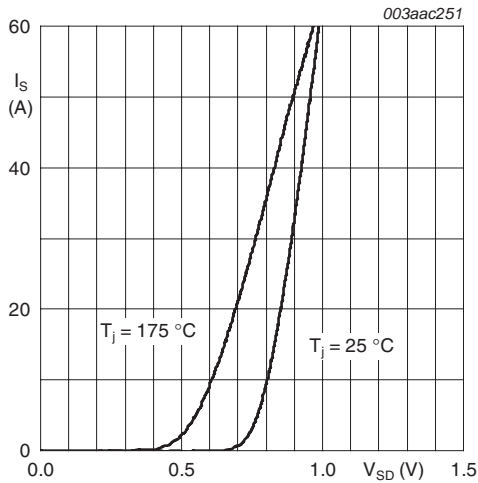
**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**



$$T_j = 25\text{ }^\circ\text{C}$$

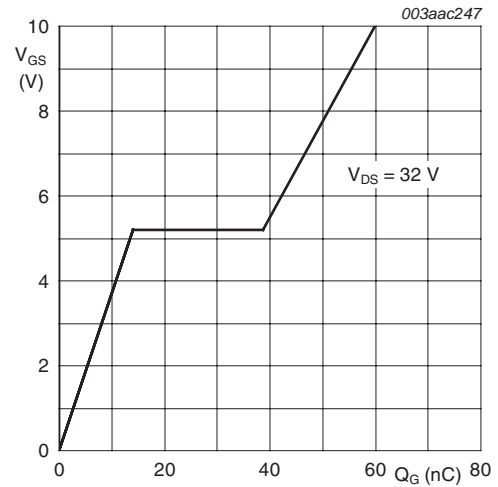
**Fig 13. Drain-source on-state resistance as a function of drain current; typical values**





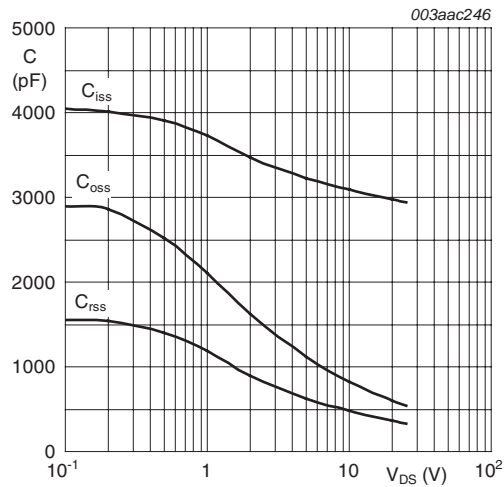
$V_{GS} = 0V$

**Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



$T_j = 25\text{ }^\circ\text{C}; I_D = 25A$

**Fig 15. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0V; f = 1MHz$

**Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

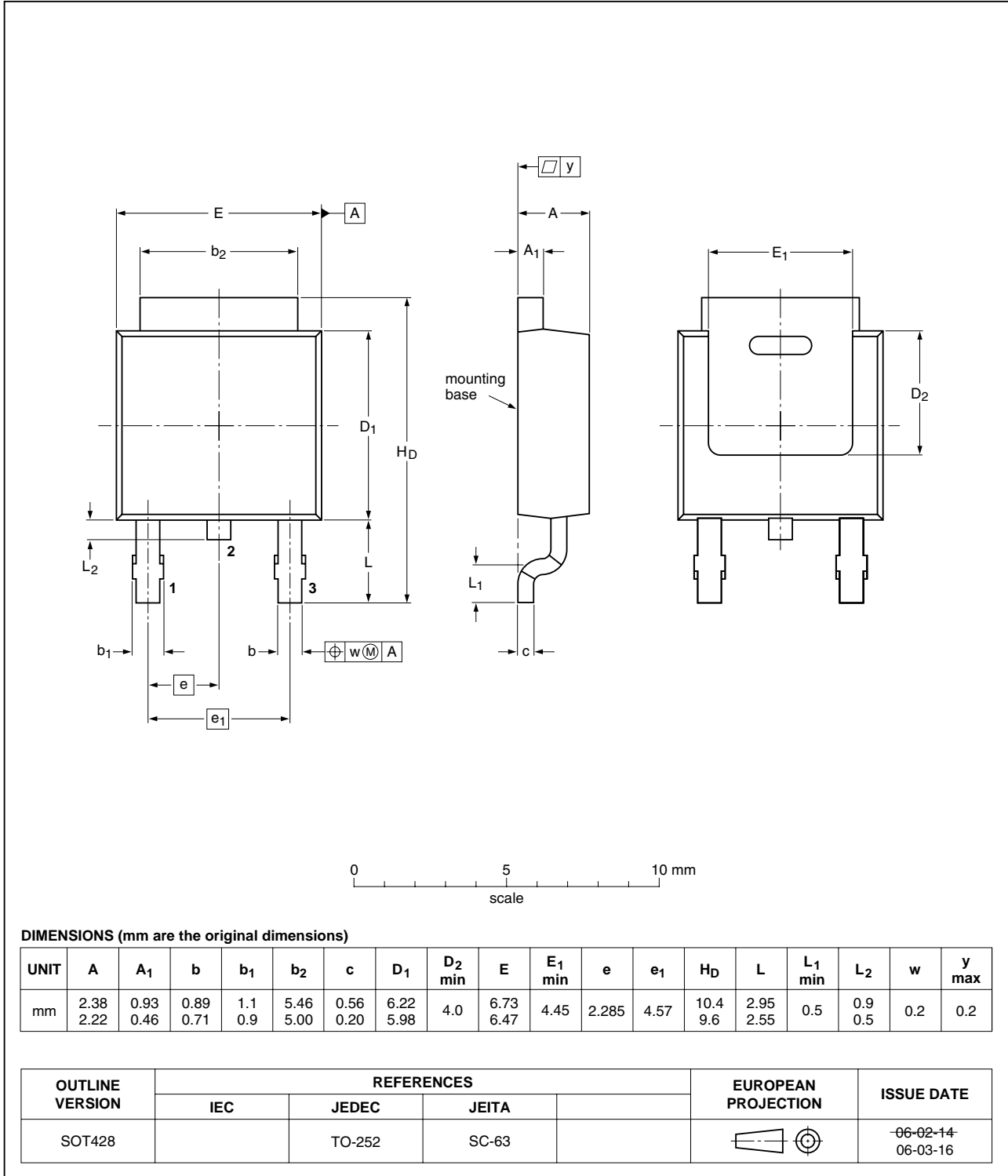


Fig 17. Package outline SOT428 (DPAK)

## 8. Revision history

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Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK725R0-40C_1	20090323	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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