BUK7K3R7-40N

Dual N-channel 40 V, 3.7 mOhm standard level MOSFET in LFPAK56D

3 March 2025 **Product data sheet**

1. General description

Automotive qualified Dual N-channel standard level MOSFET using the latest Trench 15 low ohmic enhanced-Trench Bottom Oxide (e-TBO) technology, providing high ruggedness at low R_{DSon}, housed in an LFPAK56D (Dual Power-SO8) package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Dual MOSFET – two silicon dies in one LFPAK56D package for significant space saving
- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 15 e-TBO technology:
  - Merging benefits of superjunction technology (high ruggedness) and split-gate technology (low R_{DSon})
- Fast and efficient switching with high damping and low spiking
- Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced R_{th}, R_{DSon}, and package inductance
  - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motor, lighting, and solenoid control
- Transmission control
- Ultra high-performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Limiting values FET1 and FET2							
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	105	A
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		2.2	3.2	3.7	mΩ

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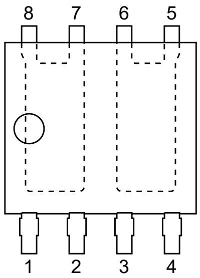
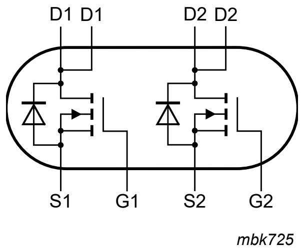
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		28	47	66	nC

[1] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D; Dual LFPAK (SOT1205)	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K3R7-40N	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K3R7-40N	73N740K

8. Limiting values

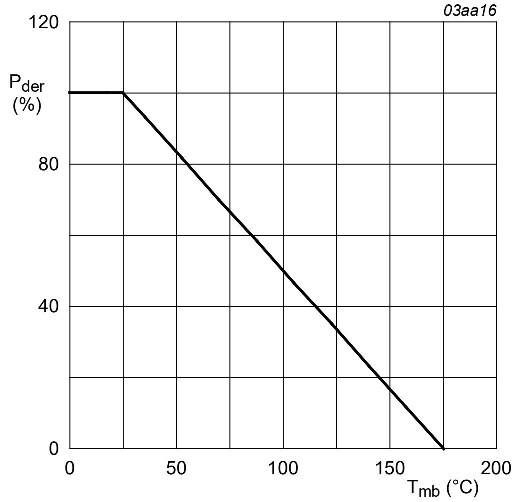
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
Limiting values FET1 and FET2						
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	97	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	105	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	82	A

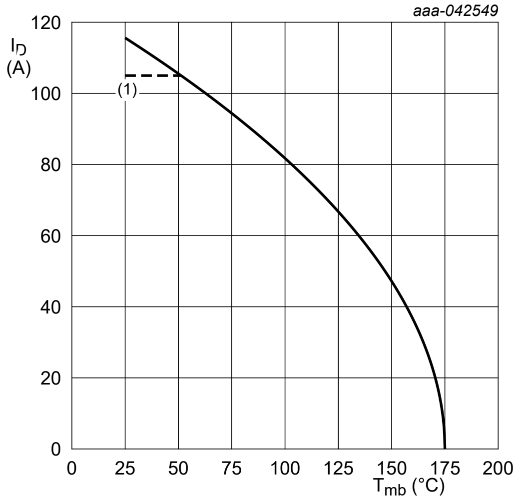
Symbol	Parameter	Conditions		Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C; Fig. 3; Fig. 4	[1]	-	462	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I_S	source current	T_{mb} = 25 °C	[1]	-	97	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	462	A
Avalanche ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 95 A; $V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 5	[2] [3]	-	29.5	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq$ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[4]	-	95	A

[1] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test.



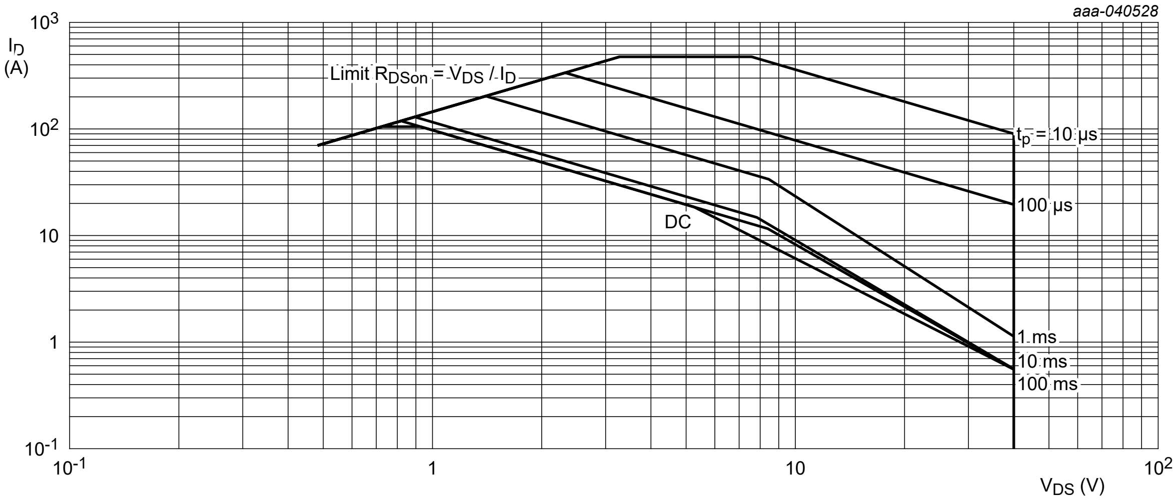
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



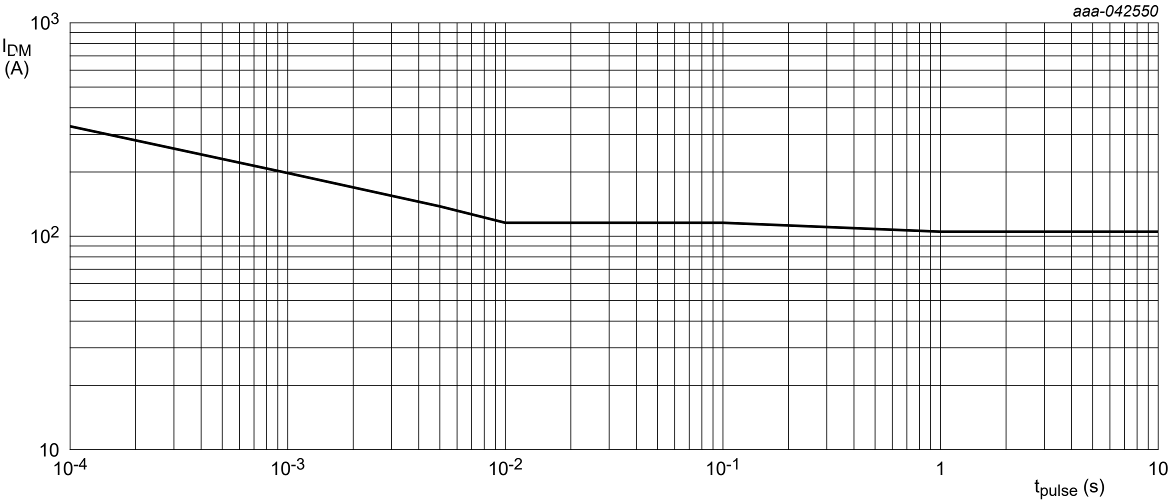
$V_{GS} \geq$ 10 V

Fig. 2. Continuous drain current as a function of mounting base temperature



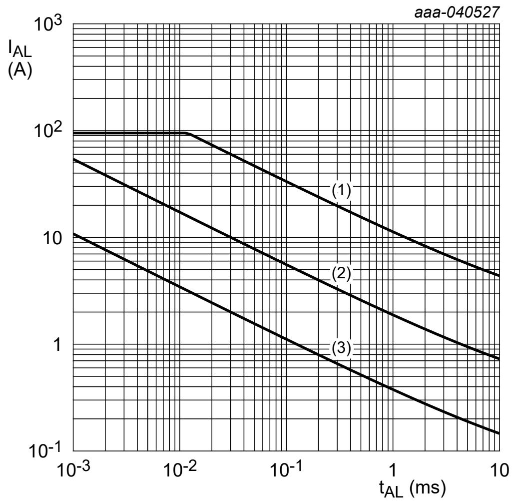
T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



V_{GS} = 10V ; T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 4. Peak Current Capability



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	1.3	1.54	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	30	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

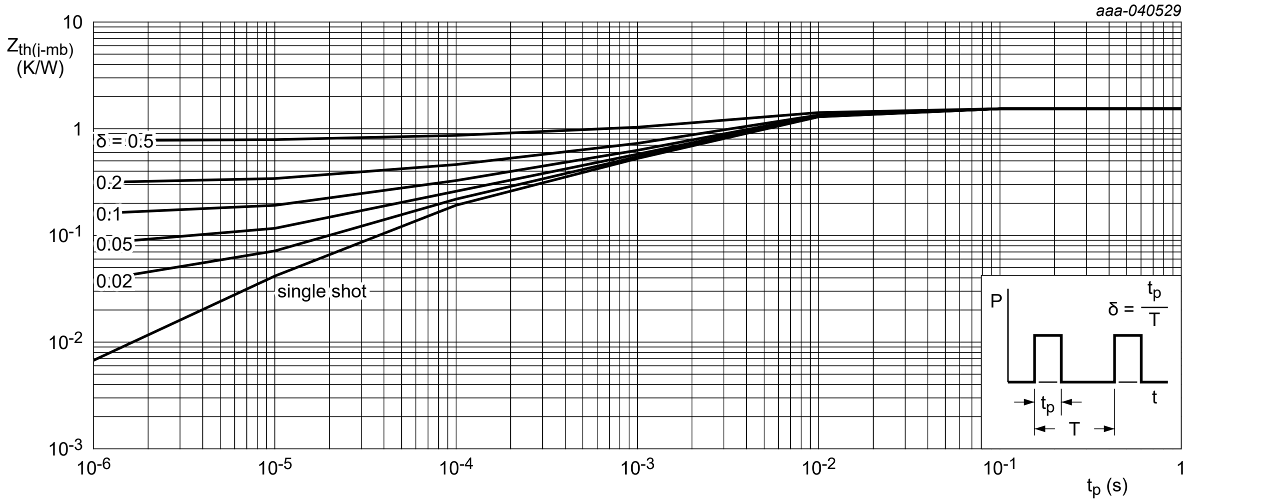


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

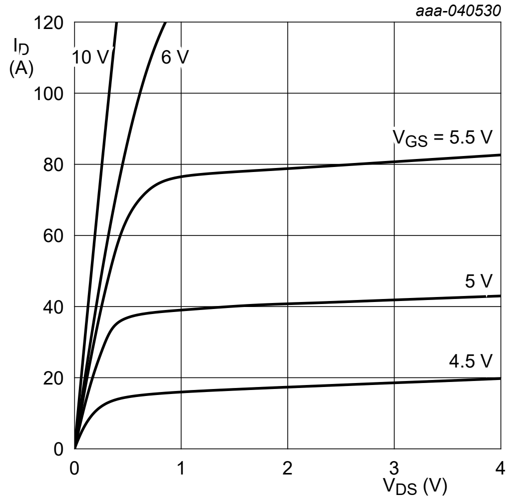
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	43	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	41	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	40.7	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 10		2.4	3	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 11		-	-	4.3	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 11		1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.02	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	0.26	10	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	22	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

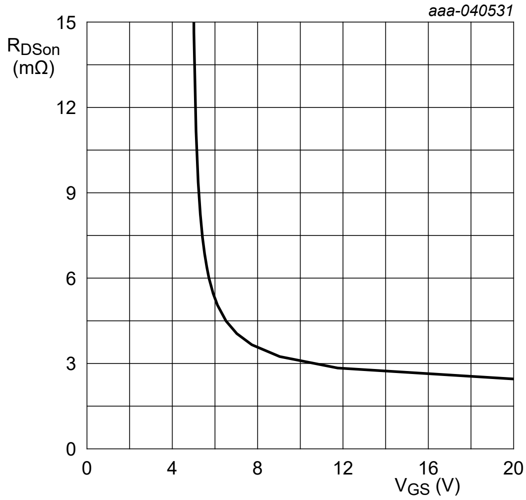
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		2.2	3.2	3.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 13		2.9	4.4	5.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 13		3.2	4.8	6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 13		3.8	5.7	7.3	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		-	1	-	Ω
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		28	47	66	nC
Q_{GS}	gate-source charge			6	10	15	nC
Q_{GD}	gate-drain charge			5	16	28	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		1404	2340	3277	pF
C_{oss}	output capacitance			474	677	880	pF
C_{rss}	reverse transfer capacitance			86	212	342	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	10	-	ns
t_r	rise time			-	22	-	ns
$t_{d(off)}$	turn-off delay time			-	27	-	ns
t_f	fall time			-	22	-	ns
Source-drain diode FET1 and FET2							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.84	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 18		-	22	-	ns
Q_r	recovered charge		[1]	-	11	-	nC

[1] includes capacitive recovery



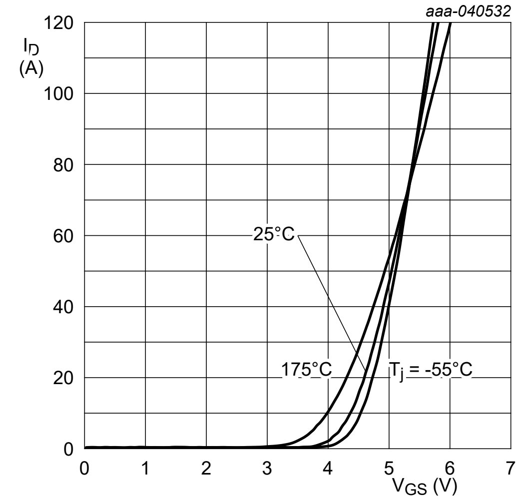
T_j = 25 °C

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values



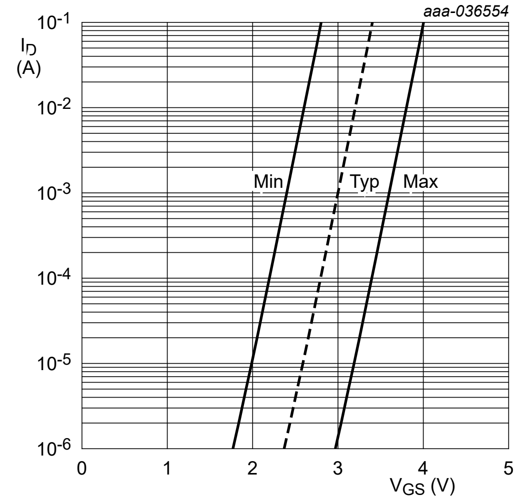
T_j = 25 °C; I_D = 25 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



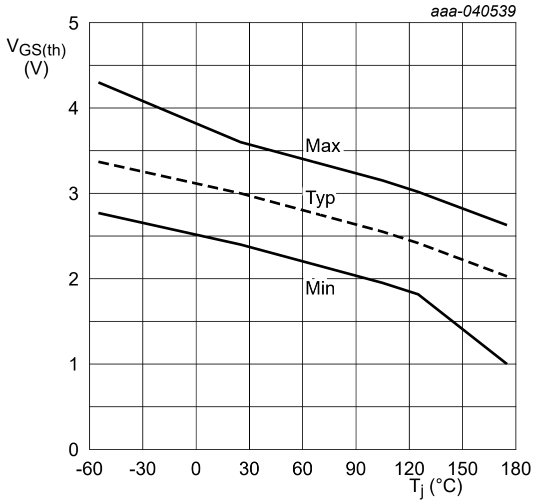
V_{DS} = 8 V

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



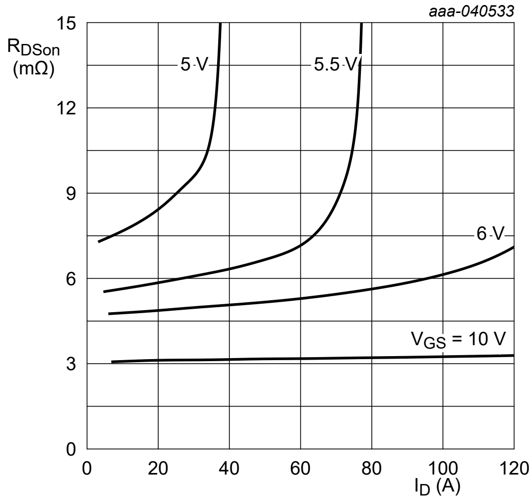
T_j = 25 °C; V_{DS} = 5 V

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



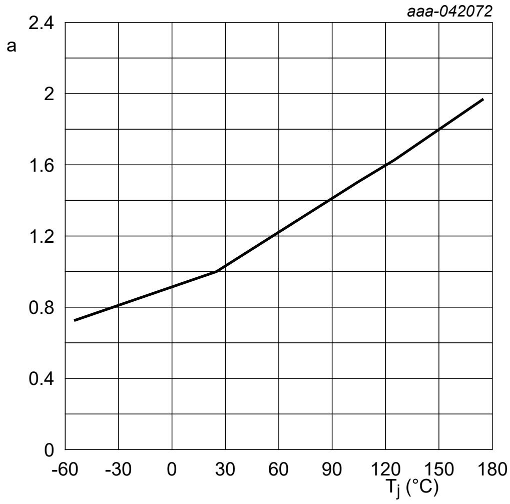
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 11. Gate-source threshold voltage as a function of junction temperature



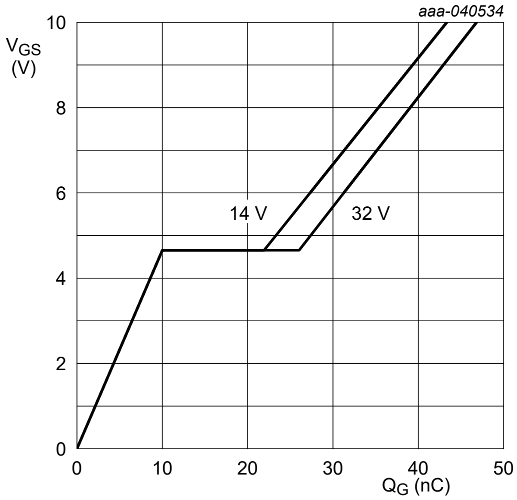
T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25°C)}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

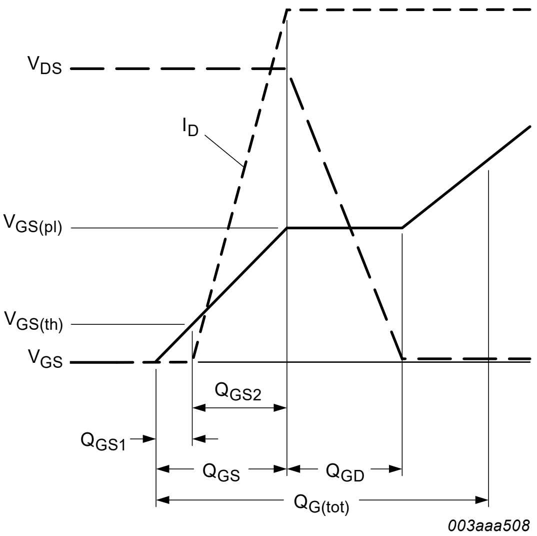
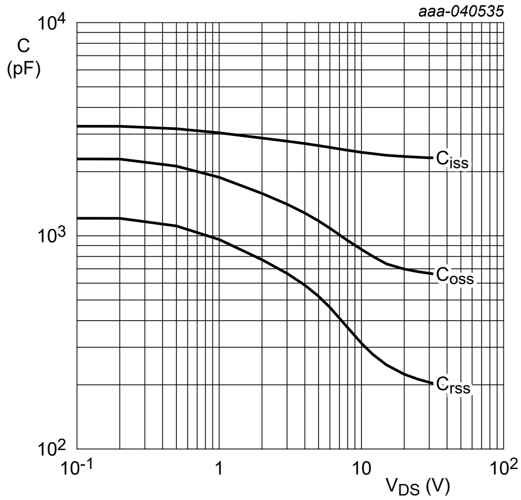
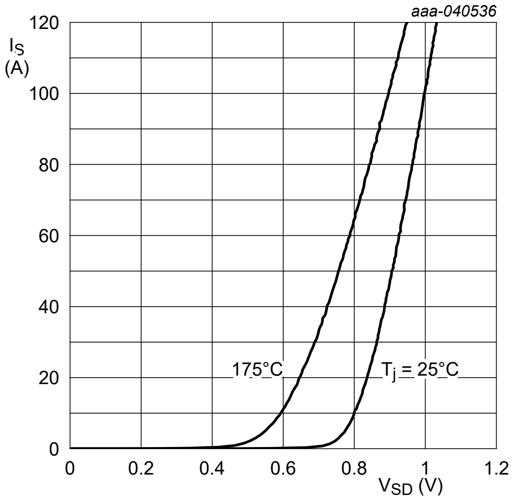


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

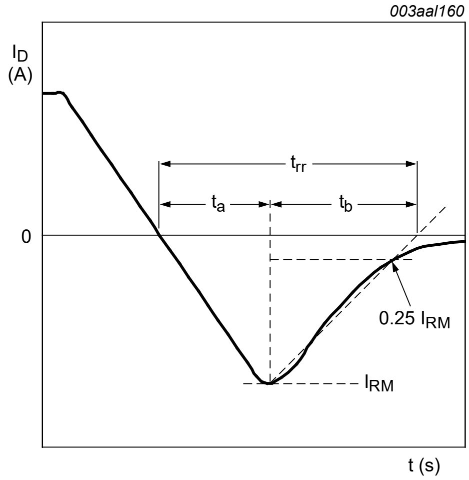
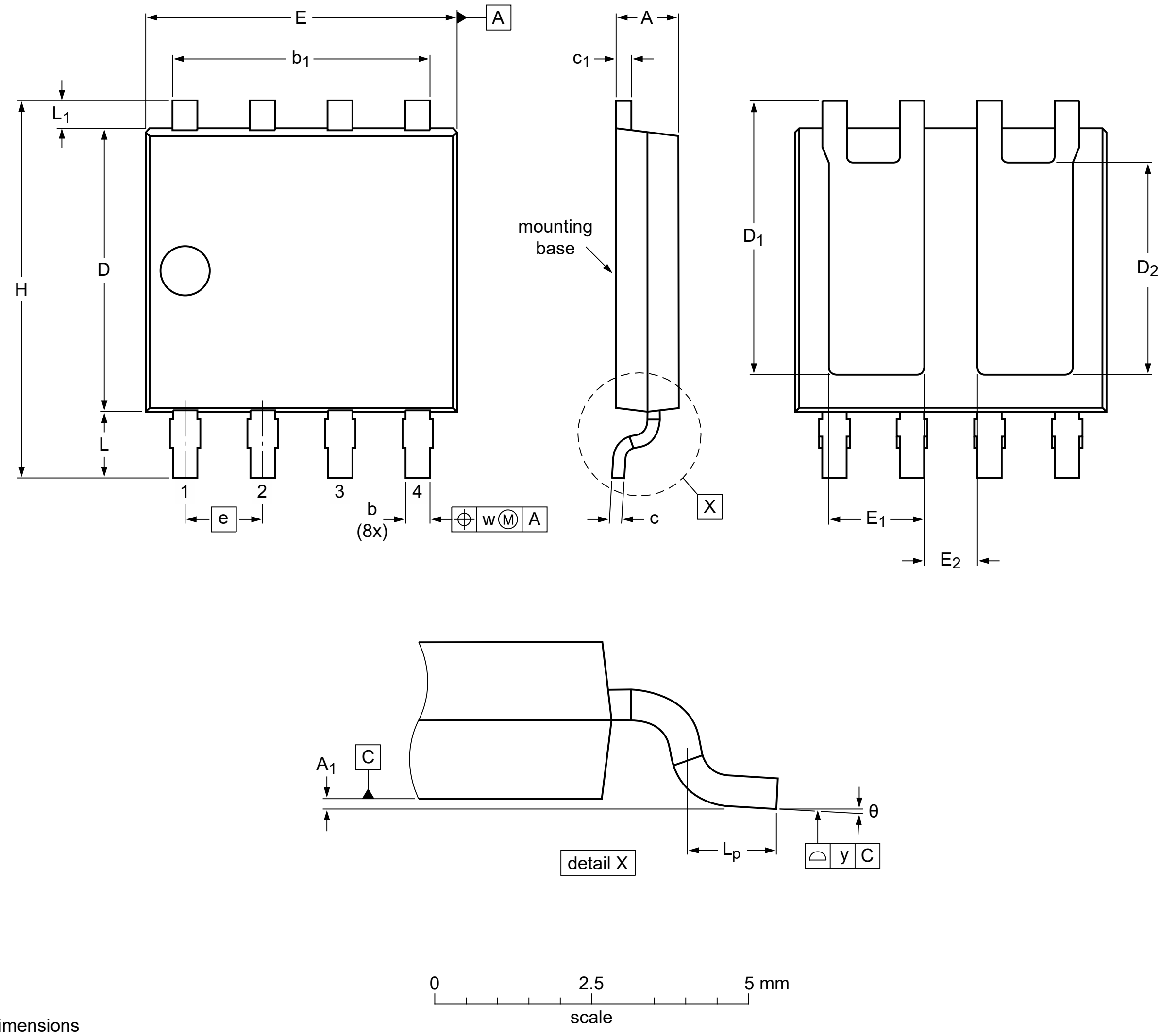


Fig. 18. Reverse recovery timing definition

11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	D(1)	D_1(1)	D_2 (ref)	E(1)	E_1(1)	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 19. Package outline LFPAK56D; Dual LFPAK (SOT1205)

12. Soldering

Footprint information for reflow soldering of LFPAK56D package **SOT1205**

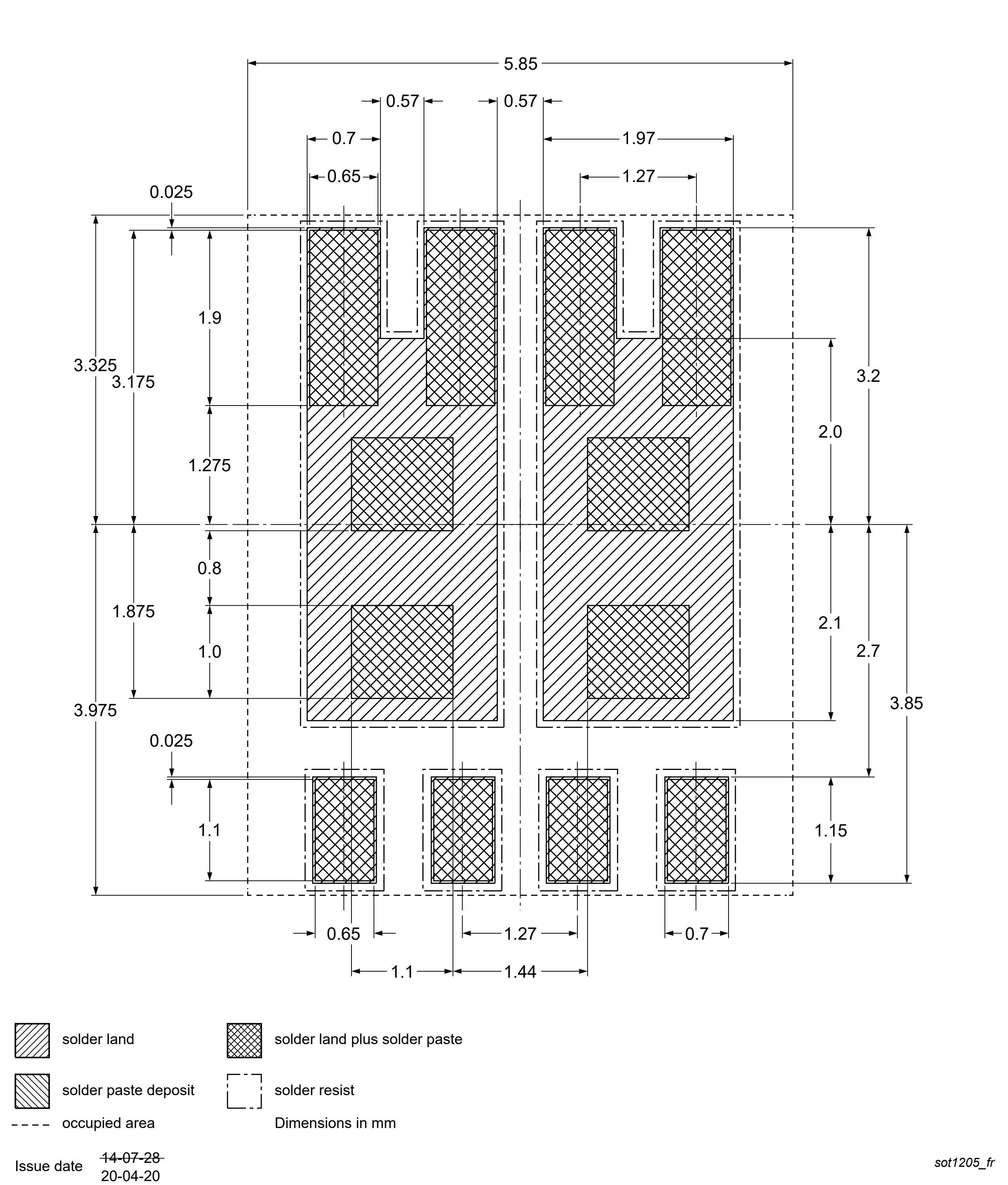


Fig. 20. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 3 March 2025