



# BUK7S1R2-40H

N-channel 40 V, 1.2 m $\Omega$  standard level MOSFET in LPAK88

10 January 2025

Product data sheet

## 1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a copper-clip LPAK88 package. This product has been fully designed and qualified to meet beyond AEC-Q101 requirements delivering high performance and reliability.

## 2. Features and benefits

- Fully automotive qualified to beyond AEC-Q101:
  - 55 °C to +175 °C rating suitable for thermally demanding environments
- LPAK88 package:
  - Designed for smaller footprint and improved power density over older wire bond packages such as D<sup>2</sup>PAK for today's space constrained high power automotive applications
  - Thin package and copper clip enables LPAK88 to be highly efficient thermally
- LPAK copper clip technology enabling improvements over wire bond packages by:
  - Increased maximum current capability and excellent current spreading
  - Improved  $R_{DSon}$
  - Low source inductance
  - Low thermal resistance  $R_{th}$
- LPAK Gull Wing leads:
  - Flexible leads enabling high Board Level Reliability absorbing mechanical and thermal cycling stress, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- Unique 40 V Trench 9 superjunction technology:
  - Reduced cell pitch and superjunction platform enables lower  $R_{DSon}$  in the same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight  $V_{GS(th)}$  limits enable easy paralleling of MOSFETs

## 3. Applications

- 12 V automotive systems
- 48 V DC/DC systems (on 12 V secondary side)
- Higher power motors, lamps and solenoid control
- Reverse polarity protection
- LED lighting
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	25 °C $\leq T_j \leq$ 175 °C		-	-	40	V
$I_D$	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; <a href="#">Fig. 2</a>	[1]	-	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C; <a href="#">Fig. 1</a>		-	-	294	W

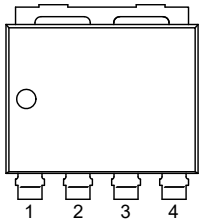
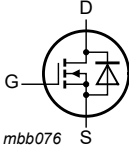
N-channel 40 V, 1.2 mΩ standard level MOSFET in LFPAK88

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_J = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 11</a>	0.74	1.06	1.2	mΩ
Dynamic characteristics						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	14	28	nC
Source-drain diode						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ <a href="#">[2]</a>	-	38	-	nC
S	softness factor	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_J = 25\text{ }^{\circ}\text{C}$	-	0.82	-	

- [1] 300A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating emperature.
- [2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	 mbb076
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">BUK7S1R2-40H</a>	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	<a href="#">SOT1235</a>

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7S1R2-40H	7S1R240H

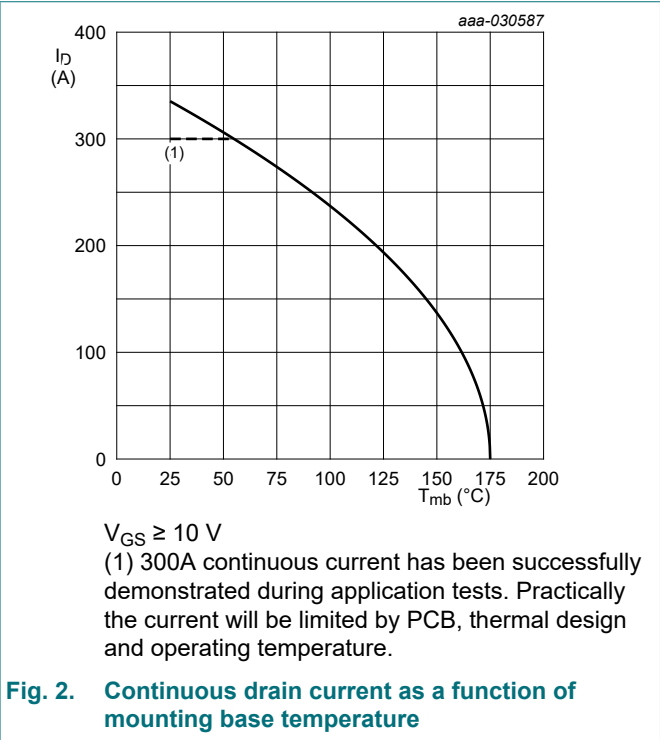
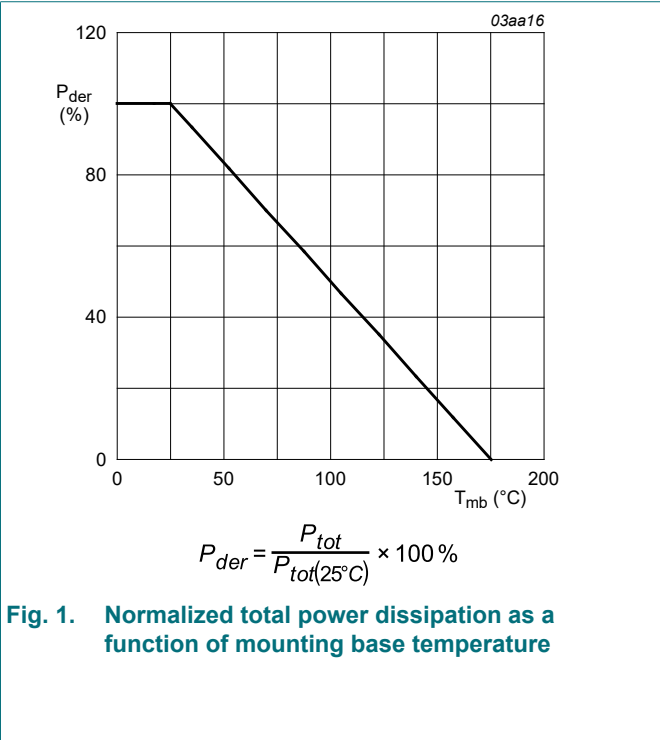
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
V <sub>GS</sub>	gate-source voltage		[1]	-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1		-	294	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2	[2]	-	300	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3		-	1341	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[3]	-	294	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1341	A
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; Fig. 4	[4] [5]	-	277	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω; Fig. 4	[6]	-	199	A

- [1] Refer to application note AN90001 for further information.
- [2] 300A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating emperature.
- [3] 294A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating temperature.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.
- [6] Protected by 100% test.



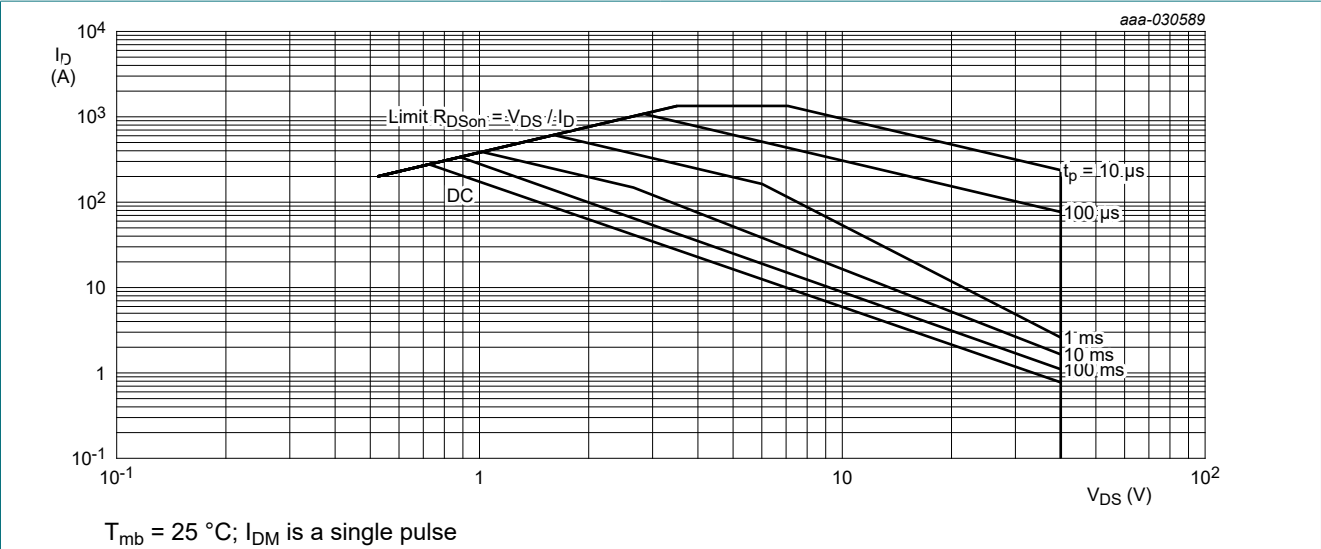


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

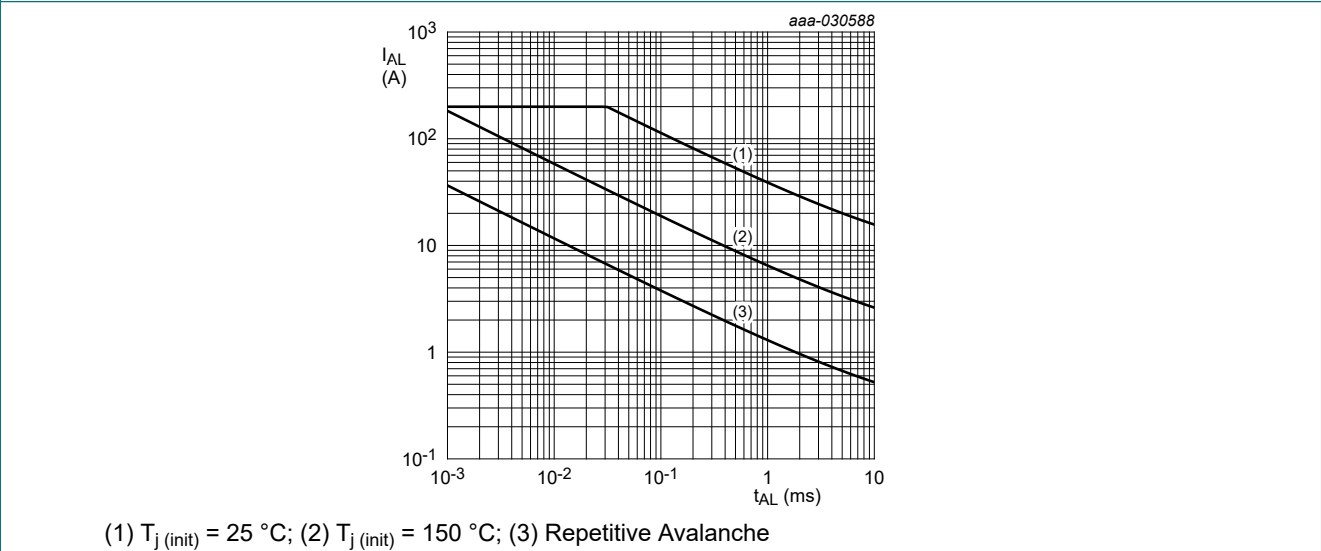


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W

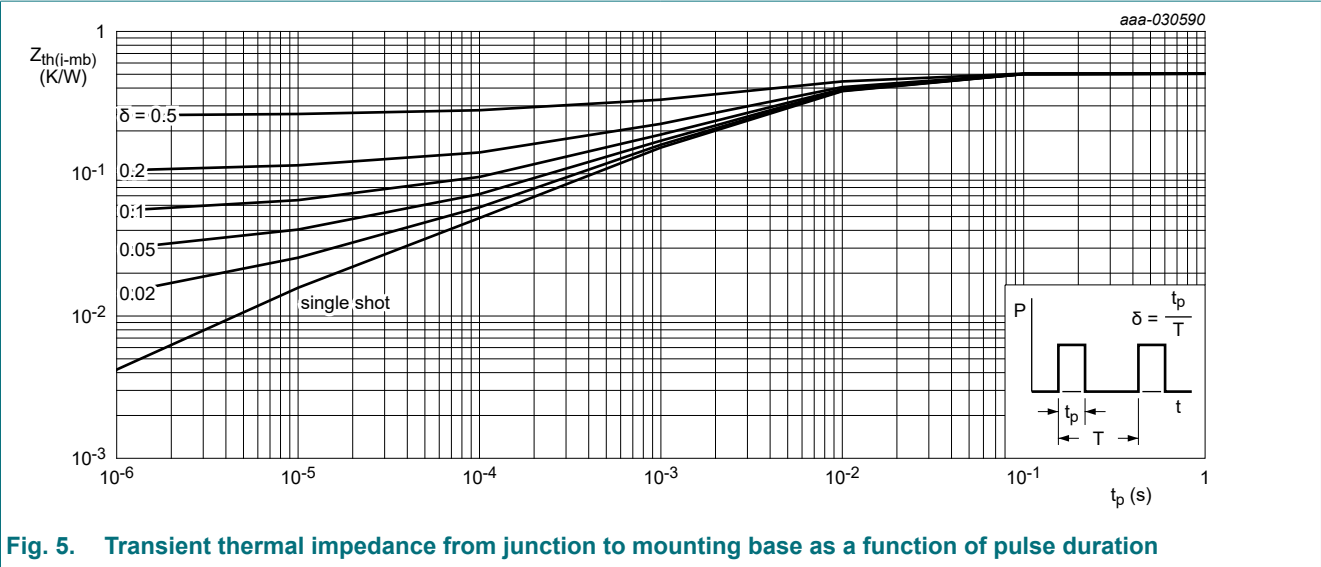


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

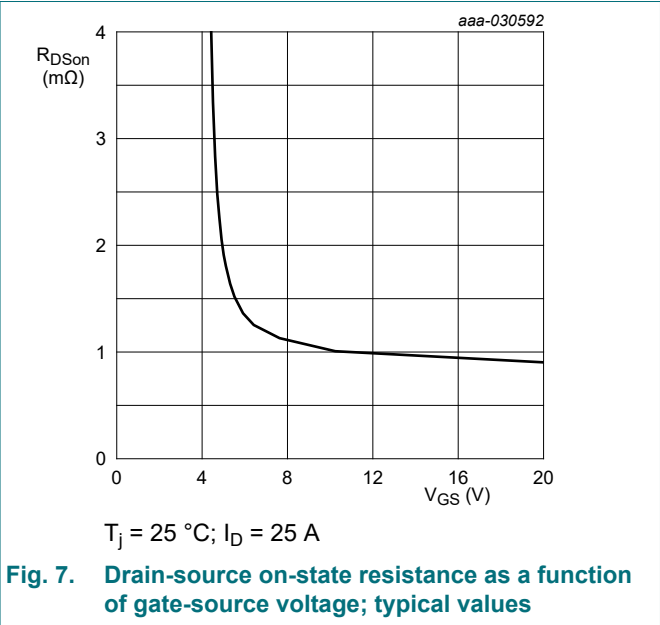
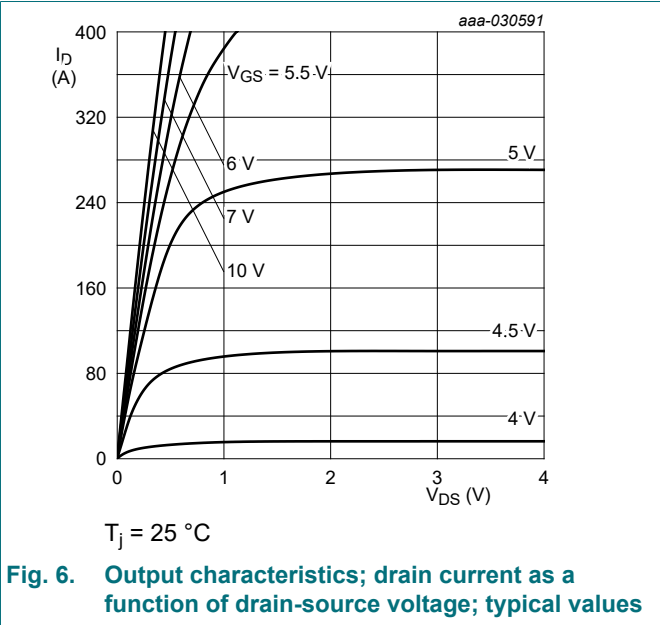
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	40	43	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -40 °C	-	40.5	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C	36	40	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = 25 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	2.4	3	3.6	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = -55 °C; <a href="#">Fig. 10</a>	-	-	4.3	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = 175 °C; <a href="#">Fig. 10</a>	1	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	0.06	1.2	μA
		V <sub>DS</sub> = 16 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 125 °C	-	1.6	25	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 175 °C	-	180	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>	0.74	1.06	1.2	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 105 °C; <a href="#">Fig. 12</a>	1.05	1.59	1.9	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 125 °C; <a href="#">Fig. 12</a>	1.16	1.76	2.1	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 12</a>	1.46	2.21	2.6	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C	0.4	1.05	2.6	Ω
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	80	112	nC
Q <sub>GS</sub>	gate-source charge		-	22	33	nC
Q <sub>GD</sub>	gate-drain charge		-	14	28	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>		-	6014	8420	pF
C <sub>oss</sub>	output capacitance			-	1352	1893	pF
C <sub>rss</sub>	reverse transfer capacitance			-	244	537	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω		-	19	-	ns
t <sub>r</sub>	rise time			-	16	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	50	-	ns
t <sub>f</sub>	fall time			-	22	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>		-	0.77	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V		-	39	-	ns
Q <sub>r</sub>	recovered charge		<a href="#">[1]</a>	-	38	-	nC
S	softness factor	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C		-	0.82	-	
		I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -500 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C		-	0.73	-	

[1] includes capacitive recovery



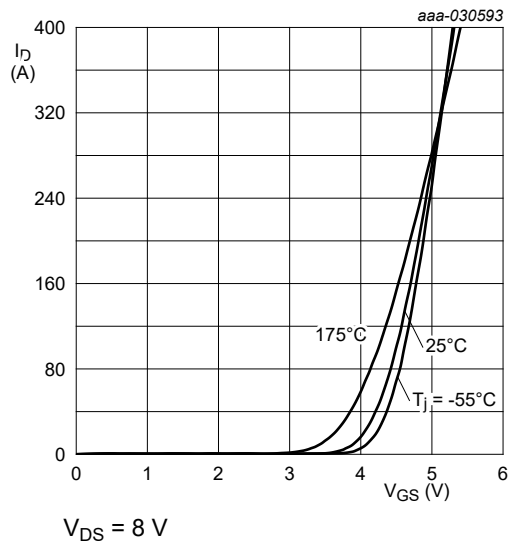


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

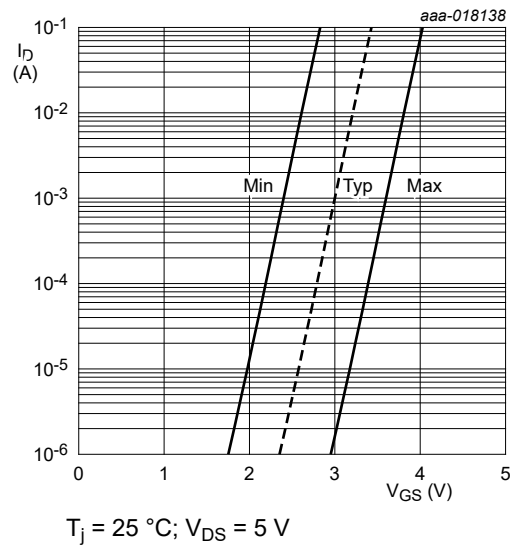


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

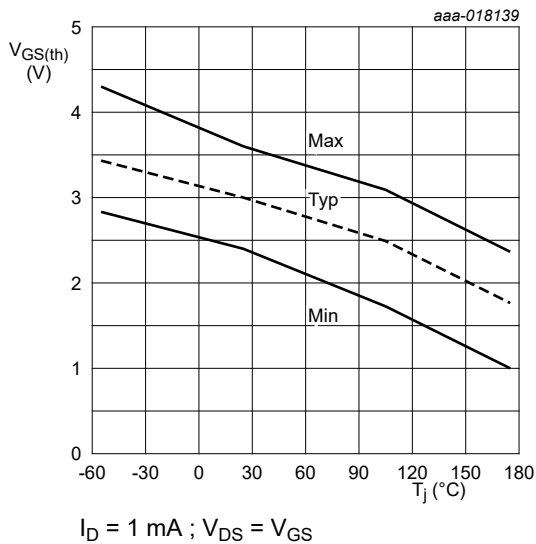


Fig. 10. Gate-source threshold voltage as a function of junction temperature

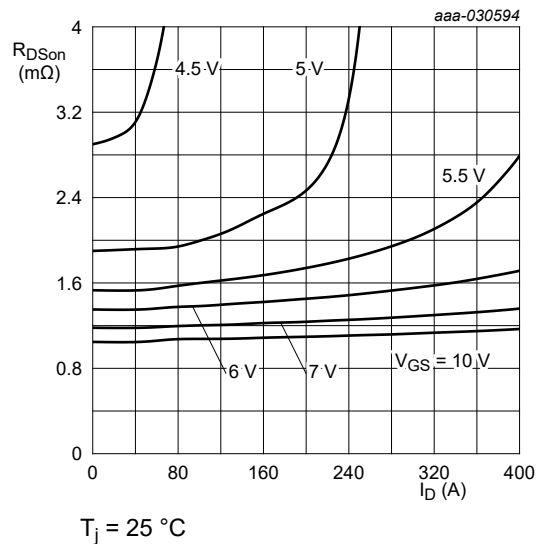


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

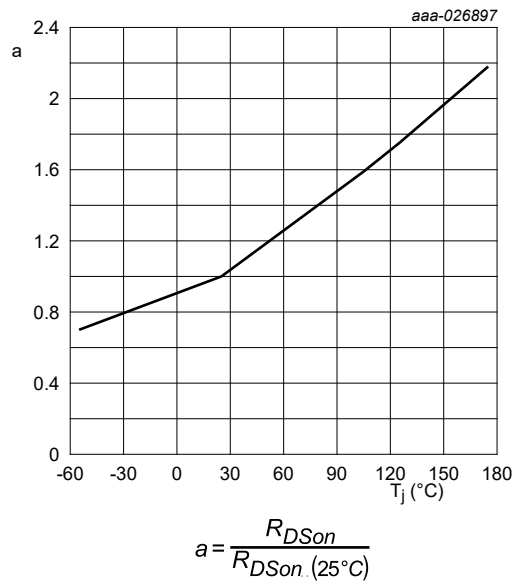


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

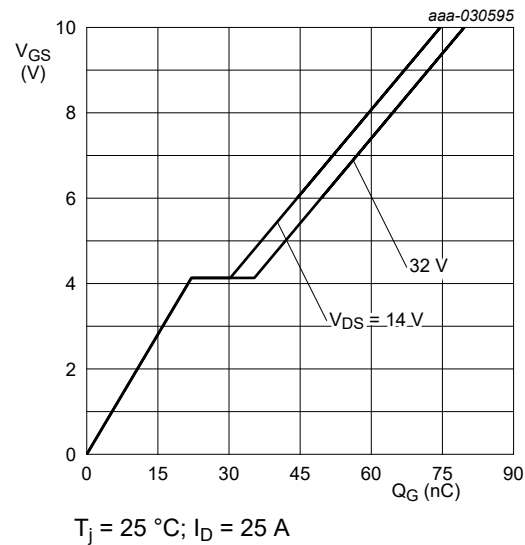


Fig. 13. Gate-source voltage as a function of gate charge; typical values

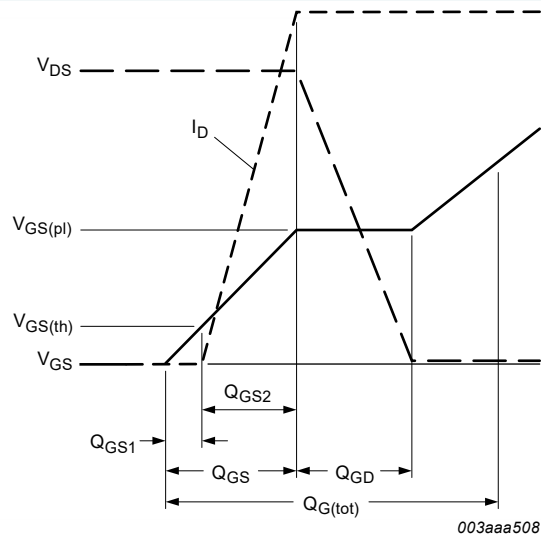


Fig. 14. Gate charge waveform definitions

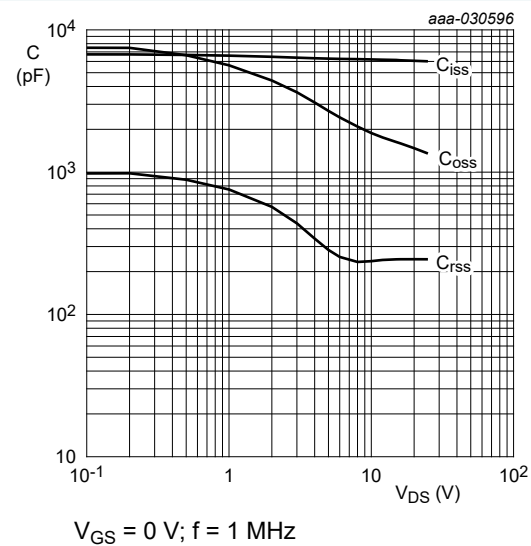
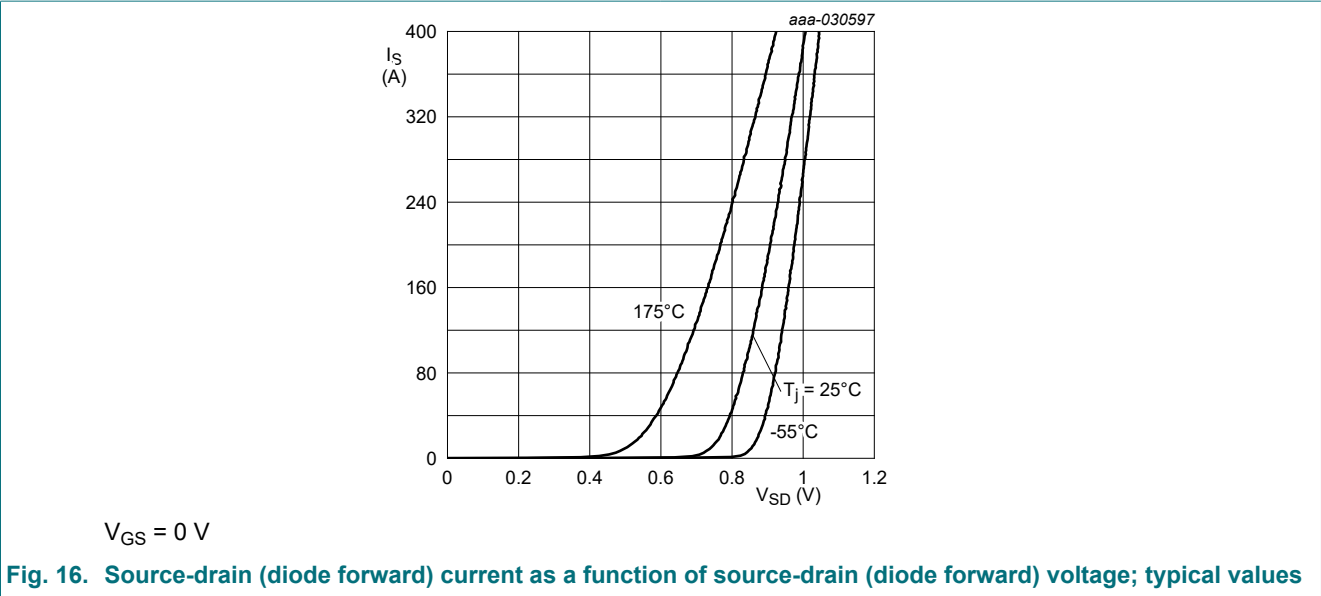


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





11. Package outline

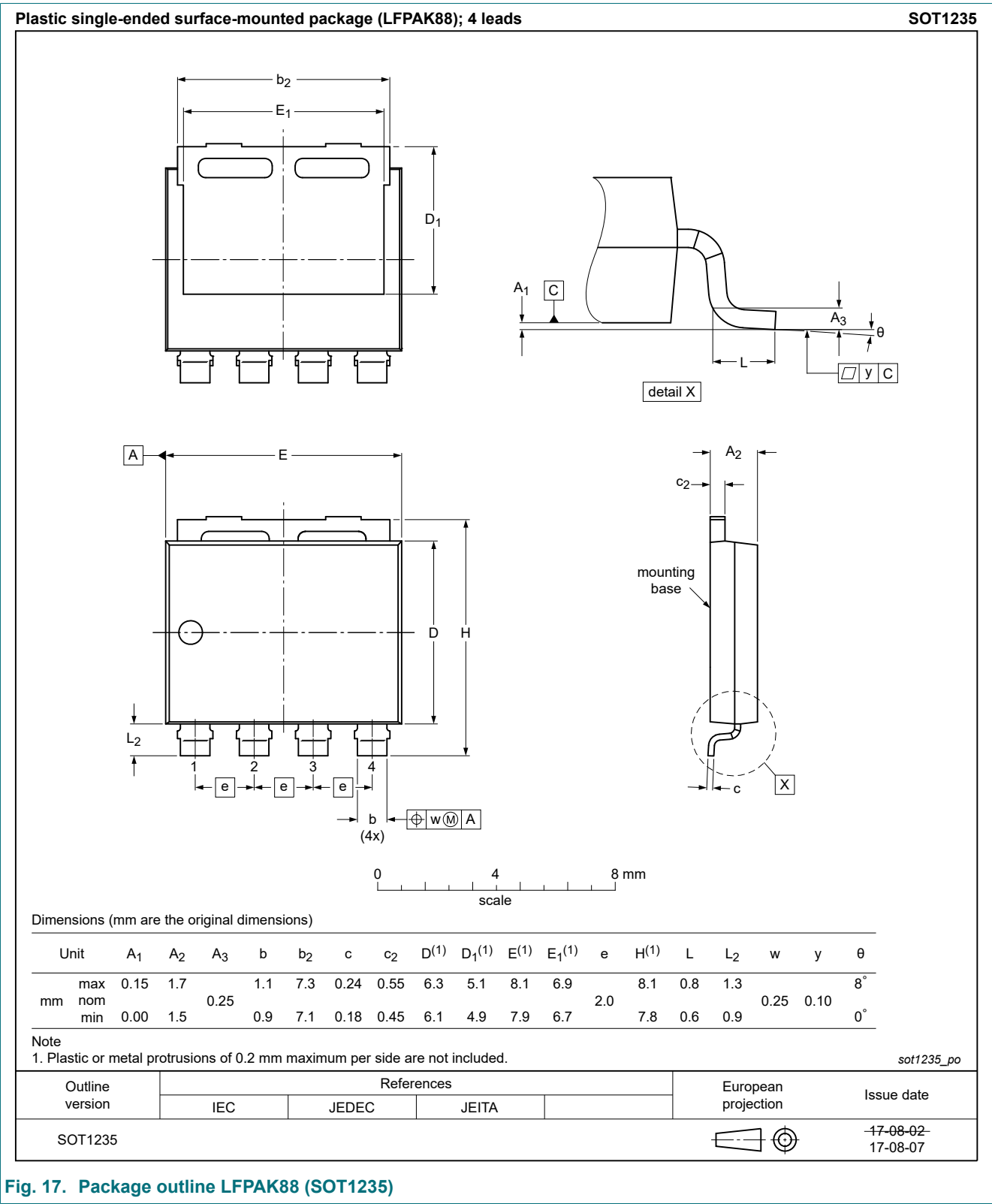
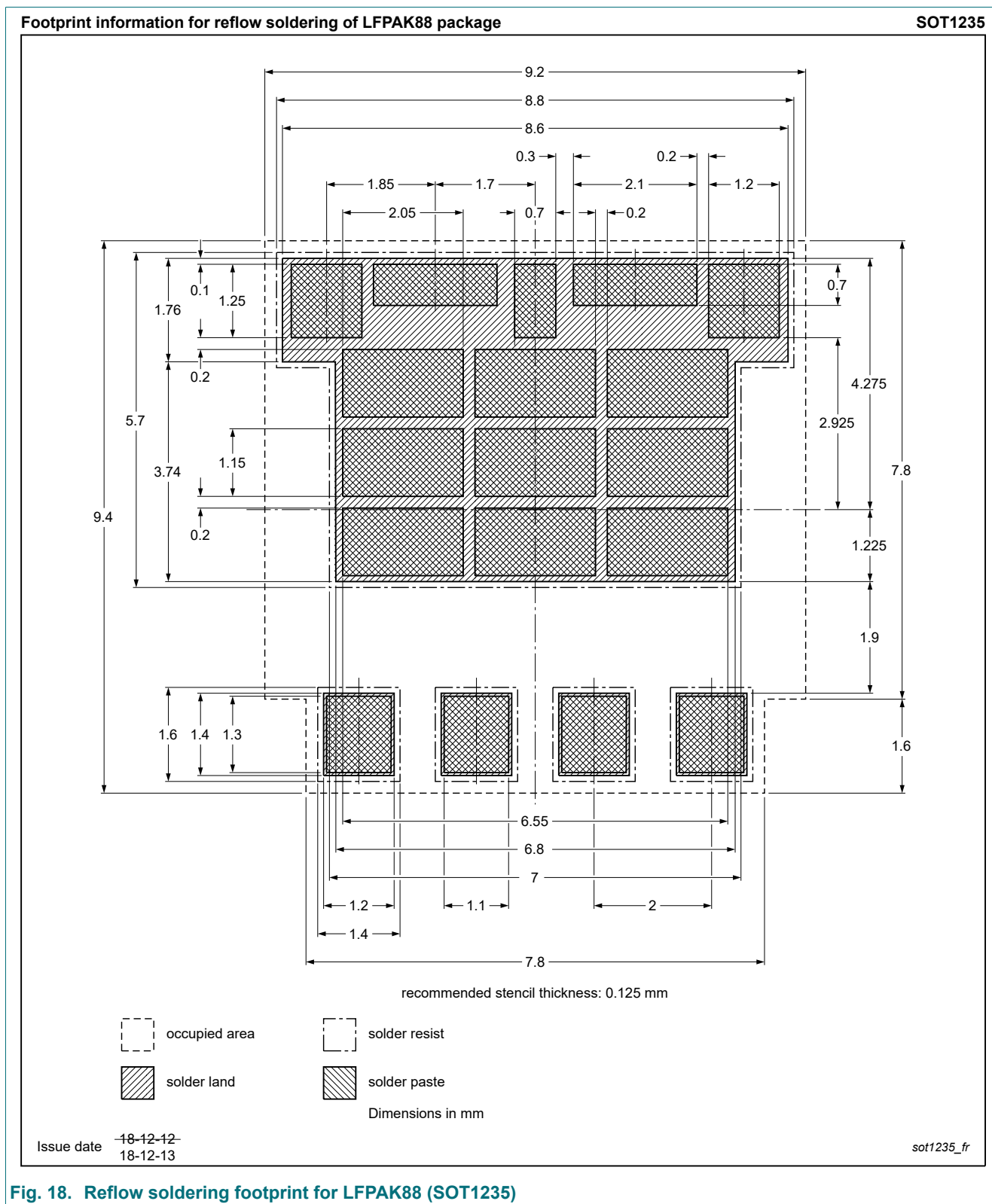


Fig. 17. Package outline LPAK88 (SOT1235)

## 12. Soldering



**Fig. 18. Reflow soldering footprint for LPAK88 (SOT1235)**

### 13. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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