



BUK7T1R4-100L

N-channel 100V, 1.35m Ω , Standard Level MOSFET in CCPAK1212i

26 August 2025

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 12 low ohmic split-gate technology, for ultra-low $R_{DS(on)}$ capability, housed in a CCPAK1212i (SOT8005A) package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

Fully automotive qualified to AEC-Q101:

- 175 °C rating suitable for thermally demanding automotive environments.

Trench 12 split-gate trench technology:

- Reduced cell pitch enables enhanced power density resulting in lower conduction losses.
- Fast and efficient switching with optimal damping for low spiking and improved switching efficiency.

CCPAK mounting base

- Large cross-sectional area of exposed drain tab for excellent thermal dissipation and low steady state thermal resistance.

CCPAK gull-wing leads:

- High Board Level Reliability (BLR), pins absorbing mechanical stress during thermal cycling.
- Visual (AOI) soldering inspection, no need for expensive x-ray equipment.

CCPAK copper clip technology:

- Low transient thermal resistance and package inductance.
- High maximum current capability and improved current spreading on silicon die.

3. Applications

- Light-electric / Electric vehicle applications
- 48V to 12V DC-DC Converters
- Synchronous rectifier for On-Board Charging (OBC) systems
- 48V Traction Inverters
- 48V Belt Starter Generator (BSG)
- Battery Management Systems

4. Quick reference data

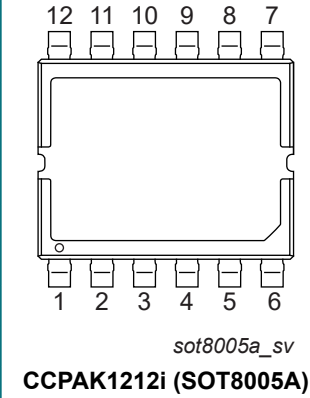
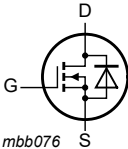
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C $\leq$ T_j $\leq$ 175 °C	-	-	100	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; Fig. 2	-	-	355	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 1	-	-	935	W
T_j	junction temperature		-55	-	175	°C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 9		-	1.07	1.35	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 10		-	2.4	3.1	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 11 ; Fig. 12		14	46	106	nC
Q _{G(tot)}	total gate charge	I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	228	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	G	gate		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7T1R4-100L	CCPAK1212i	Plastic, surface mounted copper clip package (CCPAK1212i); 12 terminals; 2.0 mm pitch, 12 mm × 12 mm × 2.5 mm body	SOT8005A

7. Marking

Table 4. Marking codes

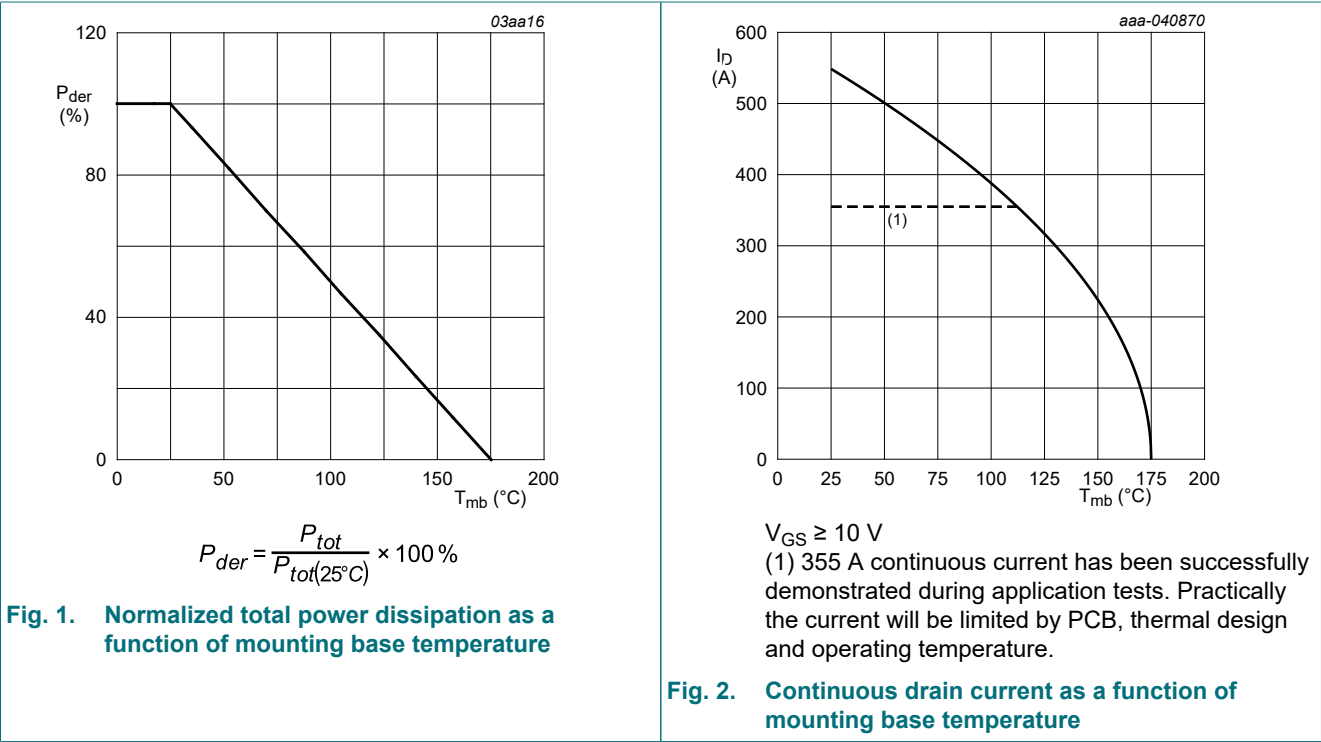
Type number	Marking code
BUK7T1R4-100L	X7T1R410L

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ		-	100	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	935	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	355	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	355	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	2195	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	355	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	2195	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 99 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 175 μs; Fig. 4	[1]	-	1130	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	99	A

[1] Protected by 100% test



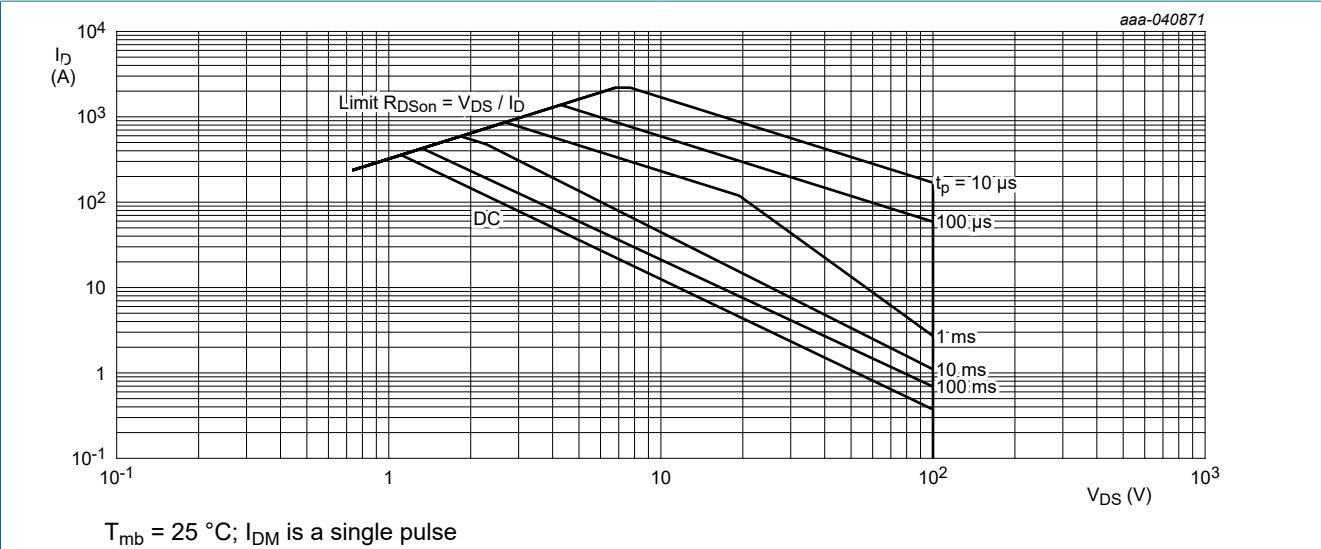


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

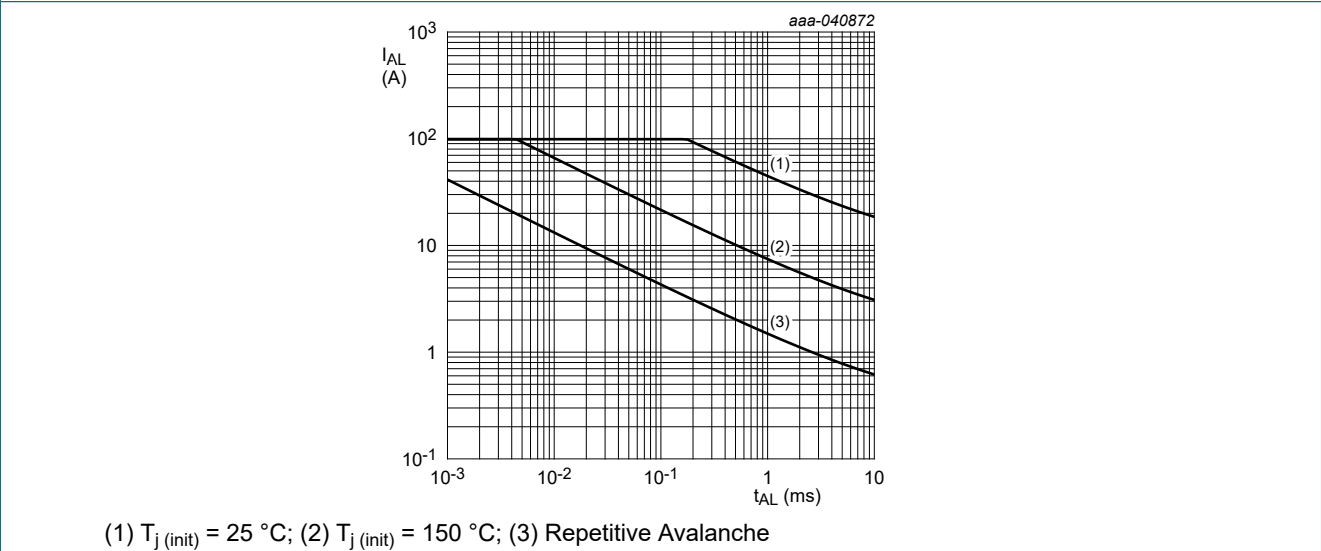


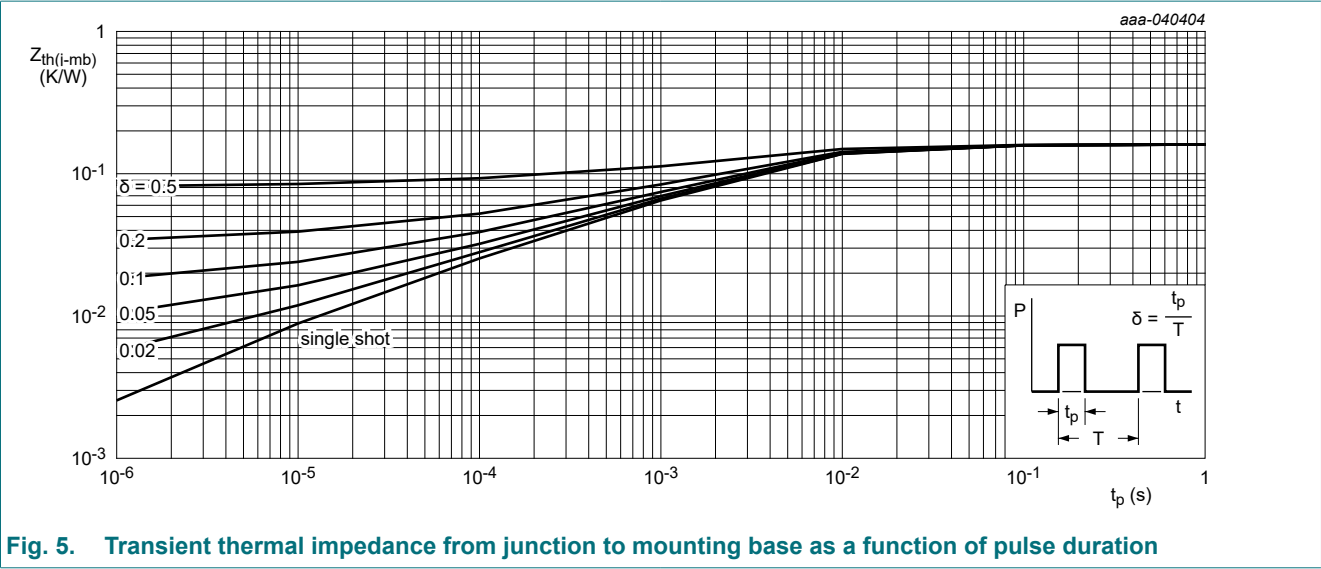
Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.123	0.16	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	30	-	K/W
		With exposed pad contacting a fixed temperature heatsink. Thermal interface material is 50 μm thick and has 0.5W/mK thermal conductivity.	[1]	1.2	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C		2	3.1	4	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C		-	1.61	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C		-	3.7	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _J ≤ 150 °C		-	-9.4	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _J = 25 °C		-	0.05	1.6	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _J = 125 °C		-	35	160	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 9		-	1.07	1.35	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 100 °C; Fig. 10		-	1.7	2.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 10		-	2.4	3.1	mΩ
		V _{GS} = 7 V; I _D = 25 A; T _J = 25 °C; Fig. 9		-	1.36	2.04	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.51	1.02	2.05	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 11 ; Fig. 12		128	255	383	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C		-	228	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 11 ; Fig. 12		46	76.5	107	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	51	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	25.4	-	nC
Q _{GD}	gate-drain charge			14	46	106	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; T _J = 25 °C; Fig. 11 ; Fig. 12		-	4.4	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 13		10901	18168	25436	pF
C _{oss}	output capacitance			2494	4157	6652	pF
C _{rss}	reverse transfer capacitance			9	92	239	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	67	-	ns
t _r	rise time			-	63	-	ns
t _{d(off)}	turn-off delay time			-	157	-	ns
t _f	fall time			-	84	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 14		-	0.76	1	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;		-	62	-	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15		-	74	-	nC

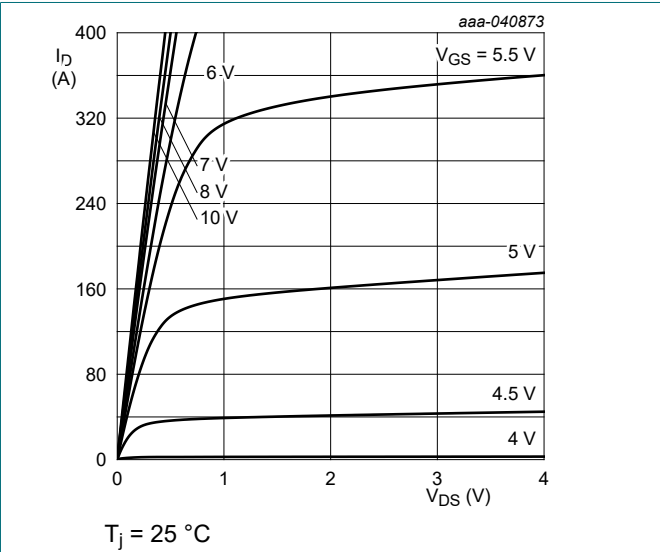


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

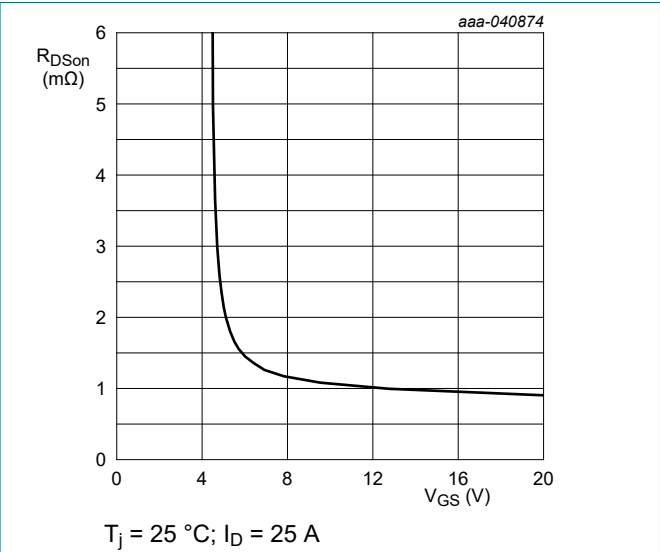


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

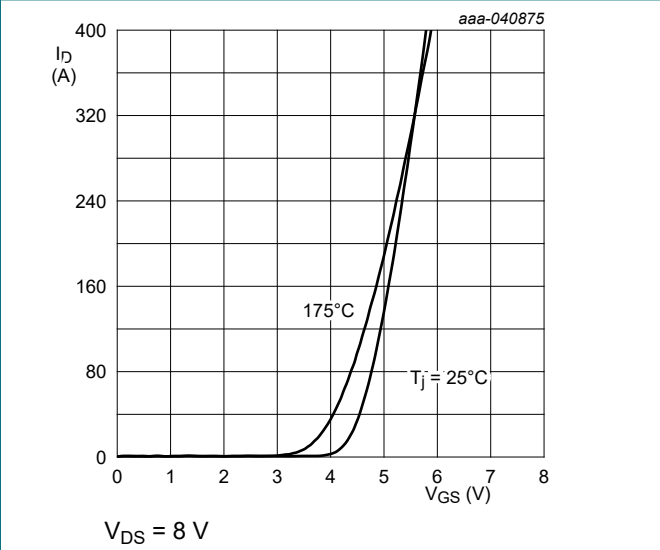


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

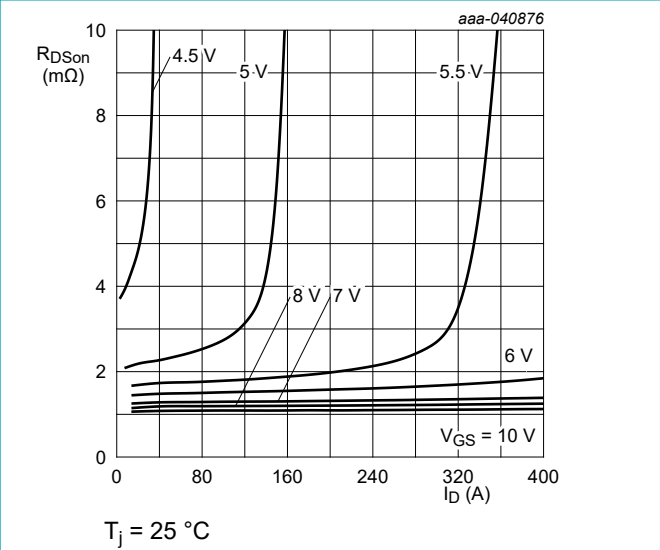


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

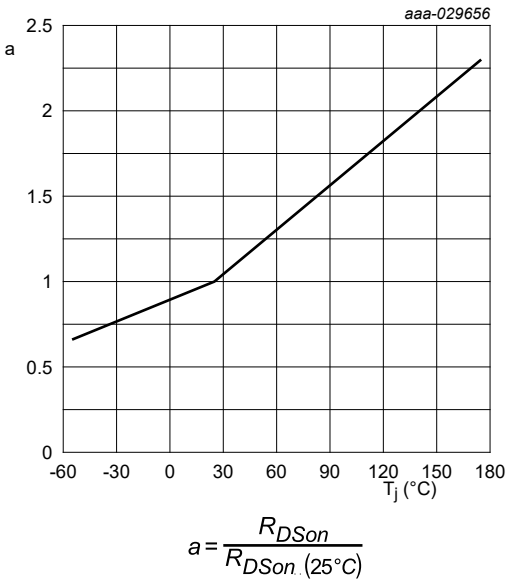


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

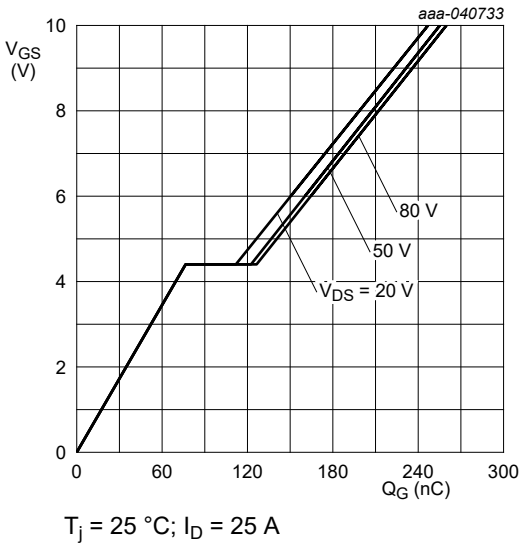


Fig. 11. Gate-source voltage as a function of gate charge; typical values

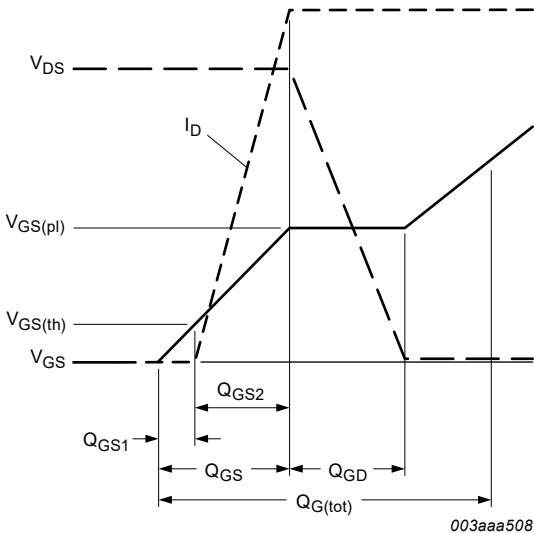


Fig. 12. Gate charge waveform definitions

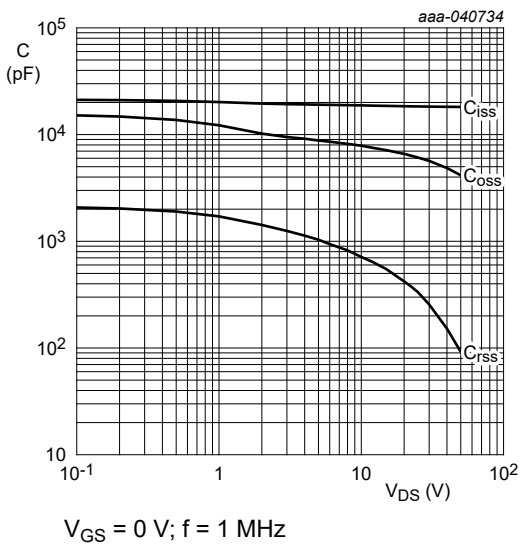


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

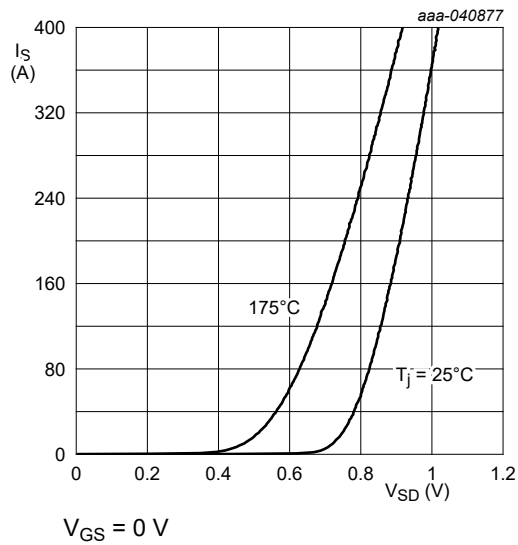


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

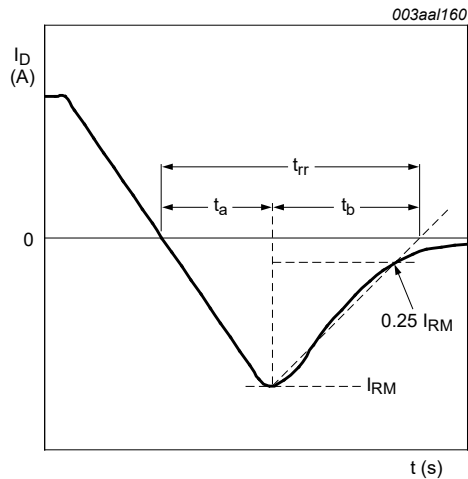


Fig. 15. Reverse recovery timing definition

11. Package outline

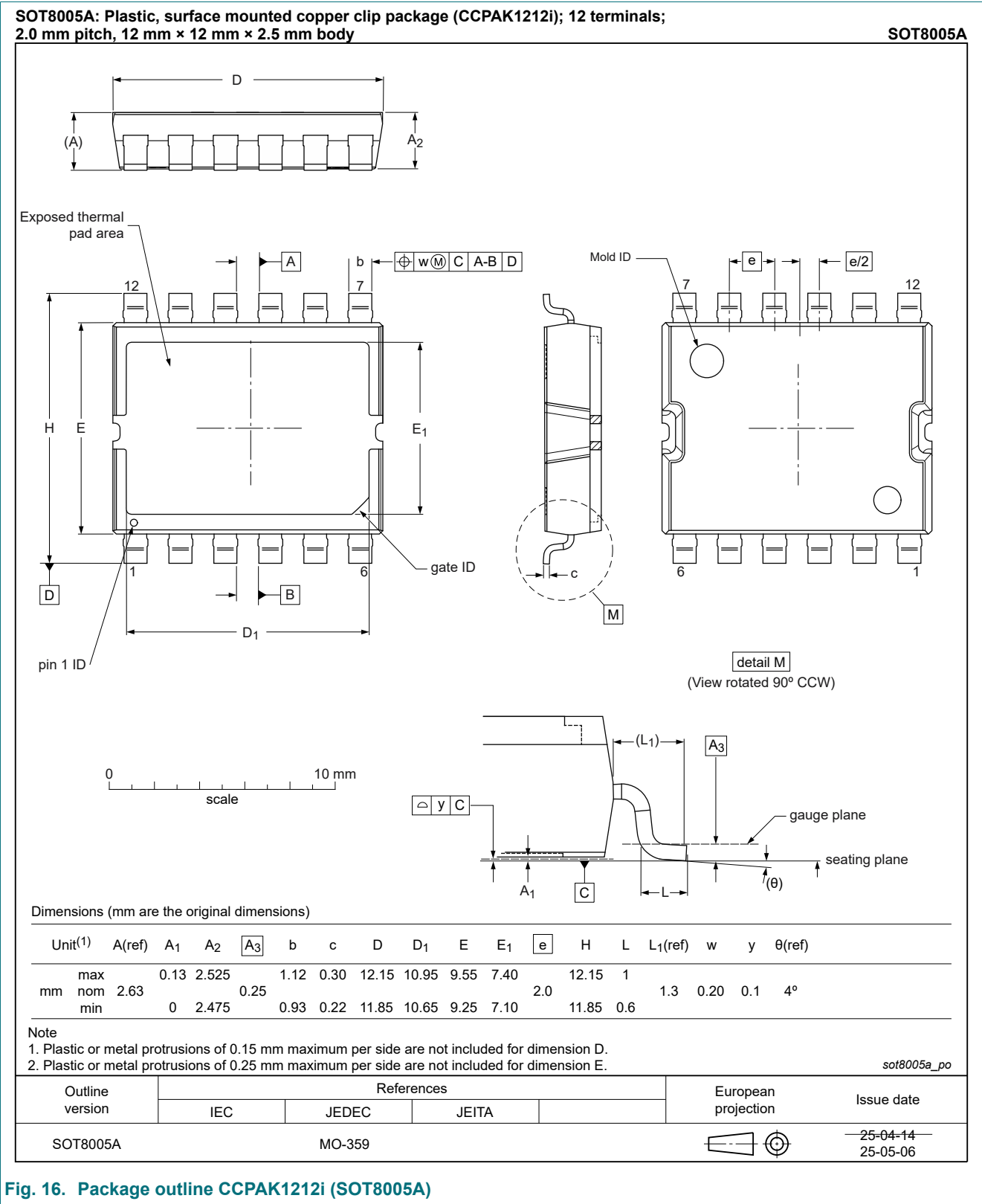


Fig. 16. Package outline CCPAK1212i (SOT8005A)

12. Soldering

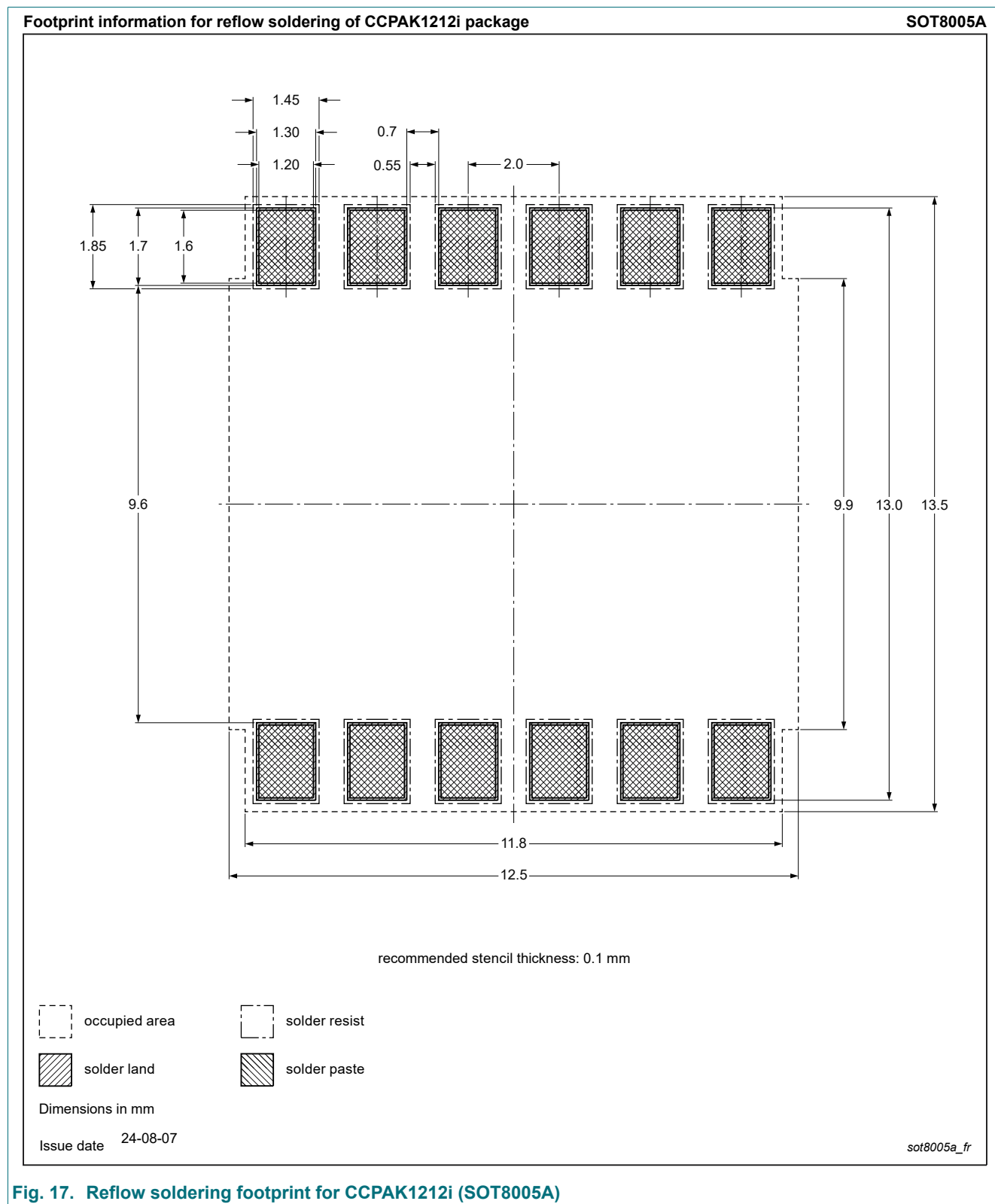


Fig. 17. Reflow soldering footprint for CCPAK1212i (SOT8005A)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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