



# BUK7Y3R5-40H

N-channel 40 V, 3.5 mΩ standard level MOSFET in LFPAK56

8 May 2018

Product data sheet

## 1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower  $R_{DSon}$  in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight  $V_{GS(th)}$  limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced  $R_{th}$  and  $R_{DSon}$
  - Increases maximum current capability and improved current spreading

## 3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

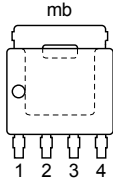
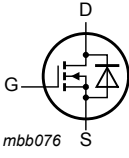
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	[1]	-	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>		-	-	115	W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>	2	2.9	3.5	mΩ
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	6	15	nC
<b>Source-drain diode</b>						
Q <sub>r</sub>	recovered charge	I <sub>S</sub> = 25 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; <a href="#">Fig. 17</a>	-	16	-	nC
S	softness factor	I <sub>S</sub> = 25 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>J</sub> = 25 °C	-	0.8	-	

[1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y3R5-40H	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y3R5-40H	73H540

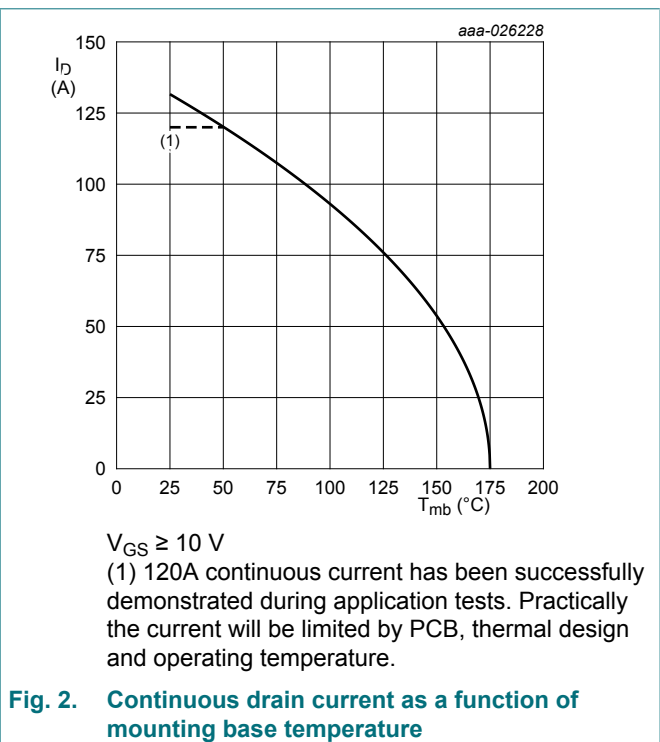
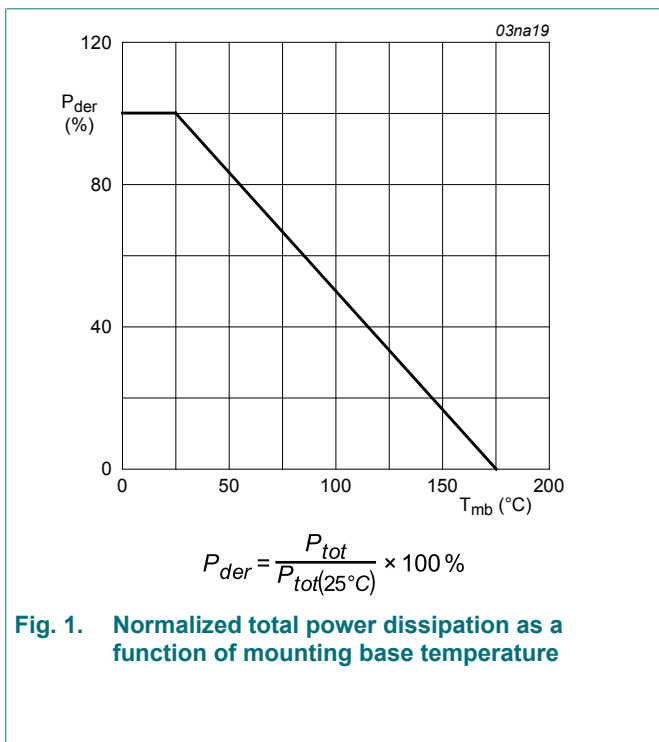
## 8. Limiting values

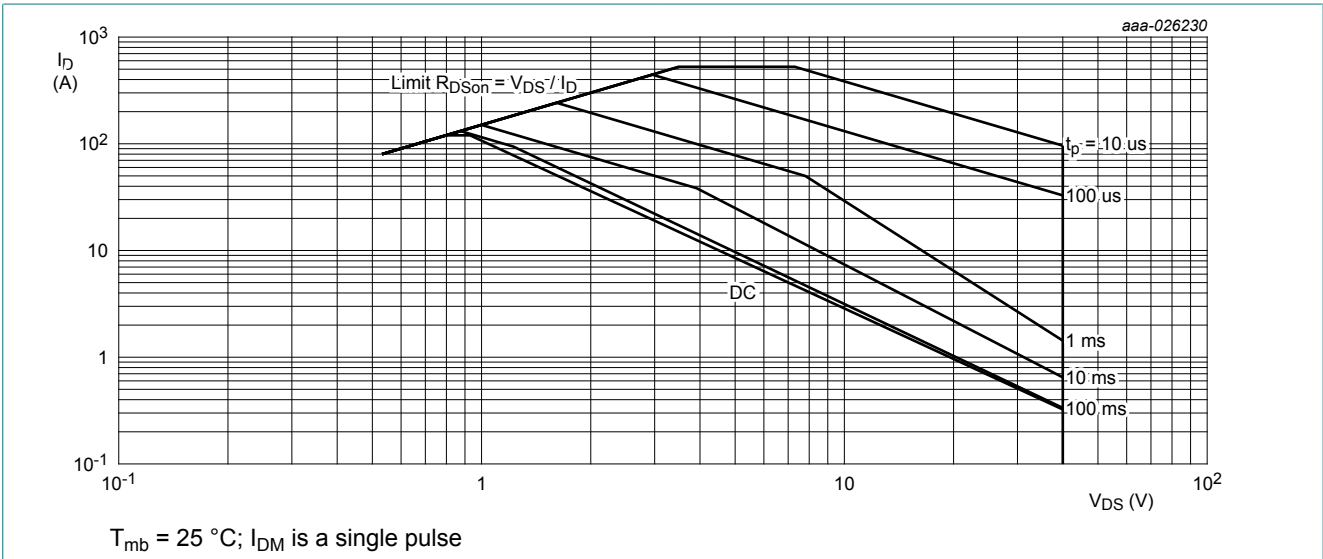
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

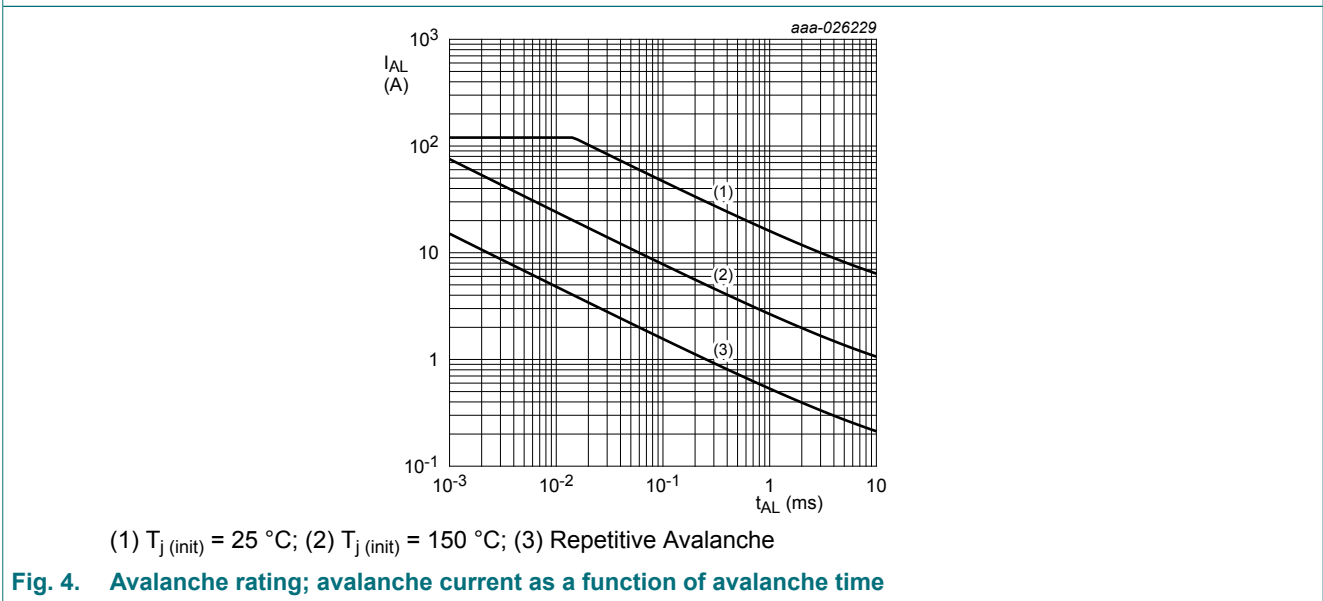
Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	115	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	[1]	-	120	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 2</a>	[1]	-	93	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>		-	526	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	120	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	526	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; <a href="#">Fig. 4</a>	[2] [3]	-	45	mJ

- [1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.





**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

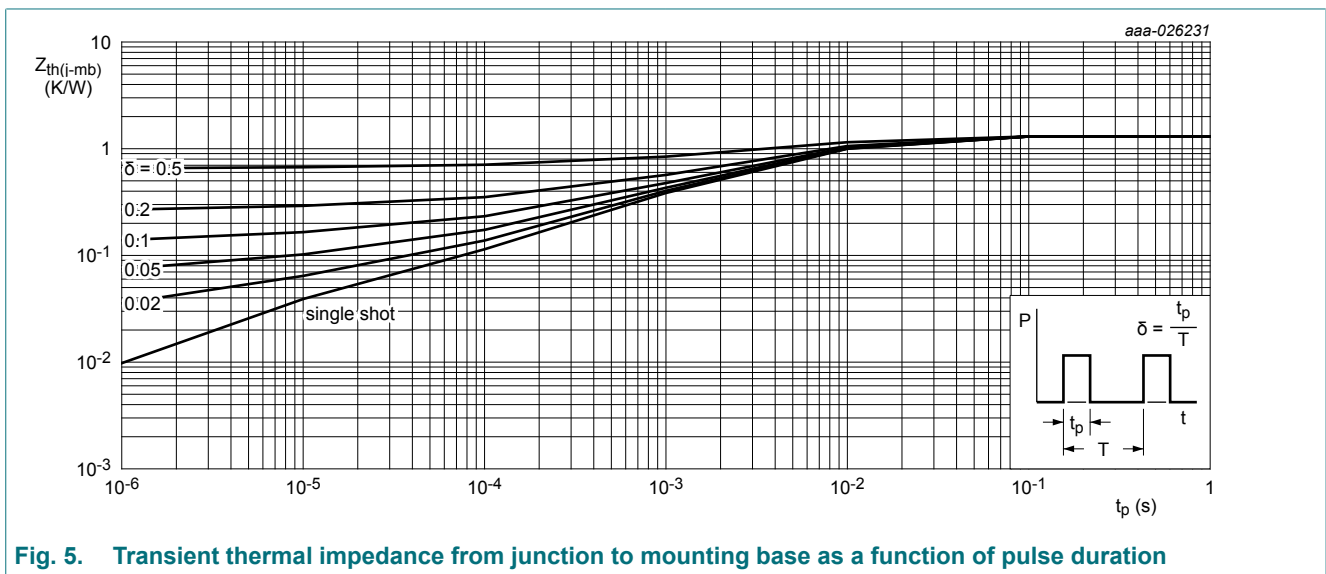


**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	1.18	1.3	K/W



**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 10. Characteristics

**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	42.7	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	40.1	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	39.7	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}; \text{ Fig. 10}$	2.4	3	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 9}$	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 9}$	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.03	1	$\mu A$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1	10	$\mu A$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	37	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

## N-channel 40 V, 3.5 mΩ standard level MOSFET in LPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>	2	2.9	3.5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 105 °C; <a href="#">Fig. 12</a>	2.7	4.1	5.2	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 125 °C; <a href="#">Fig. 12</a>	2.9	4.5	5.6	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 12</a>	3.4	5.4	6.7	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C	0.32	0.8	2	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	31	53	nC
Q <sub>GS</sub>	gate-source charge		-	10	15	nC
Q <sub>GD</sub>	gate-drain charge		-	6	15	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>J</sub> = 25 °C; <a href="#">Fig. 15</a>	-	2294	3441	pF
C <sub>oss</sub>	output capacitance		-	682	954	pF
C <sub>rss</sub>	reverse transfer capacitance		-	112	247	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω	-	10	-	ns
t <sub>r</sub>	rise time		-	8	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	19	-	ns
t <sub>f</sub>	fall time		-	9	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 16</a>	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; <a href="#">Fig. 17</a>	-	25	-	ns
Q <sub>r</sub>	recovered charge		-	16	-	nC
S	softness factor	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>J</sub> = 25 °C	-	0.8	-	
		I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -500 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.6	-	

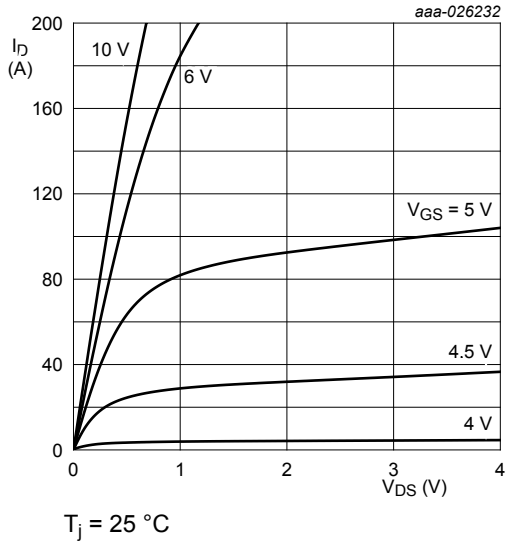


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

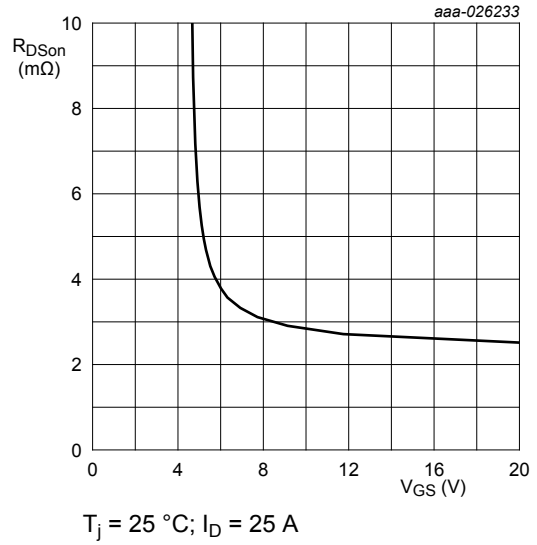


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

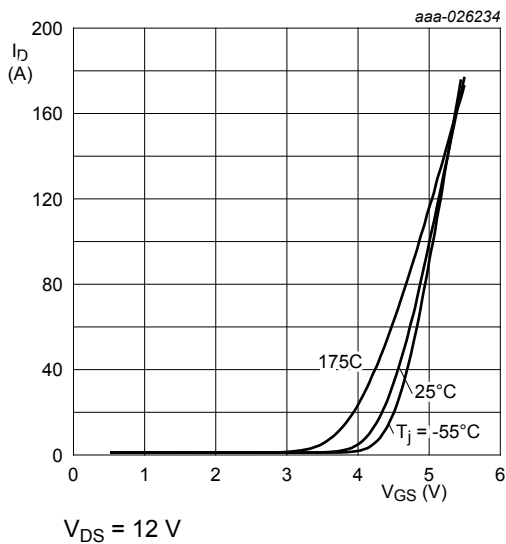


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

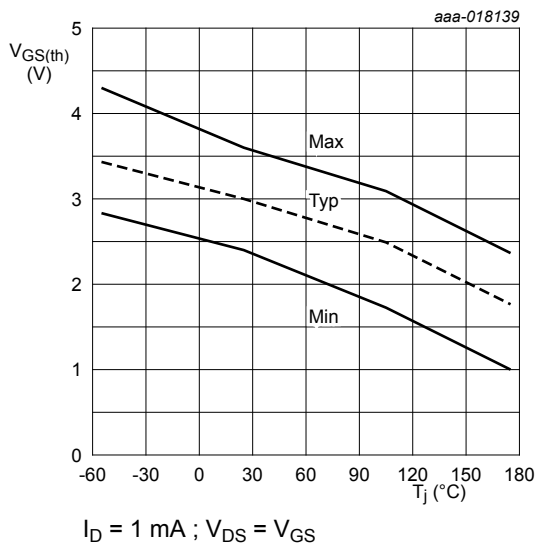


Fig. 9. Gate-source threshold voltage as a function of junction temperature

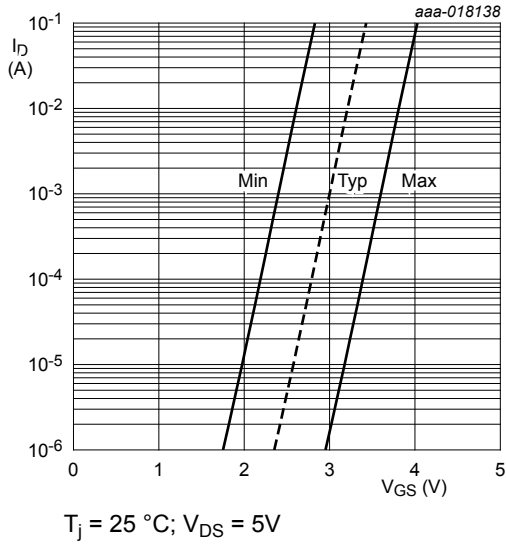


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

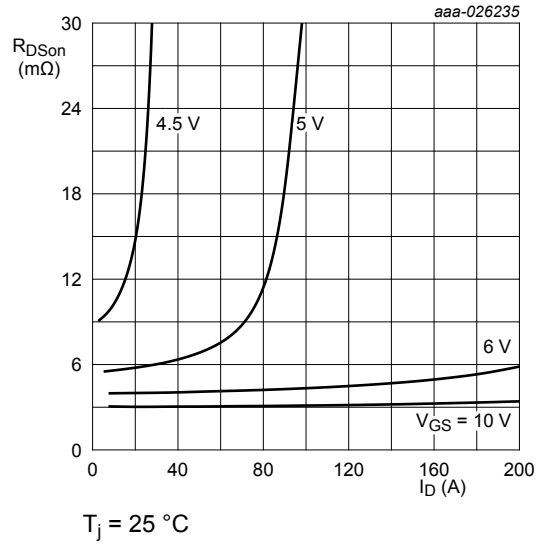


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

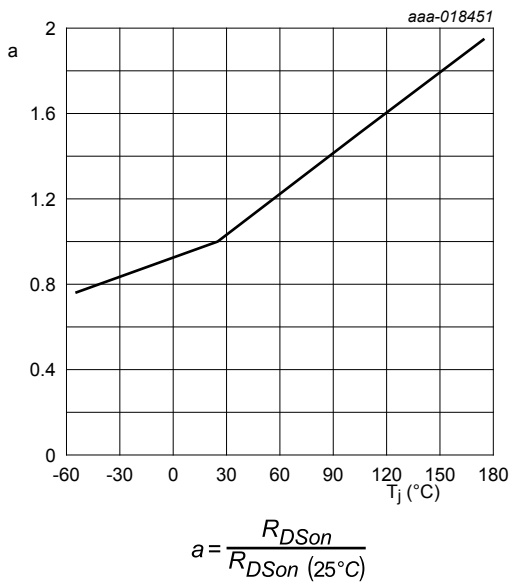


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

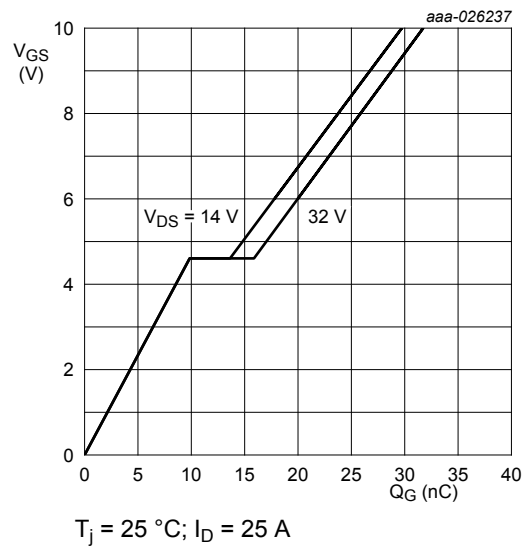
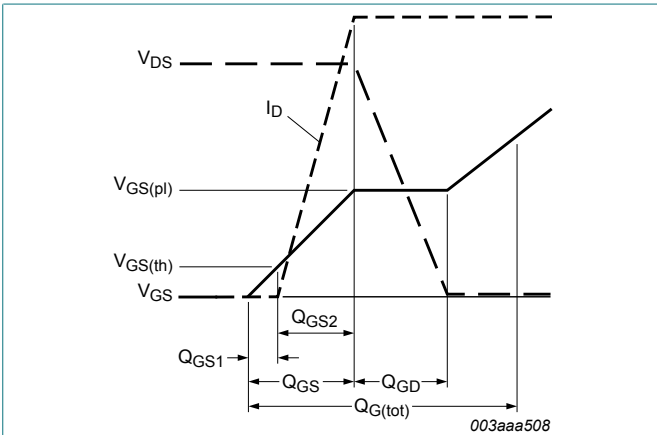
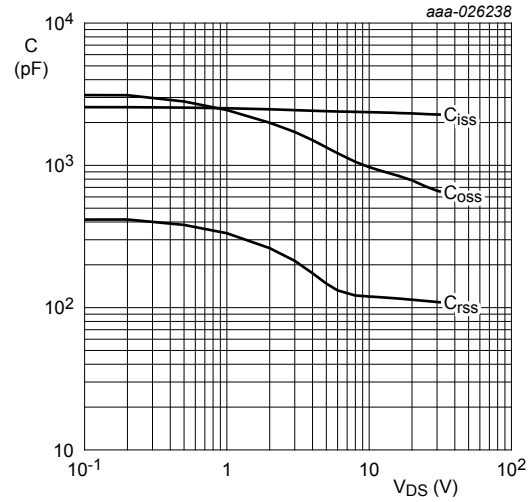


Fig. 13. Gate-source voltage as a function of gate charge; typical values



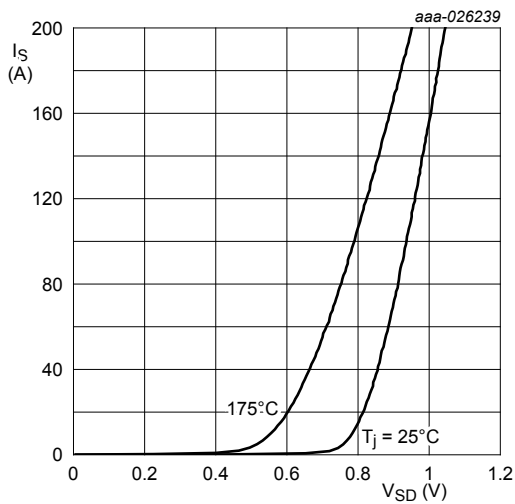


**Fig. 14. Gate charge waveform definitions**



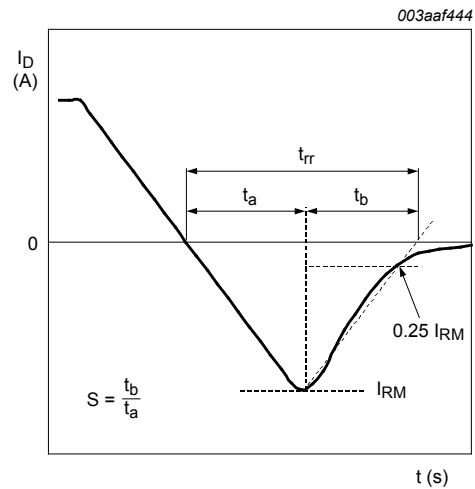
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$V_{GS} = 0 \text{ V}$

**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

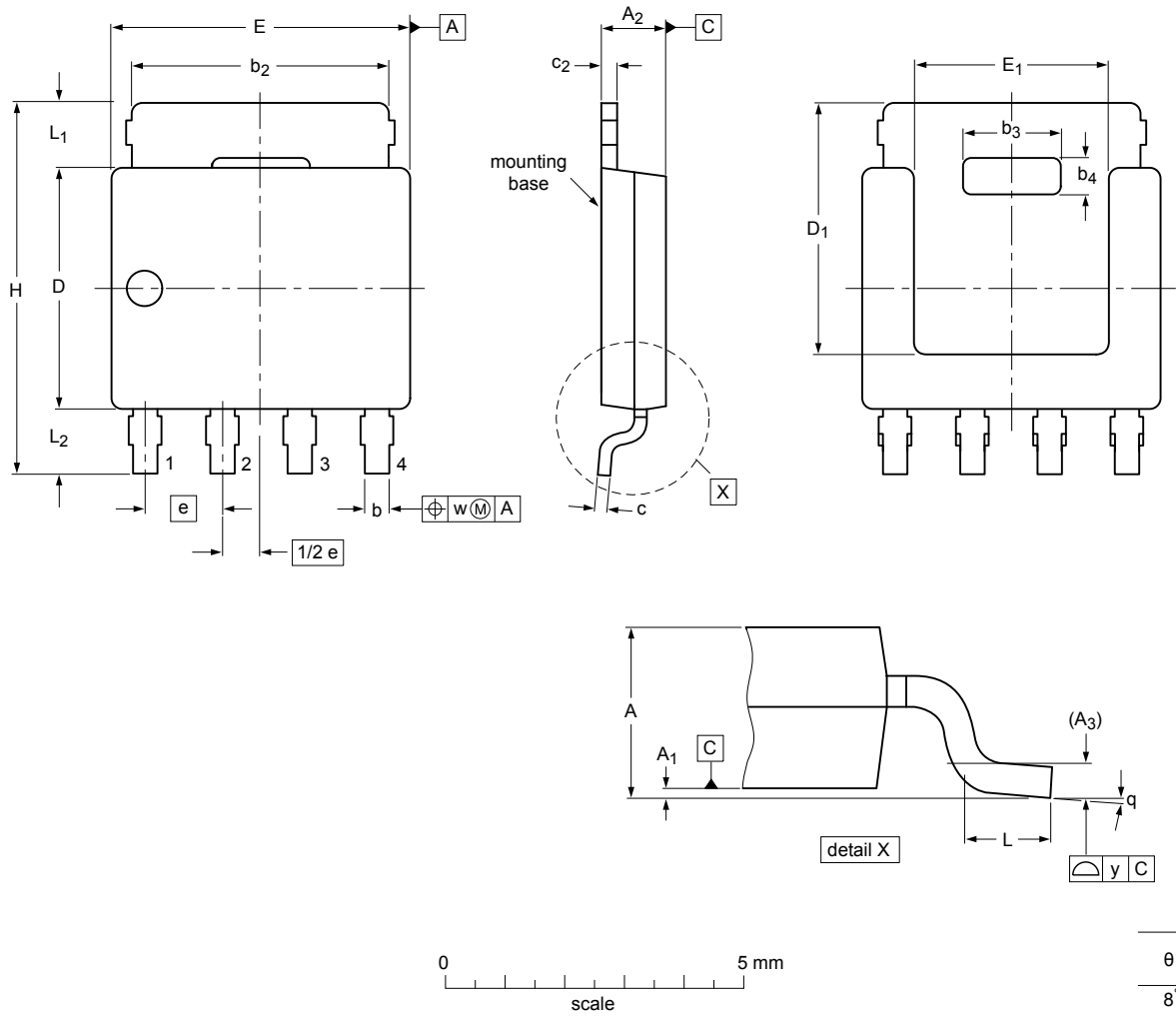


$$t_{rr} = t_a + t_b$$

**Fig. 17. Reverse recovery waveform definitions**

### 11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3	1.27	6.2	0.85	1.3	1.3		
nom				0.25																0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT669		MO-235			-11-03-25- 13-02-27

Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Soldering

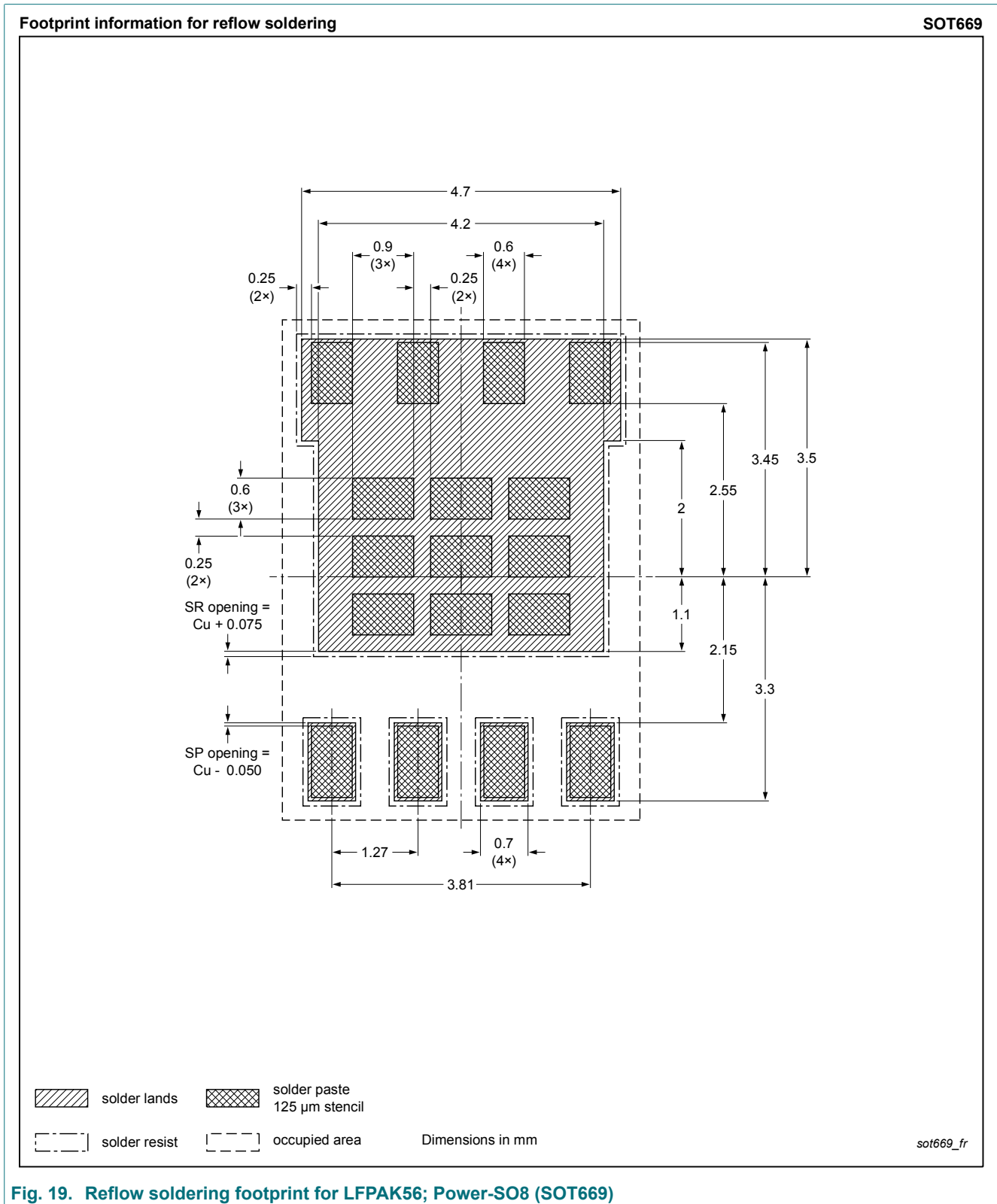
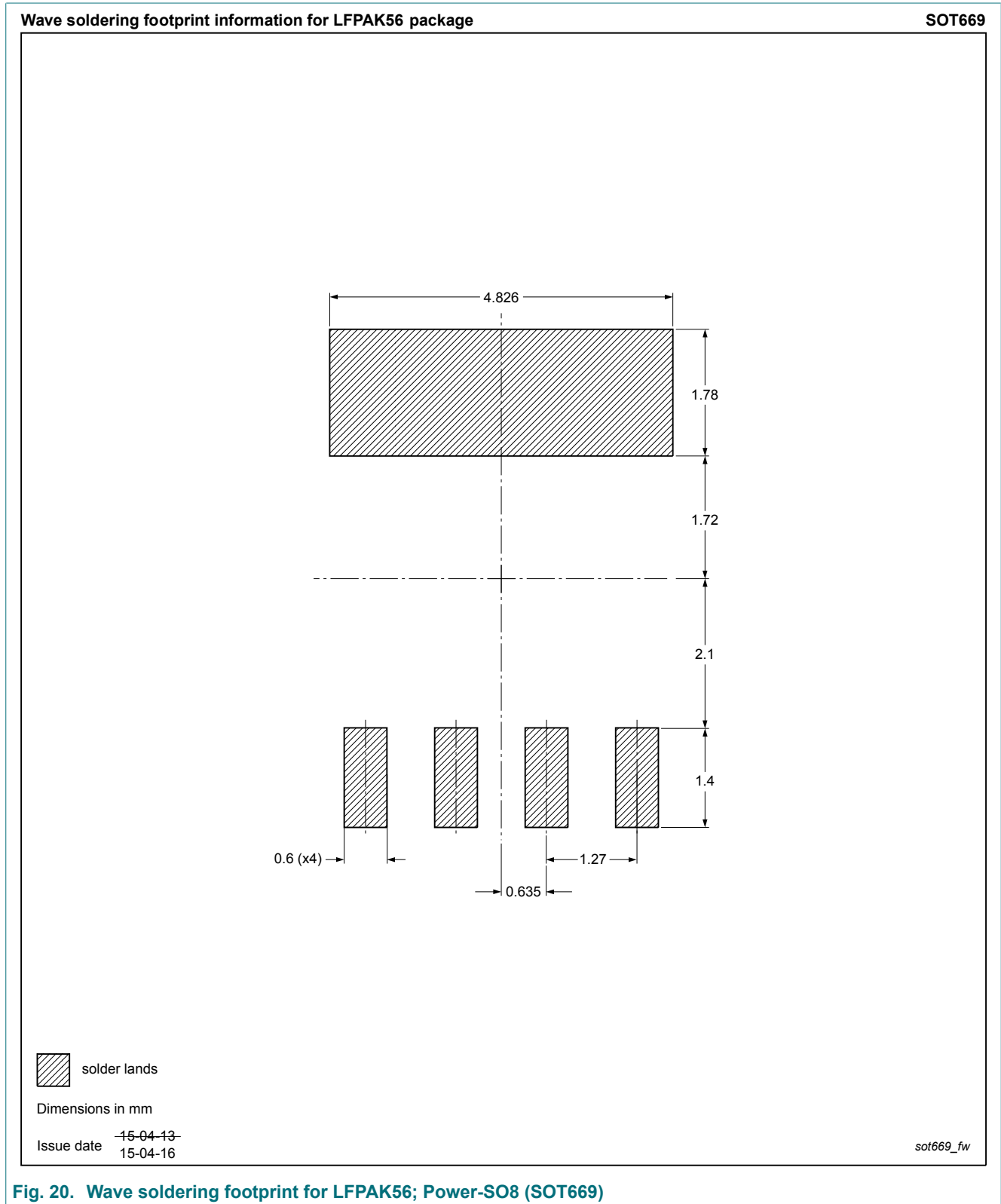


Fig. 19. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)



## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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