

# BUK9107-55ATE

## N-channel TrenchPLUS logic level FET

Rev. 02 — 16 February 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. The devices include TrenchPLUS diodes for ElectroStatic Discharge (ESD) protection and temperature sensing. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Allows responsive temperature monitoring due to integrated temperature sensor
- Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

### 1.3 Applications

- 12 V and 24 V high power motor drives
- Automotive and general purpose power switching
- Electrical Power Assisted Steering (EPAS)
- Protected drive for lamps

### 1.4 Quick reference data

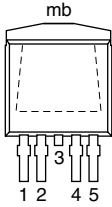
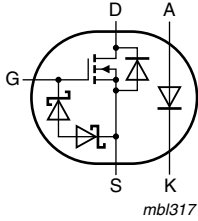
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	55	V
$I_D$	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a> and <a href="#">3</a>	[1]	-	140	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a>	-	-	272	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 50\text{ A}; T_j = 25\text{ °C}$	-	6	7.7	mΩ
		$V_{GS} = 10\text{ V}; I_D = 50\text{ A}; T_j = 25\text{ °C}$	-	5.2	6.2	mΩ
		$V_{GS} = 5\text{ V}; I_D = 50\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 7</a> and <a href="#">8</a>	-	5.8	7	mΩ
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250\text{ }\mu\text{A}; T_j > -55\text{ °C}; T_j < 175\text{ °C}$	-1.4	-1.54	-1.68	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250\text{ }\mu\text{A}; T_j = 25\text{ °C}$	648	658	668	mV

[1] Current is limited by power dissipation chip rating.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT426 (D2PAK)</b></p>	 <p><i>mb1317</i></p>
2	A	anode		
3	D	drain		
4	K	cathode		
5	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK9107-55ATE	D2PAK	plastic single-ended surface-mounted package (D2PAK); 5 leads (one lead cropped)	SOT426

## 4. Limiting values

**Table 4. Limiting values**

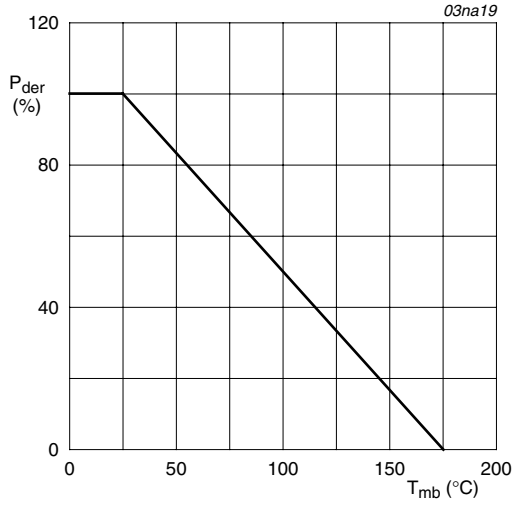
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	55	V	
$V_{GS}$	gate-source voltage	[1]	-15	15	V	
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ see <a href="#">Figure 2</a> ;	[2]	-	140	A
		see <a href="#">Figure 3</a>	[3]	-	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ see <a href="#">Figure 2</a>	[3]	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s};$ pulsed; see <a href="#">Figure 3</a>	-	560	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a>	-	272	W	
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA	
		pulsed; $t_p = 5\text{ ms}; \delta = 0.01$	-	50	mA	
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-100	100	V	
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
$V_{DGS}$	drain-gate voltage		-	55	V	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[2]	-	140	A
			[3]	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C}$	-	560	A	
<b>Clamping</b>						
$E_{DS(CL)S}$	non-repetitive drain-source clamping energy	$I_D = 75\text{ A}; V_{DS} \leq 55\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ unclamped; $T_{j(init)} = 25\text{ °C}$	-	500	mJ	
<b>Electrostatic discharge</b>						
$V_{esd}$	electrostatic discharge voltage	HBM; $C = 100\text{ pF}; R = 1.5\text{ k}\Omega;$ pins 1, 3, 5	-	6	kV	

[1] Voltage is limited by clamping.

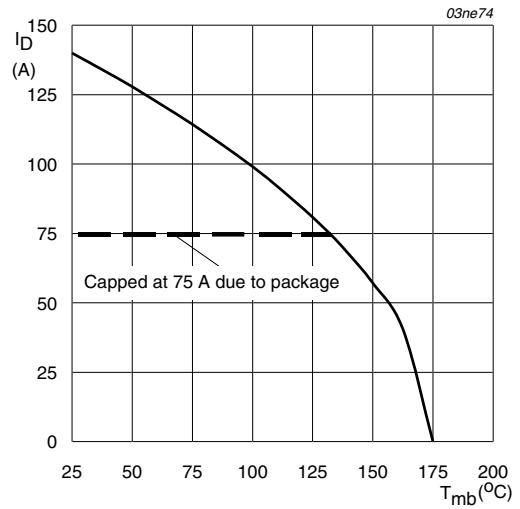
[2] Current is limited by power dissipation chip rating.

[3] Continuous current is limited by package.



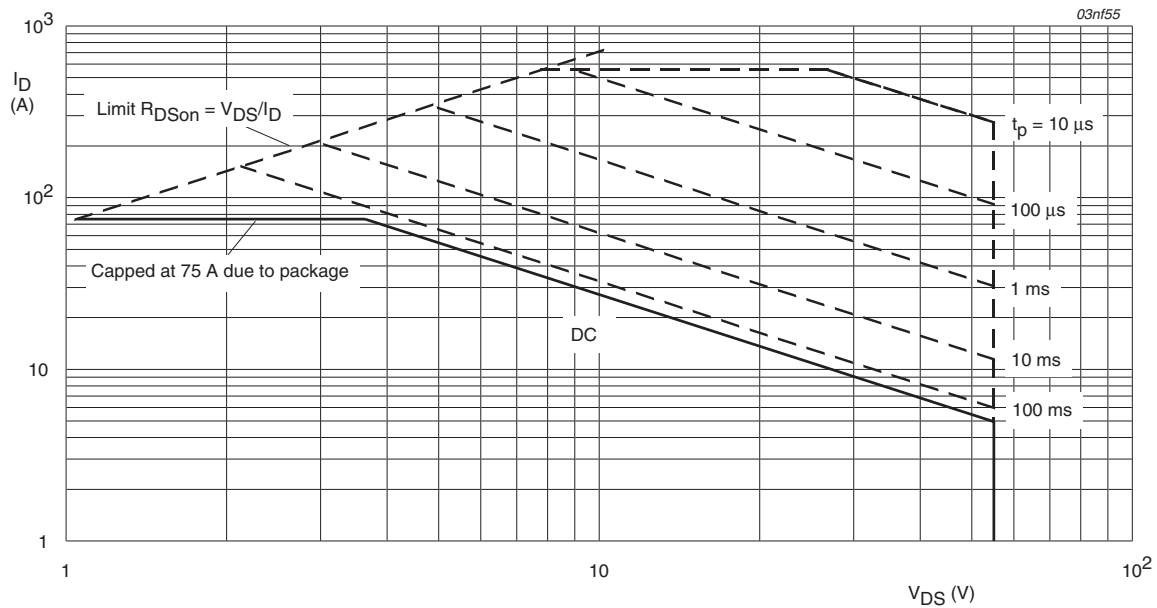
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature**



$V_{GS} \geq 5V$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature**



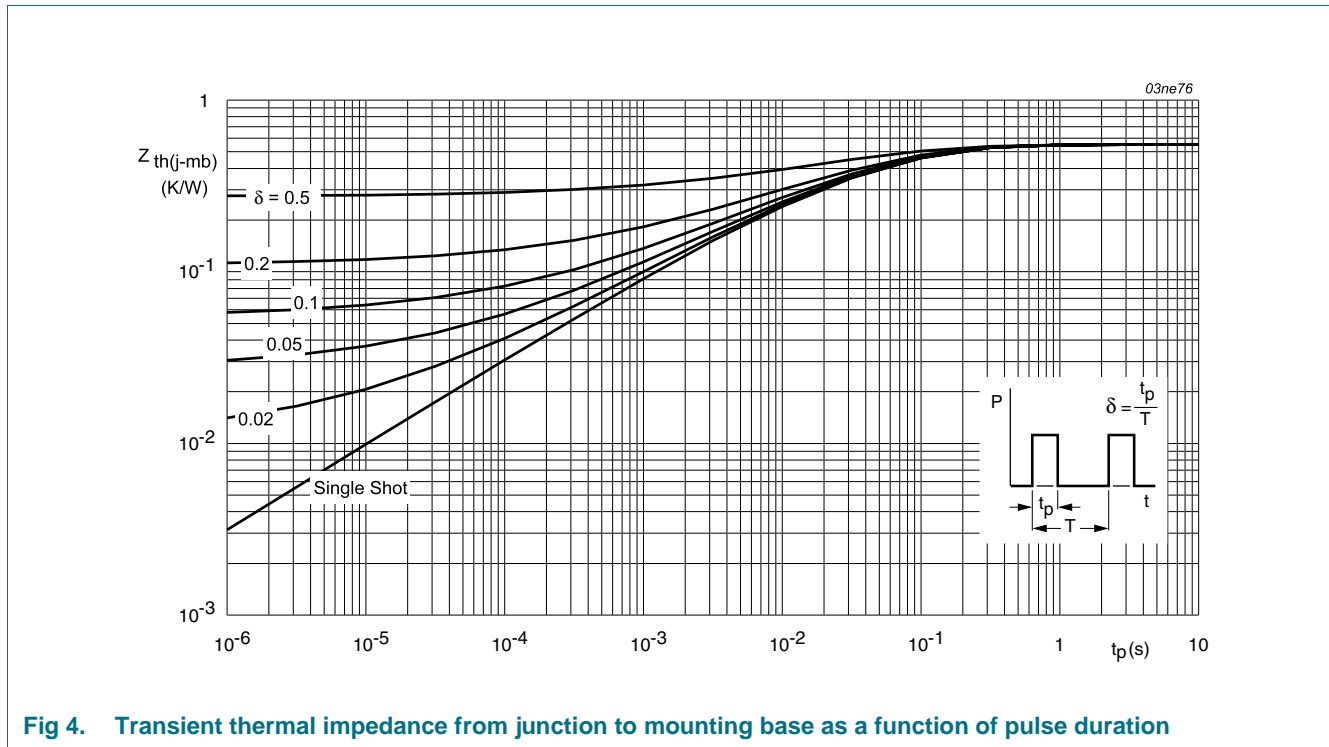
$T_{mb} = 25^\circ C; I_{DM}$  is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board; minimum footprint	-	-	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.55	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

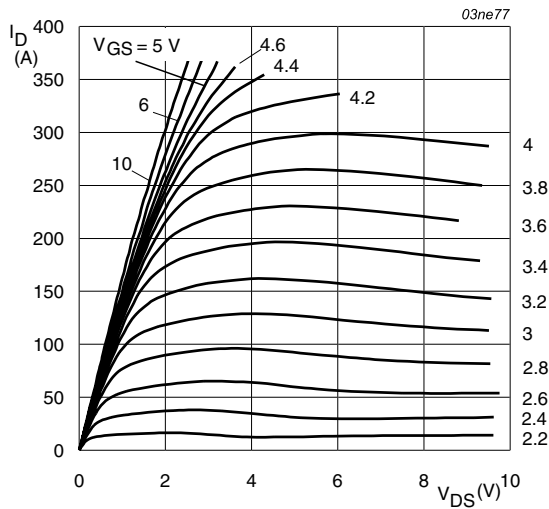
## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	-	-	2.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.1	10	$\mu\text{A}$
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	250	$\mu\text{A}$
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = -1 \text{ mA}; -55 \text{ }^\circ\text{C} < T_j < 175 \text{ }^\circ\text{C}$	12	15	-	V
		$I_G = 1 \text{ mA}; -55 \text{ }^\circ\text{C} < T_j < 175 \text{ }^\circ\text{C}$	12	15	-	V
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	1000	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	1000	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 50 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	5.8	7	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 50 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	14	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 50 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	6	7.7	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 50 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	5.2	6.2	m $\Omega$
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250 \text{ } \mu\text{A}; T_j = 25 \text{ }^\circ\text{C}$	648	658	668	mV
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250 \text{ } \mu\text{A}; T_j > -55 \text{ }^\circ\text{C}; T_j < 175 \text{ }^\circ\text{C}$	-1.4	-1.54	-1.68	mV/K
$V_{F(TSD)hys}$	temperature sense diode forward voltage hysteresis	$I_F > 125 \text{ } \mu\text{A}; I_F < 250 \text{ } \mu\text{A}; T_j = 25 \text{ }^\circ\text{C}$	25	32	50	mV
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 50 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	108	-	nC
$Q_{GS}$	gate-source charge		-	15	-	nC
$Q_{GD}$	gate-drain charge		-	47	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	5836	-	pF
$C_{oss}$	output capacitance		-	958	-	pF
$C_{rss}$	reverse transfer capacitance		-	595	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	51	-	ns
$t_r$	rise time		-	202	-	ns
$t_{d(off)}$	turn-off delay time		-	341	-	ns
$t_f$	fall time		-	207	-	ns

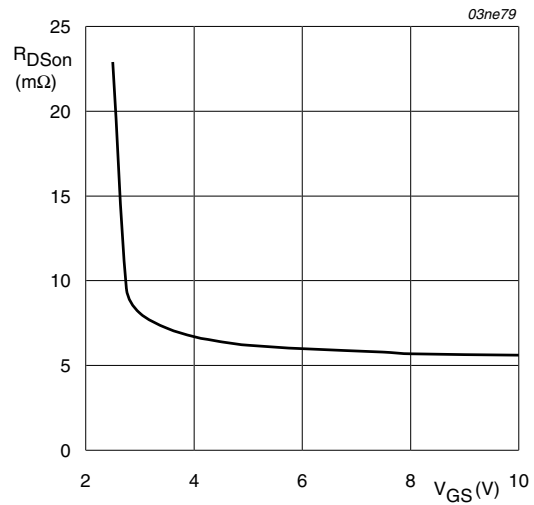
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$L_D$	internal drain inductance	from upper edge of drain mounting base to centre of die; $T_j = 25\text{ °C}$	-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad; $T_j = 25\text{ °C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = -10\text{ V}$ ;	-	85	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ °C}$	-	250	-	nC



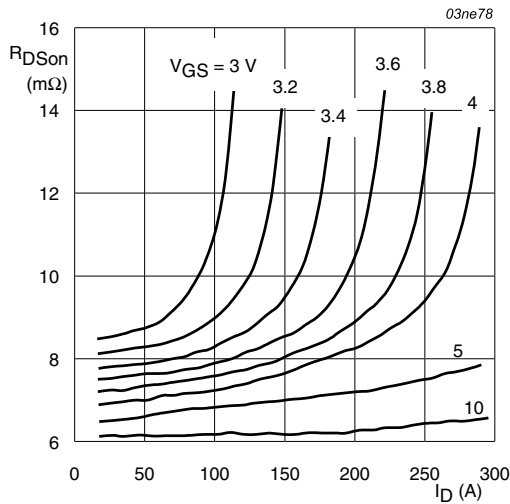
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



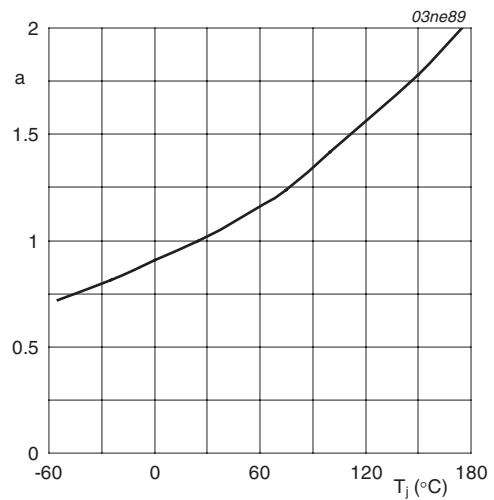
$T_j = 25^\circ\text{C}; I_D = 50\text{A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

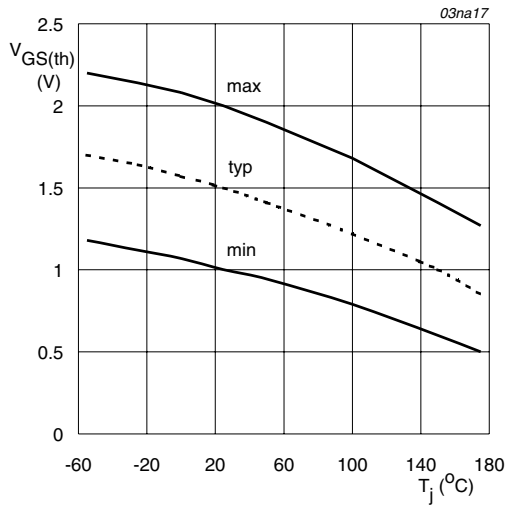
**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

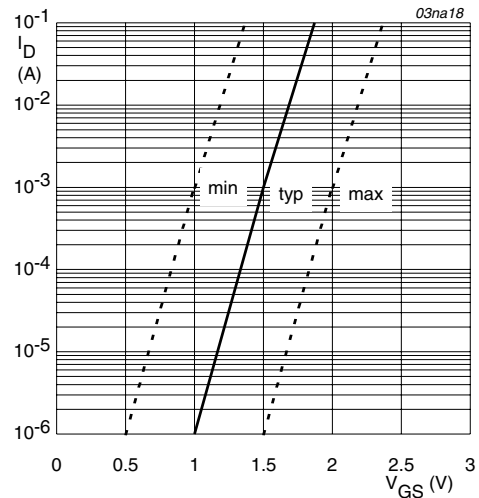
**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**





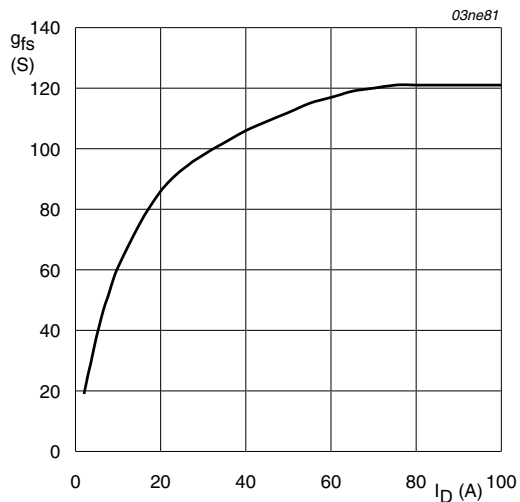
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



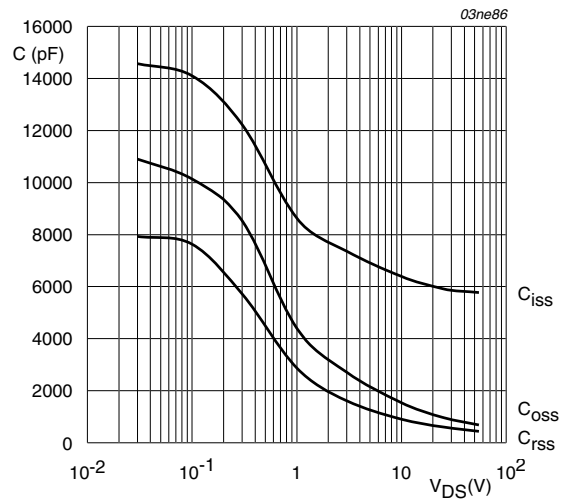
$$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



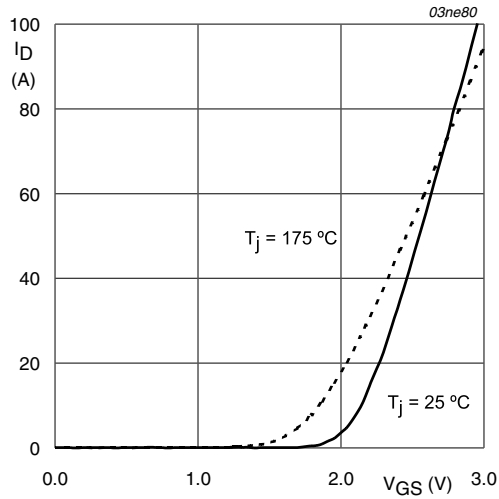
$$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$$

**Fig 11. Forward transconductance as a function of drain current; typical values**



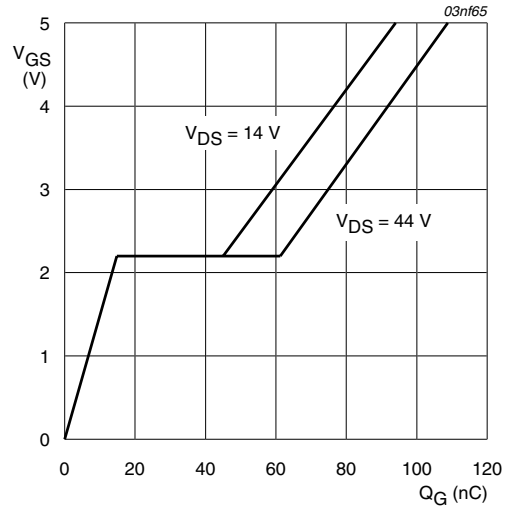
$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



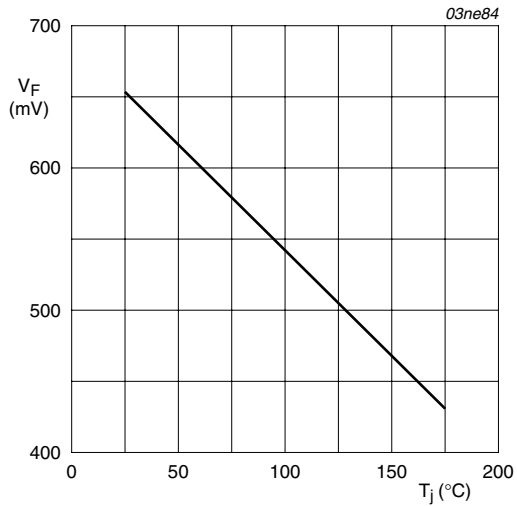
$V_{DS} = 25V$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



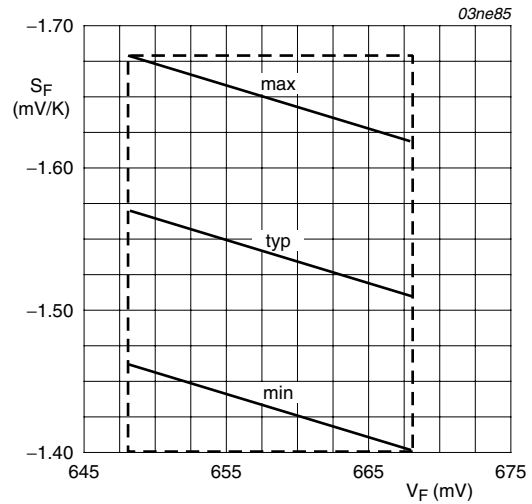
$T_j = 25^{\circ}C; I_D = 50A$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



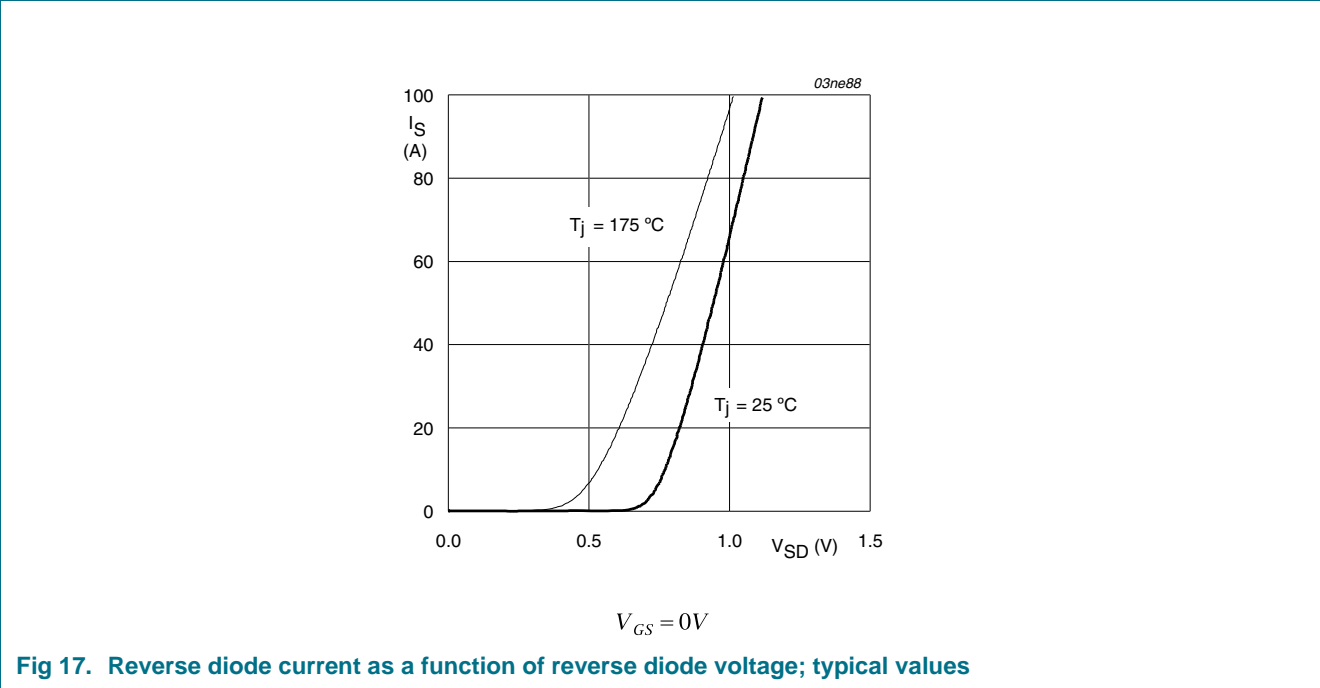
$I_F = 250\mu A$

**Fig 15. Forward voltage of temperature sense diode as a function of junction temperature; typical values**



$V_F$  at  $T_j = 25^{\circ}C; I_F = 250\mu A$

**Fig 16. Temperature coefficient of temperature sense diode as a function of forward voltage; typical values**



**Fig 17. Reverse diode current as a function of reverse diode voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 5 leads (one lead cropped)

SOT426

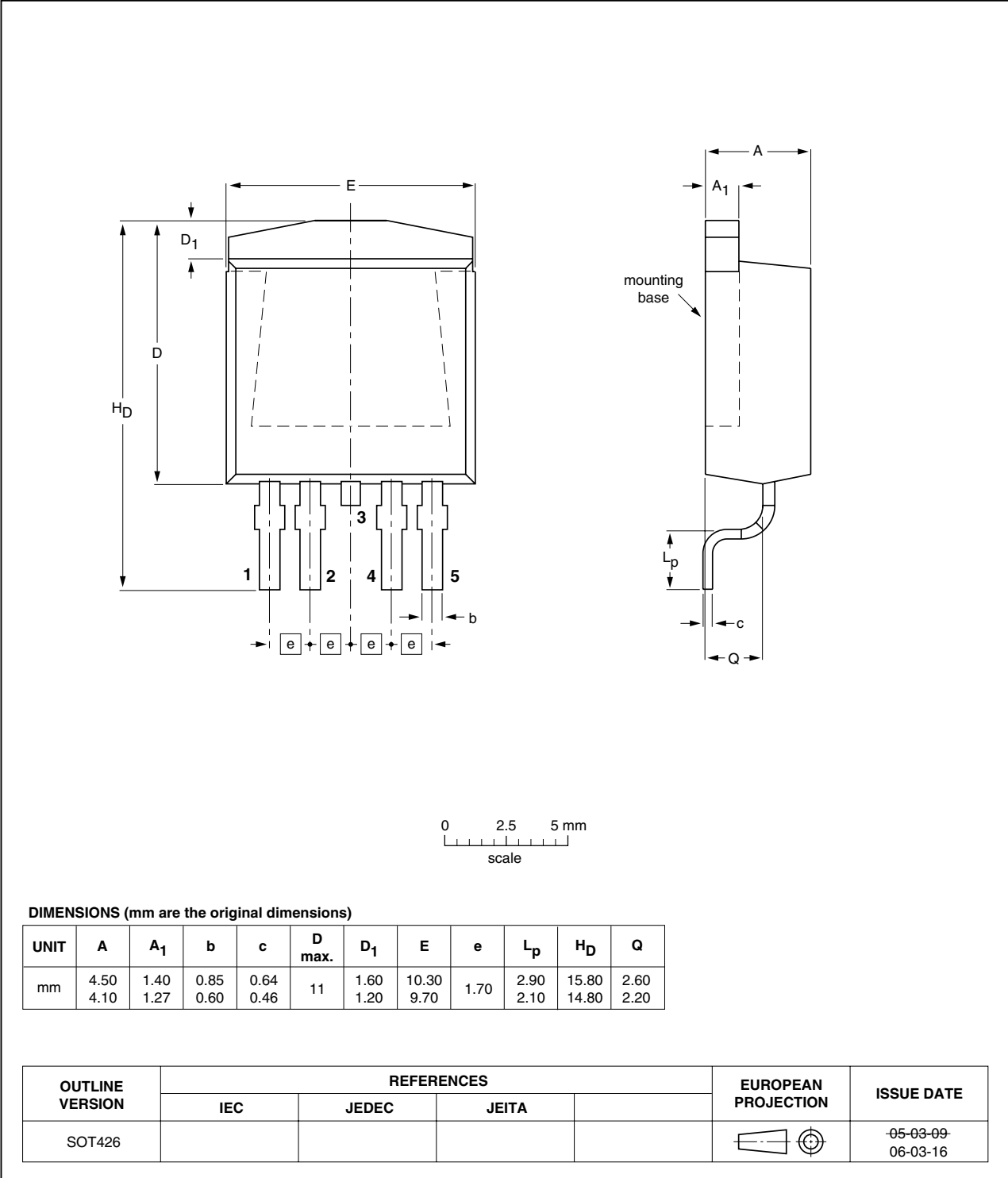


Fig 18. Package outline SOT426 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9107-55ATE_2	20090216	Product data sheet	-	BUK9107_9907_55ATE-01
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number BUK9107-55ATE separated from data sheet BUK9107_9907_55ATE-01.</li></ul>		
BUK9107_9907_55ATE-01 (9397 750 09138)	20020207	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 9.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 9.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**TrenchMOS** — is a trademark of NXP B.V.

## 10. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 11. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>3</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>5</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>6</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>12</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>13</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>14</b>
9.1	Data sheet status . . . . .	14
9.2	Definitions . . . . .	14
9.3	Disclaimers . . . . .	14
9.4	Trademarks . . . . .	14
<b>10</b>	<b>Contact information</b> . . . . .	<b>14</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: Rev. 02 — 16 February 2009

Document identifier: BUK9107-55ATE\_2