

BUK92150-55A

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TrenchMOS™ logic level FET

Rev. 03 — 30 May 2002

Product data

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance.

Product availability:

BUK92150-55A in SOT428 (D-PAK).

2. Features

- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching:
 - ◆ 12 V and 24 V loads
 - ◆ Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MBK091</p> <p>SOT428 (D-PAK)</p>	<p>MBB076</p>
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	-	11	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	36	W
T_j	junction temperature		-	175	°C
R_{DSon}	drain-source on-state resistance	$T_j = 25\text{ °C}; V_{GS} = 5\text{ V}; I_D = 5\text{ A}$	120	140	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 4.5\text{ V}; I_D = 5\text{ A}$	-	155	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 10\text{ V}; I_D = 5\text{ A}$	97	125	mΩ
		$T_j = 175\text{ °C}; V_{GS} = 5\text{ V}; I_D = 5\text{ A}$	-	280	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

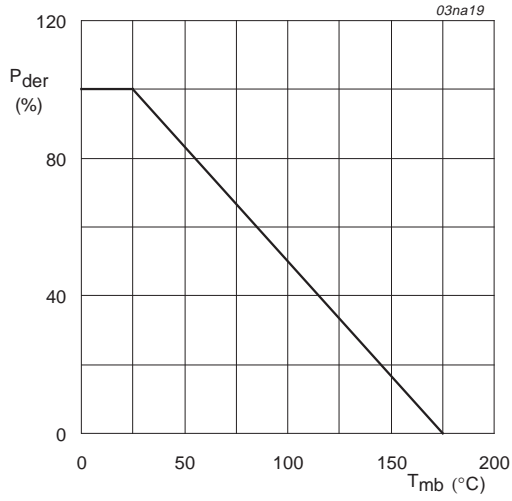
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage (DC)		-	±15	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2 and 3	-	11	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2	-	7.8	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	44	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	36	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C

Source-drain diode

I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	-	11	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	44	A

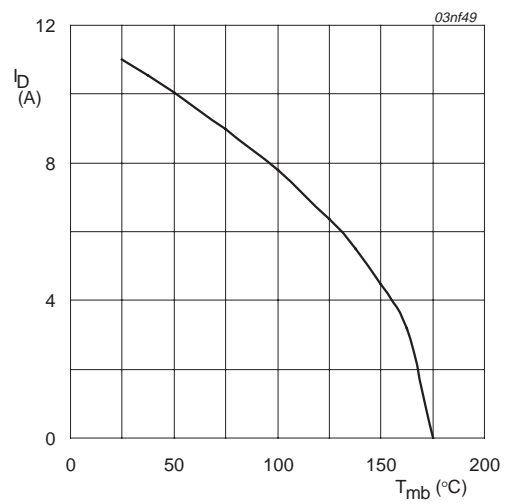
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 11\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_j = 25\text{ °C}$	-	16	mJ
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

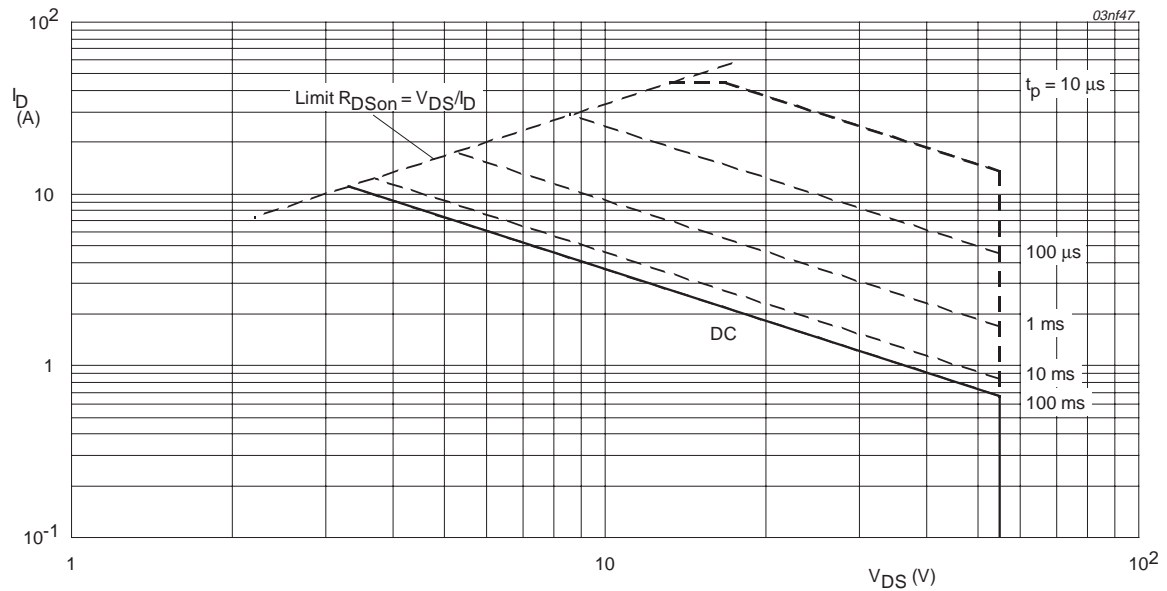
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 4.5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	71.4	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	4.1	K/W

7.1 Transient thermal impedance

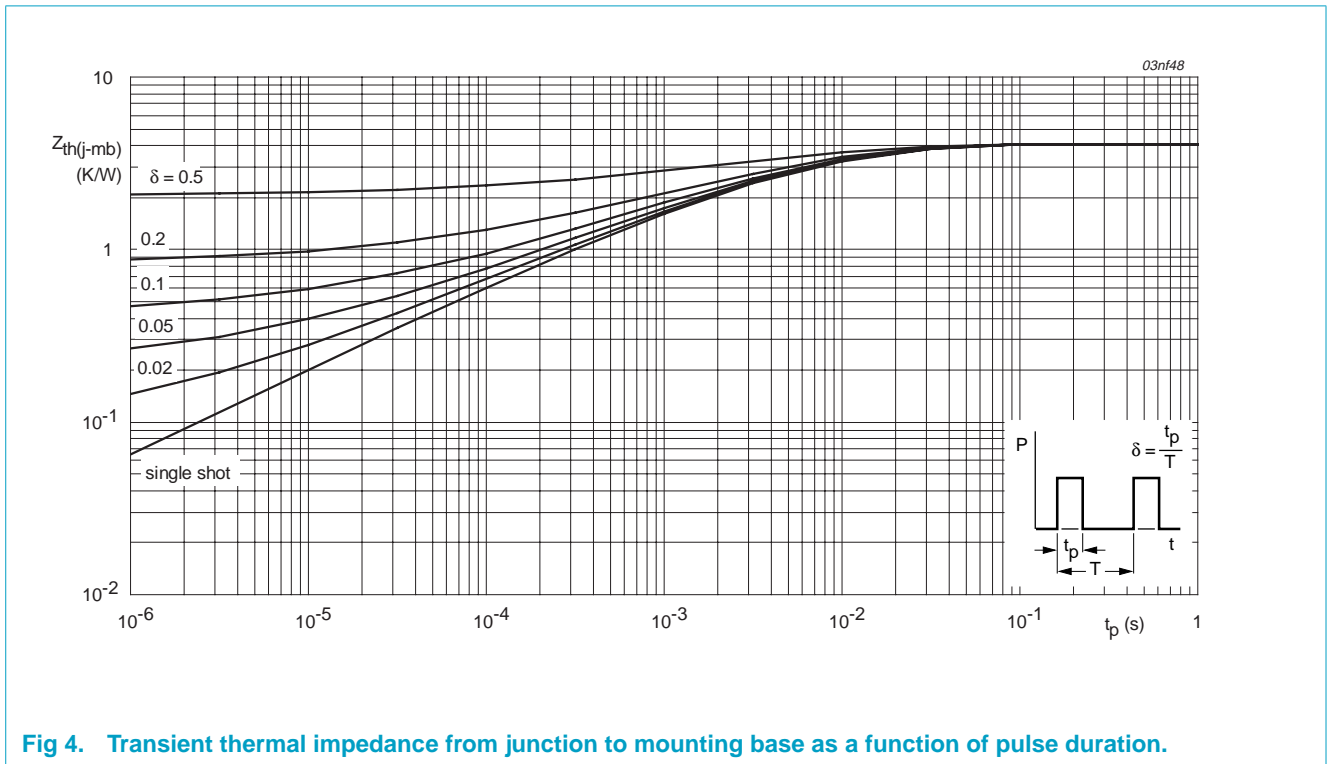


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

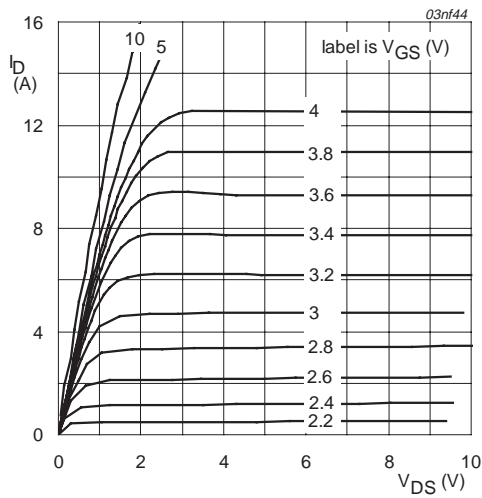
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.05	10	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	120	140	m Ω
		$T_j = 175\text{ °C}$	-	-	280	m Ω
		$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A};$	-	-	155	m Ω
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A};$	-	97	125	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 5\text{ V}; V_{DD} = 44\text{ V};$	-	6	-	nC
Q_{gs}	gate-to-source charge	$I_D = 5\text{ A};$ Figure 14	-	0.72	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	2.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$	-	240	338	pF
C_{oss}	output capacitance	$f = 1\text{ MHz};$ Figure 12	-	50	65	pF
C_{rss}	reverse transfer capacitance		-	40	58	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 20\text{ V}; R_L = 3.3\text{ }\Omega;$	-	8	-	ns
t_r	rise time	$V_{GS} = 5\text{ V}; R_G = 10\text{ }\Omega;$	-	57	-	ns
$t_{d(off)}$	turn-off delay time		-	16	-	ns
t_f	fall time		-	13	-	ns
L_d	internal drain inductance	measured from drain to centre of die	-	2.5	-	nH
L_s	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH

Table 5: Characteristics...continued

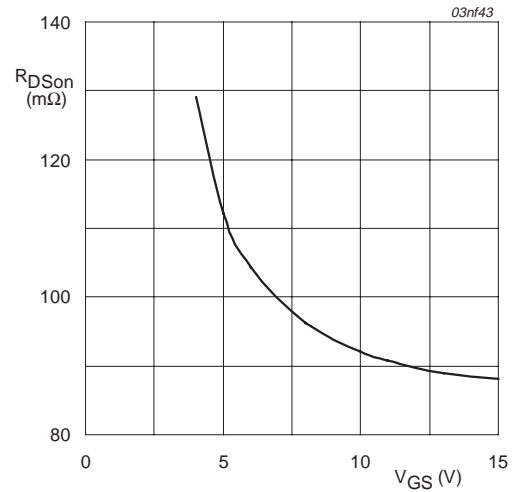
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 15\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$	-	24	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$	-	26	-	nC



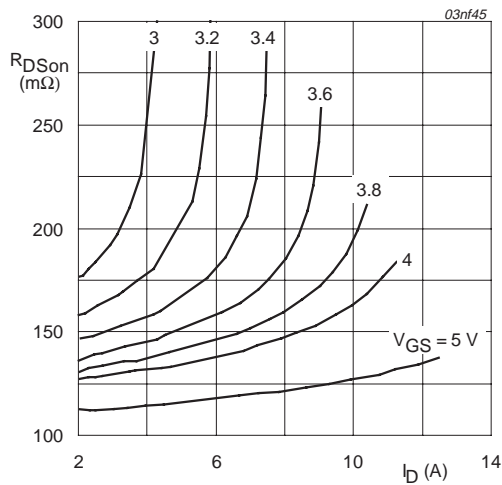
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



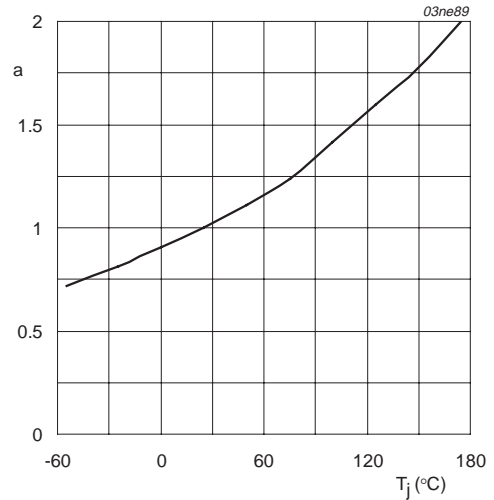
$T_j = 25\text{ }^\circ\text{C}; I_D = 5\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



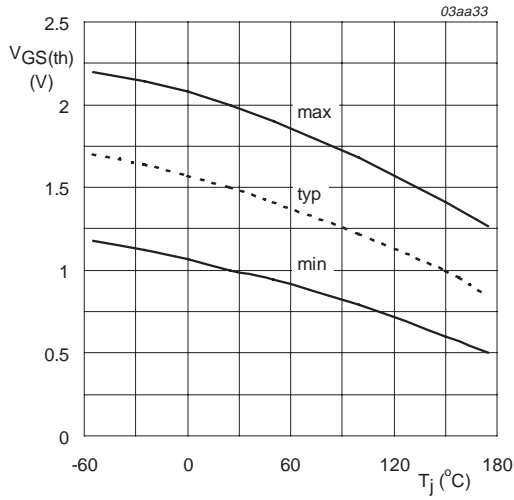
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



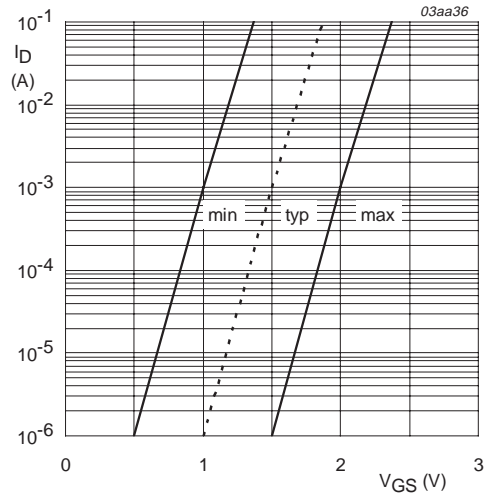
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



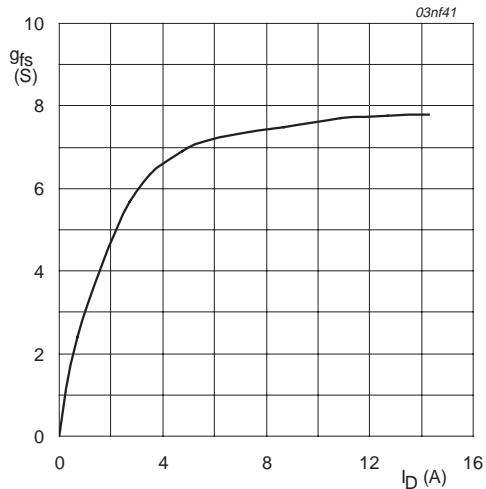
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



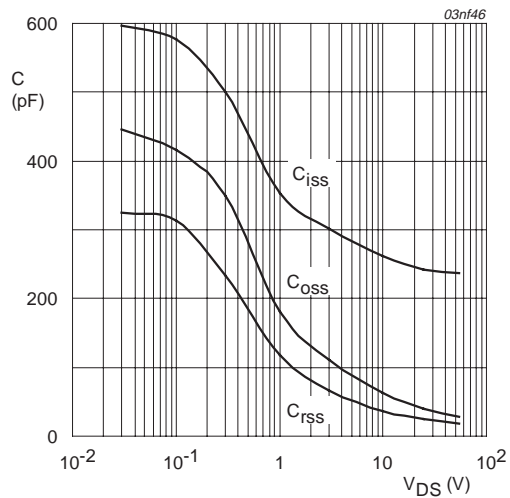
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



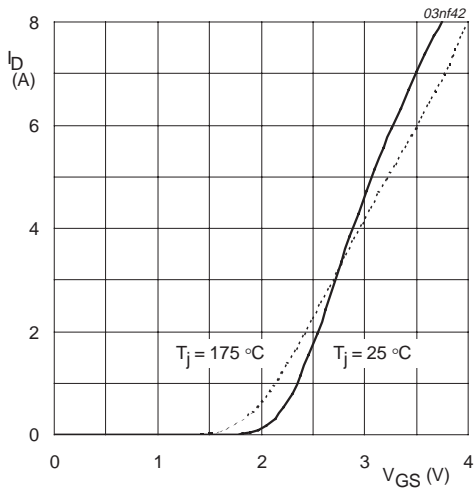
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



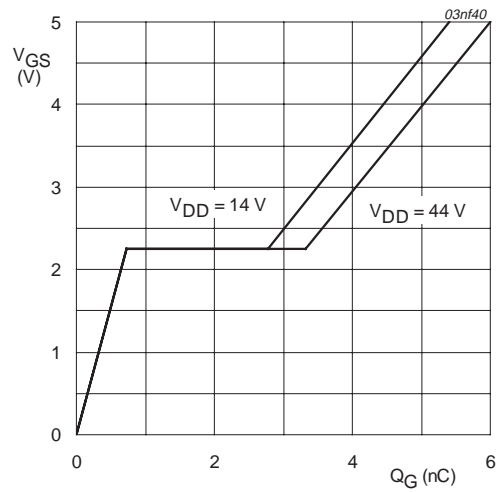
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



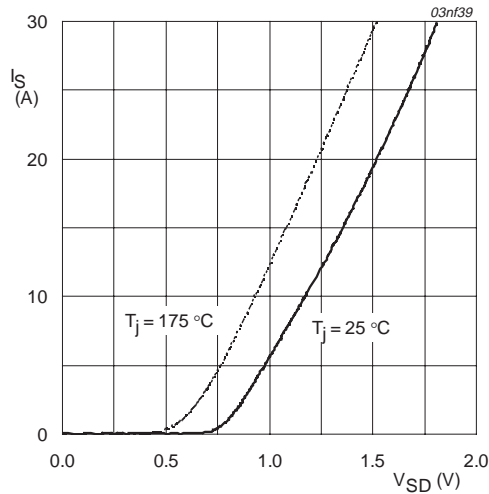
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25 \text{ }^\circ\text{C}; I_D = 5 \text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



$V_{GS} = 0 \text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

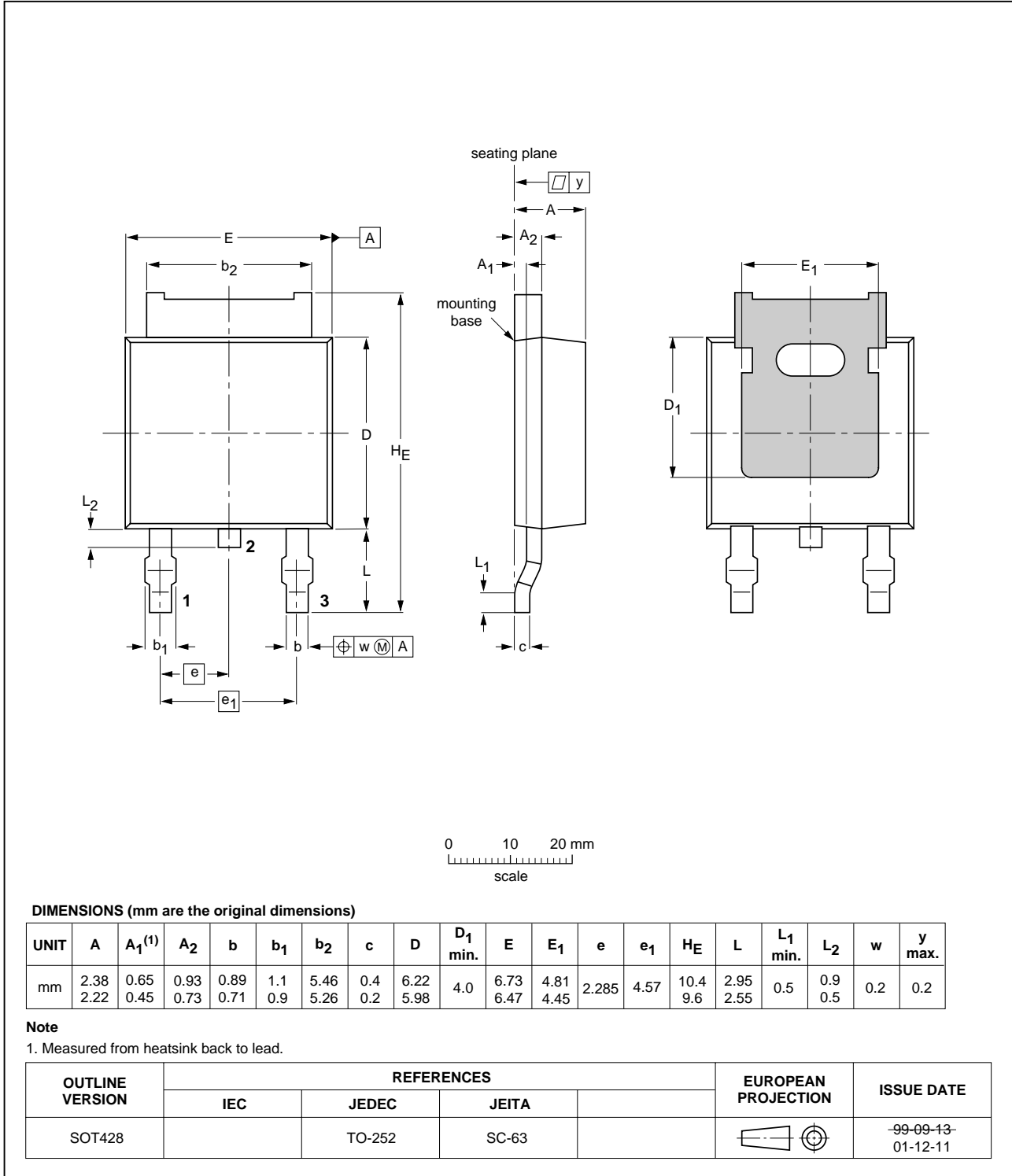


Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20020530	-	Product data (9397 750 09725) Modifications: <ul style="list-style-type: none">• R_{DSon} Max @ 5 V lowered to 140 mΩ. Values @ 10 V and 4.5 V adjusted accordingly.
02	20010703	-	Product data; second version.
01	20000690	-	Product data; initial manuscript version.

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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 Printed in The Netherlands

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Date of release: 30 May 2002

Document order number: 9397 750 09725



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