

BUK95/96/9E4R4-40B

TrenchMOS™ logic level FET

Rev. 02 — 13 October 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive (HPA) TrenchMOS™ technology.

1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Logic level compatible.

1.3 Applications

- Automotive systems
- Motors, lamps and solenoids
- 12 V loads
- General purpose power switching.

1.4 Quick reference data

- $E_{DS(AL)S} \leq 961$ mJ
- $I_D \leq 75$ A
- $R_{DS(on)} = 3.9$ m Ω (typ)
- $P_{tot} \leq 254$ W.

2. Pinning information

Table 1: Pinning - SOT78, SOT404, and SOT226 simplified outlines and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		
		SOT78 (TO-220AB) SOT404 (D²-PAK) SOT226 (I²-PAK)	

[1] It is not possible to make connection to pin 2 of the SOT404 package.

3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
BUK954R4-40B	TO-220AB	Plastic single-ended heat-sink mounted package	SOT78
BUK964R4-40B	D ² -PAK	Plastic single-ended surface mounted package	SOT404
BUK9E4R4-40B	I ² -PAK	Plastic single-ended low-profile package	SOT226

4. Limiting values

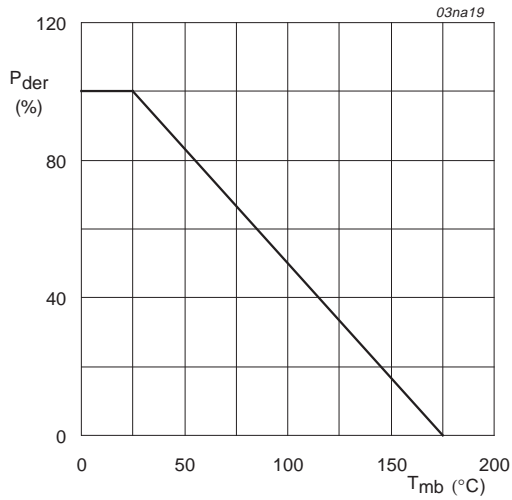
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	40	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage (DC)		-	± 15	V
I_D	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V};$ Figure 2 and 3	[1] -	174	A
			[2] -	75	A
		$T_{mb} = 100 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V};$ Figure 2	[2] -	75	A
I_{DM}	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C};$ pulsed; $t_p \leq 10 \text{ }\mu\text{s};$ Figure 3	-	697	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C};$ Figure 1	-	254	W
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$
T_j	junction temperature		-55	+175	$^\circ\text{C}$
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	[1] -	174	A
			[2] -	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C};$ pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	697	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75 \text{ A};$ $V_{DS} \leq 40 \text{ V}; V_{GS} = 5 \text{ V}; R_{GS} = 50 \text{ }\Omega;$ starting $T_{mb} = 25 \text{ }^\circ\text{C}$	-	961	mJ

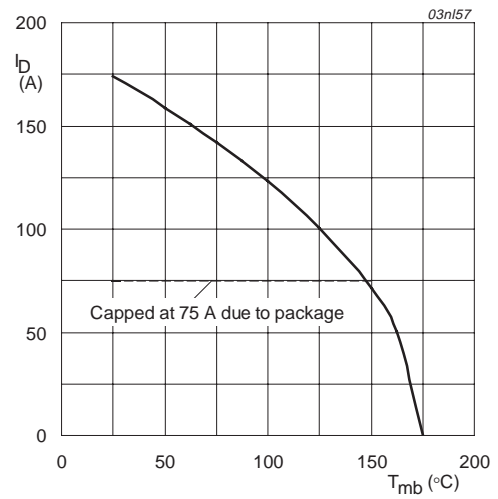
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



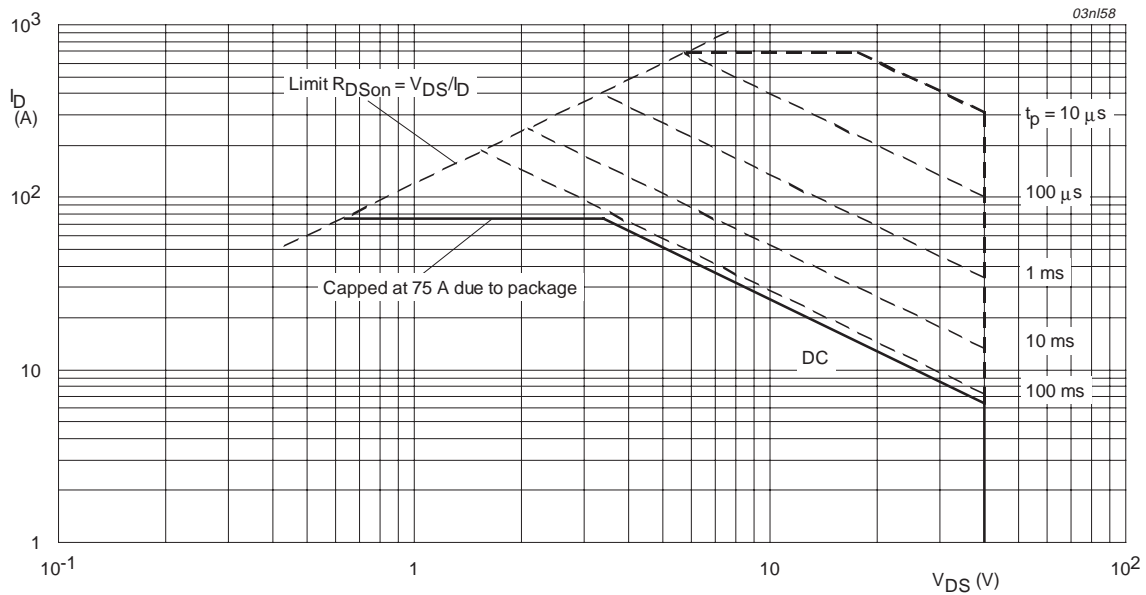
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5 V$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} single pulse.

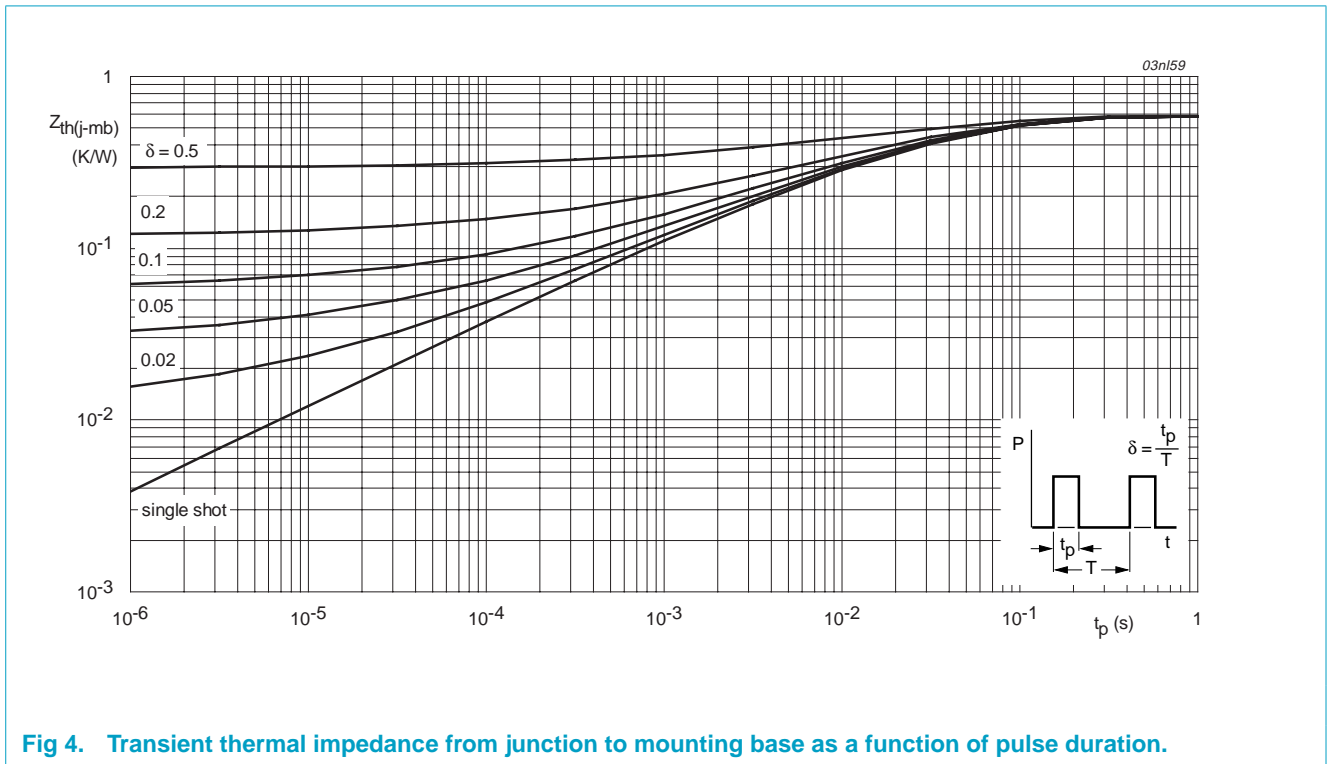
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.59	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78 (TO-220AB)	vertical in still air	-	60	-	K/W
	SOT226 (I ² -PAK)	vertical in still air	-	60	-	K/W
	SOT404 (D ² -PAK)	minimum footprint; mounted on a PCB	-	50	-	K/W

5.1 Transient thermal impedance



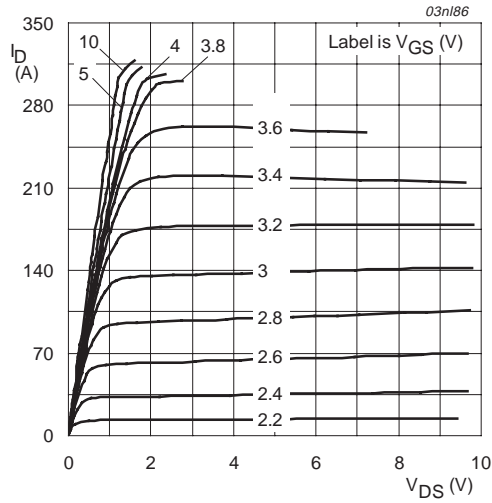
6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	40	-	-	V
		$T_j = -55\text{ °C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	1.1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 40\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.02	1	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	3.9	4.4	m Ω
		$T_j = 175\text{ °C}$	-	-	8.3	m Ω
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}$	-	-	4.8	m Ω
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	-	3.6	4	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 5\text{ V}; V_{DD} = 32\text{ V};$	-	64	-	nC
Q_{gs}	gate-to-source charge	$I_D = 25\text{ A};$ Figure 14	-	11	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	24	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$	-	5343	7124	pF
C_{oss}	output capacitance	$f = 1\text{ MHz};$ Figure 12	-	943	1131	pF
C_{rss}	reverse transfer capacitance		-	408	558	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$	-	44	-	ns
t_r	rise time	$V_{GS} = 5\text{ V}; R_G = 10\text{ }\Omega$	-	118	-	ns
$t_{d(off)}$	turn-off delay time		-	197	-	ns
t_f	fall time		-	132	-	ns
L_d	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die SOT78	-	3.5	-	nH
		from upper edge of drain mounting base to center of die SOT404/SOT226	-	2.5	-	nH
L_s	internal source inductance	from source lead to source bond pad	-	7.5	-	nH

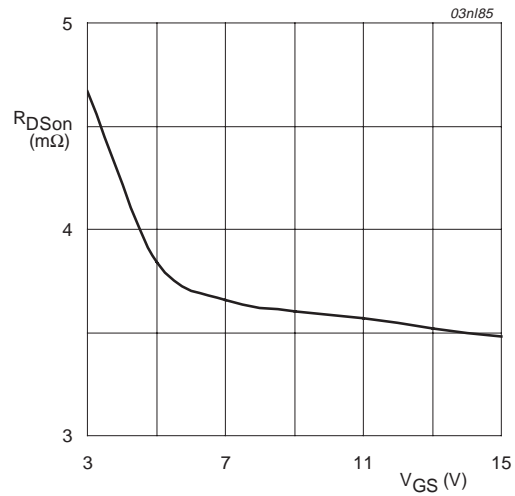
Table 5: Characteristics...continued*T_j = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs	-	70	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V	-	67	-	nC



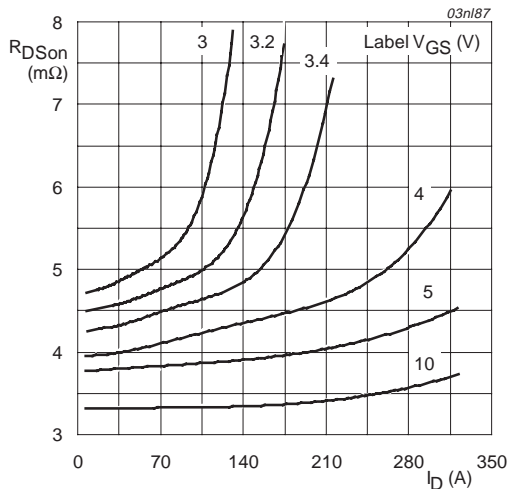
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



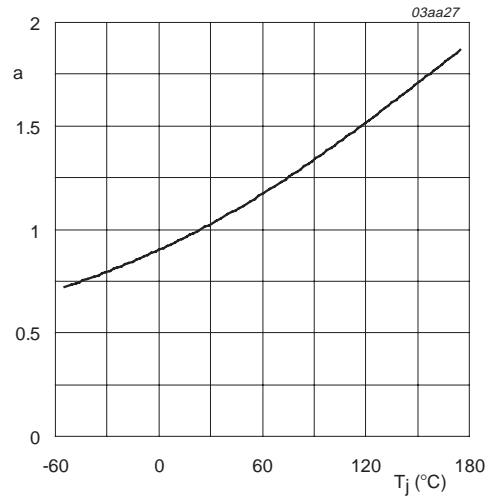
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



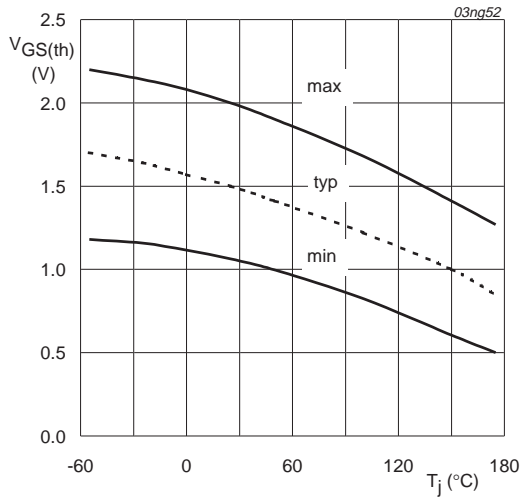
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



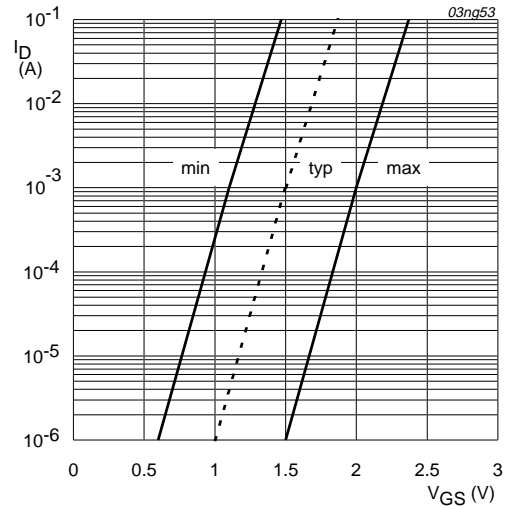
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



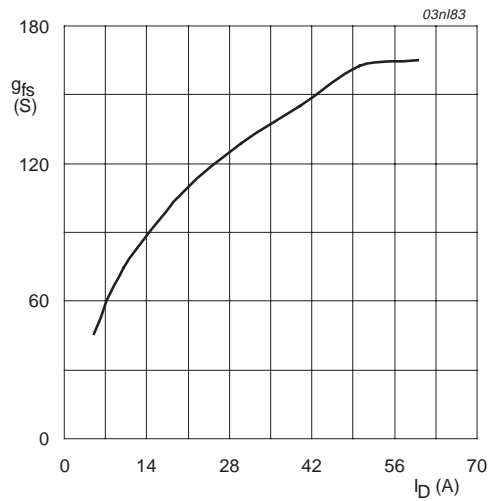
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



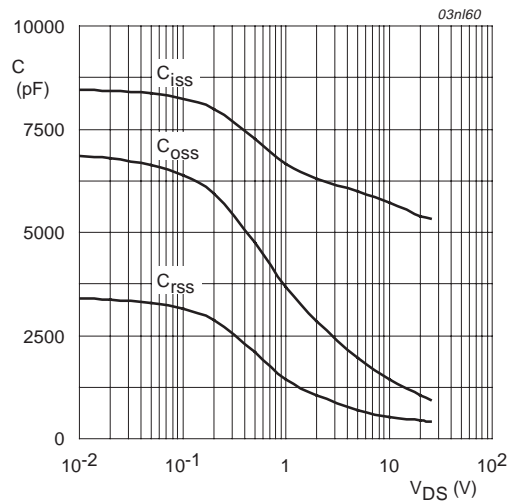
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



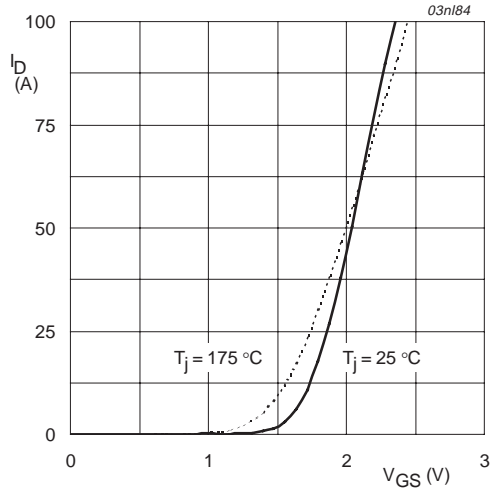
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



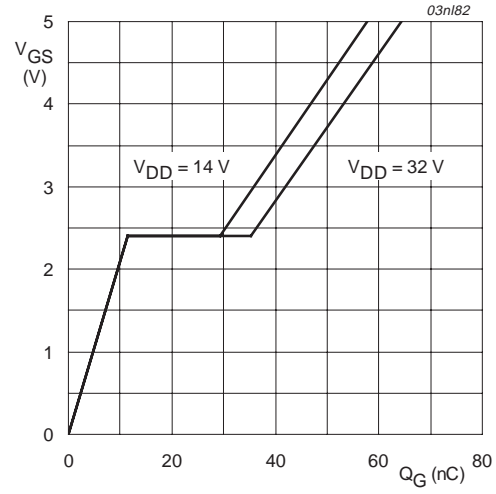
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



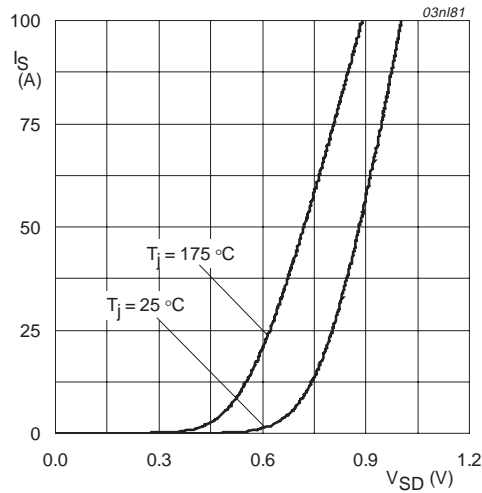
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25 \text{ }^\circ\text{C}; I_D = 25 \text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



$V_{GS} = 0 \text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

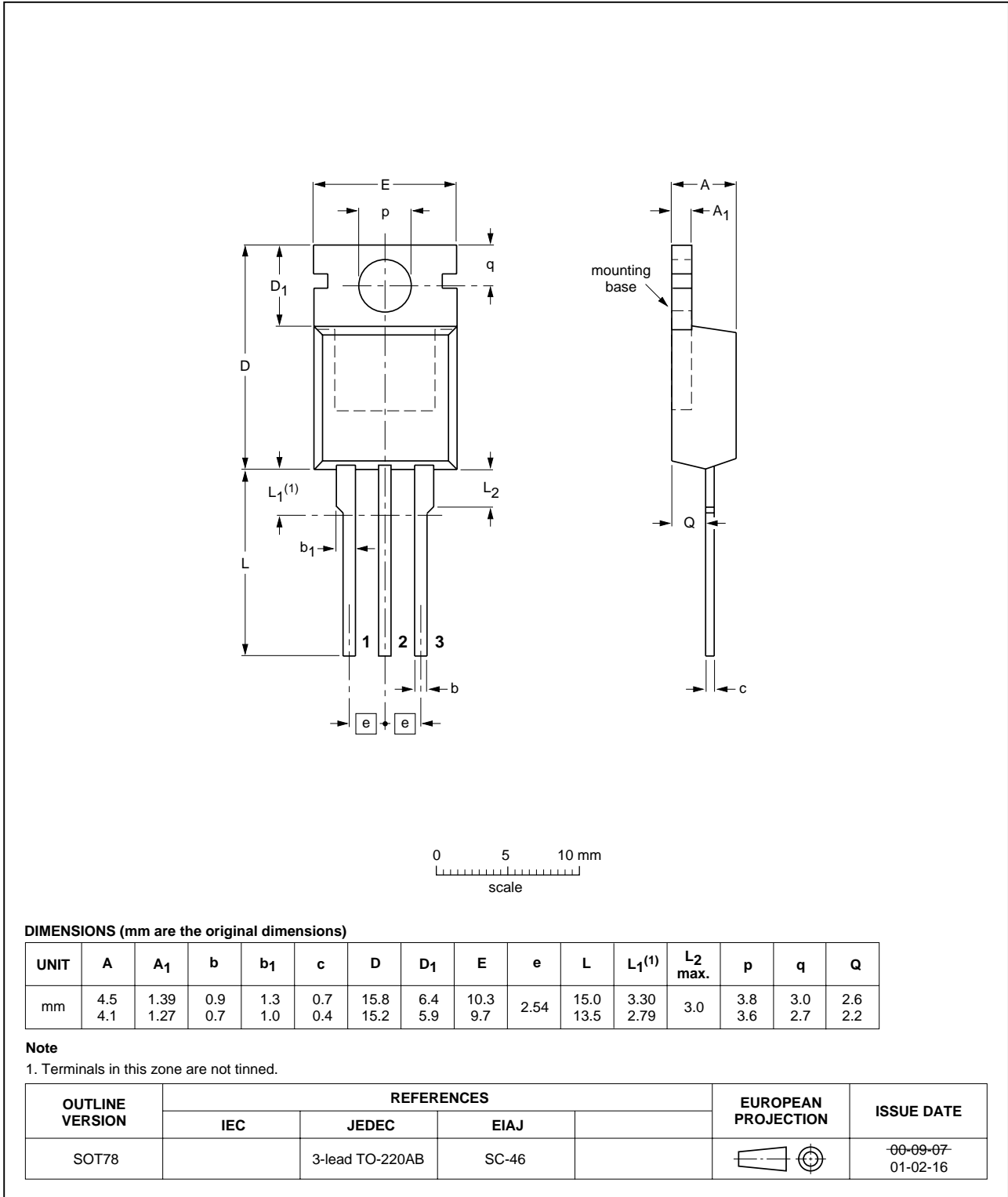


Fig 16. SOT78 (TO-220AB).

Plastic single-ended package; low-profile 3 lead TO-220AB

SOT226

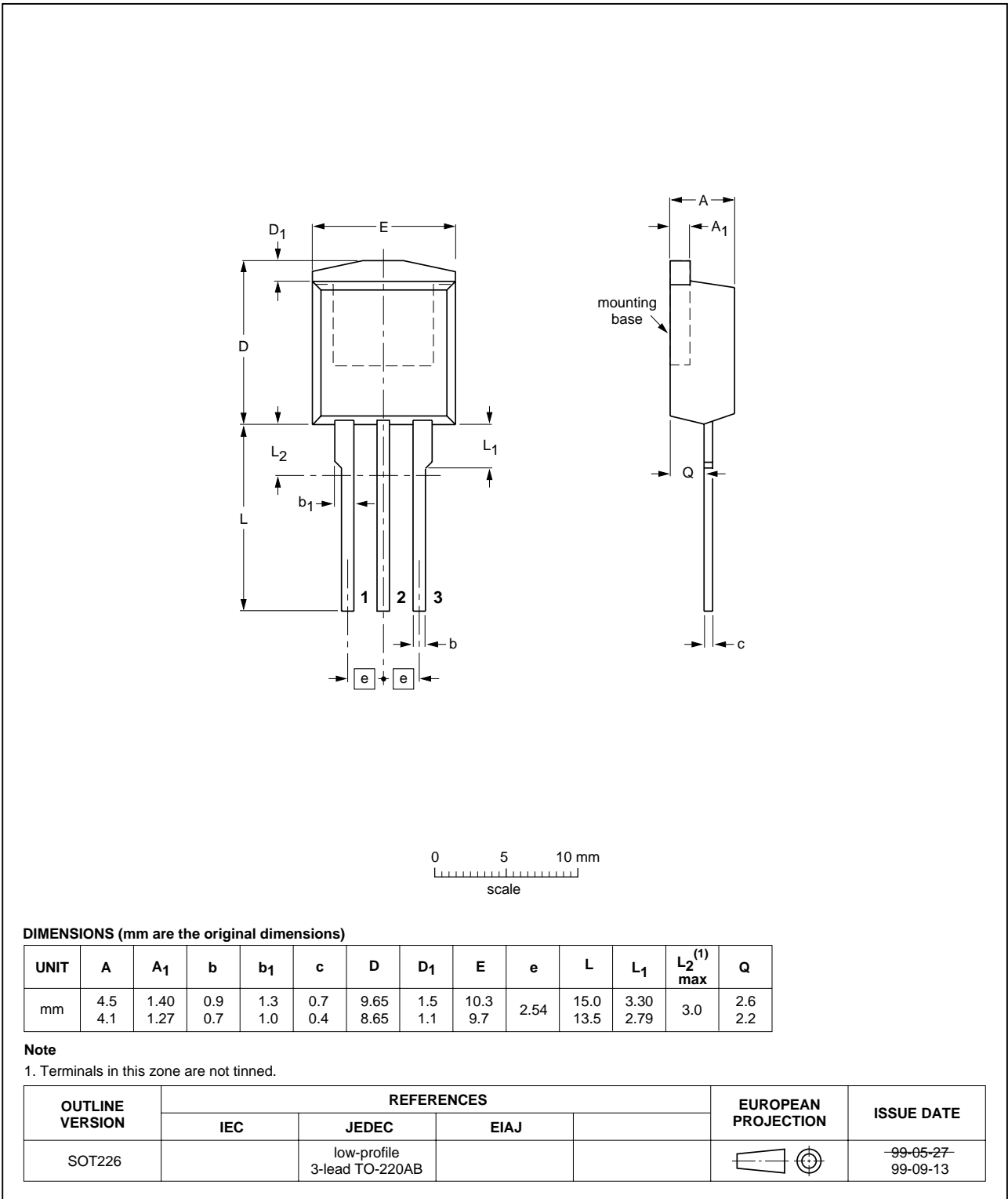


Fig 17. SOT226 (I²-PAK).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404

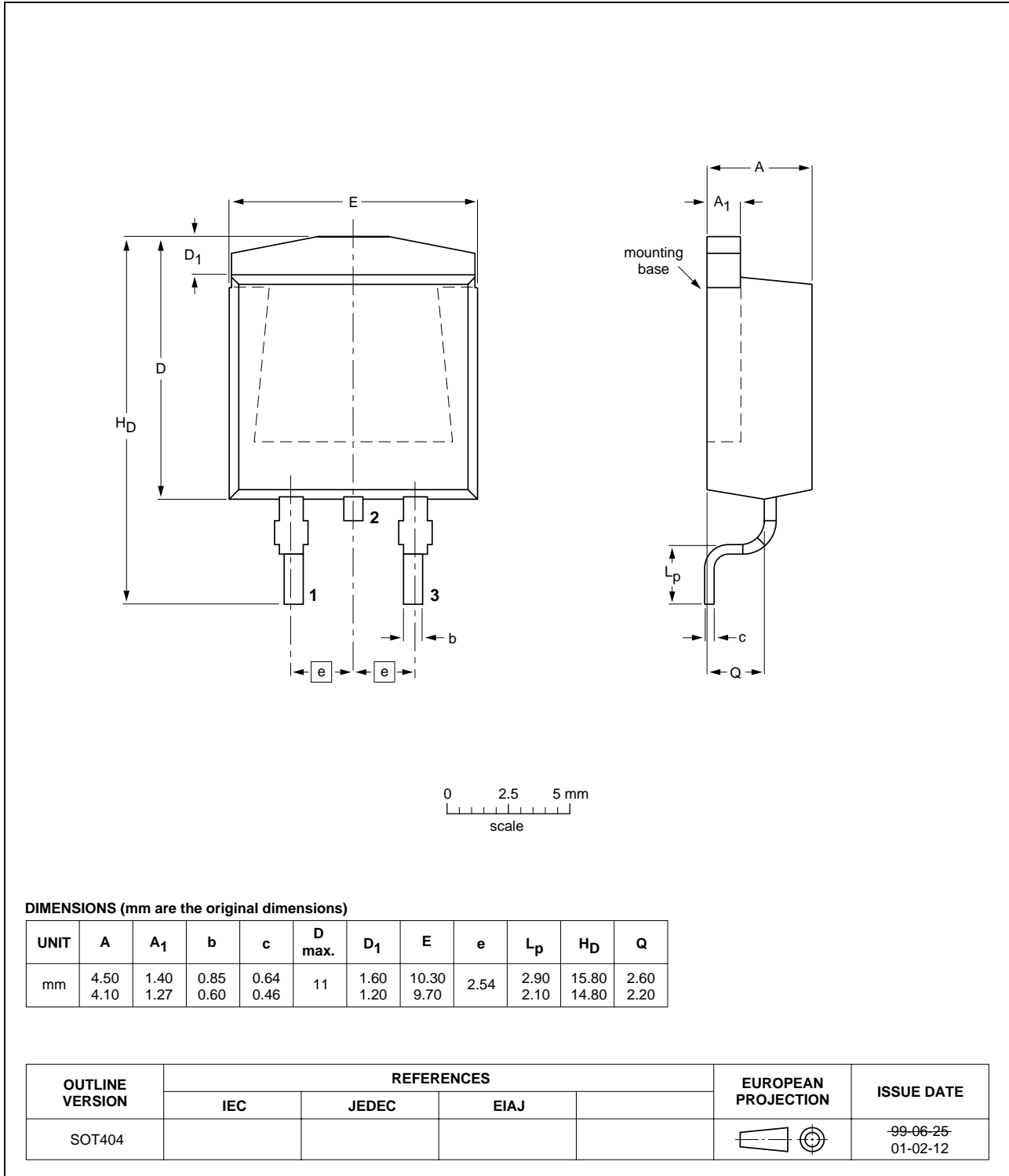
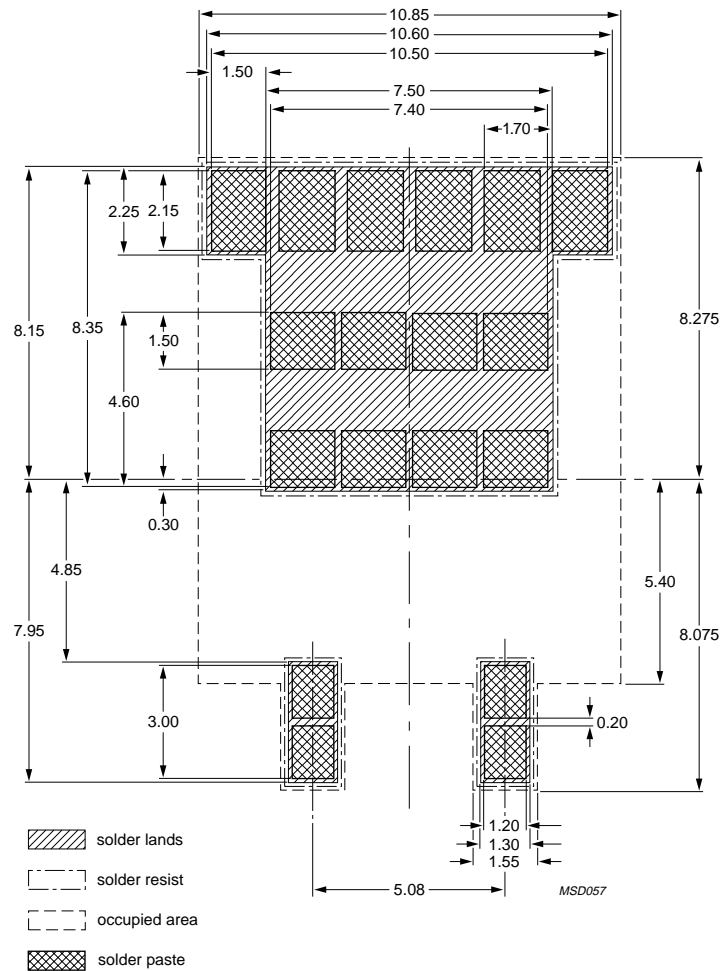


Fig 18. SOT404 (D²-PAK).

8. Soldering



Dimensions in mm.

Fig 19. Reflow soldering footprint for SOT404.

9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20031013	-	Product data (9397 750 12051) Modifications: <ul style="list-style-type: none">• Addition of BUK9E4R4-40B part to data sheet.
01	20030402	-	Product data (9397 750 11134)

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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