



BUK9832-55A

N-channel TrenchMOS logic level FET

Rev. 02 — 1 June 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Q101 compliant

1.3 Applications

- 12 V and 24 V loads
- Motors, lamps and solenoids
- Automotive and general purpose power switching

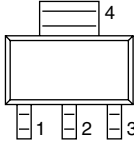
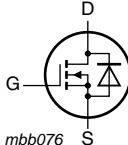
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_{sp} = 25\text{ °C};$ see Figure 1 ; see Figure 3	-	-	12	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C};$ see Figure 2	-	-	8	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 8\text{ A};$ $T_j = 25\text{ °C}$	-	-	36	m Ω
		$V_{GS} = 10\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C}$	-	25	29	m Ω
		$V_{GS} = 5\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C};$ see Figure 12 ; see Figure 13	-	27	32	m Ω
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 10\text{ A}; V_{sup} \leq 55\text{ V};$ $R_{GS} = 50\text{ }\Omega; V_{GS} = 5\text{ V};$ $T_{j(init)} = 25\text{ °C};$ unclamped	-	-	100	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT223 (SC-73)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
4	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9832-55A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

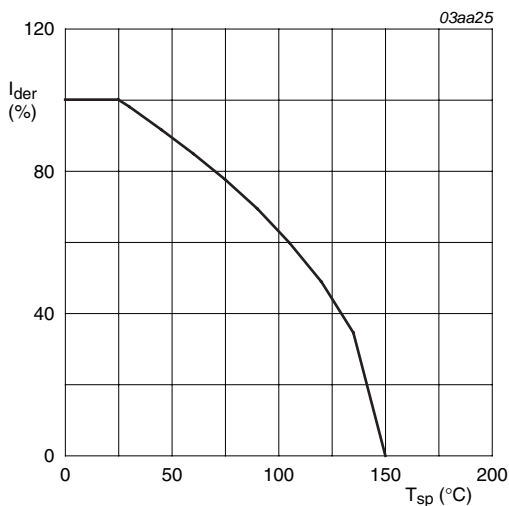
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	-	55	V
V_{GS}	gate-source voltage		-10	-	10	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1 ; see Figure 3	-	-	12	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1	-	-	7	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 3	-	-	47	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	-	8	W
T_{stg}	storage temperature		-55	-	150	°C
T_j	junction temperature		-55	-	150	°C
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50\text{ }\mu\text{s}$	-15	-	15	V

Source-drain diode

I_S	source current	$T_{sp} = 25\text{ °C}$	-	-	12	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{sp} = 25\text{ °C}$	-	-	47	A

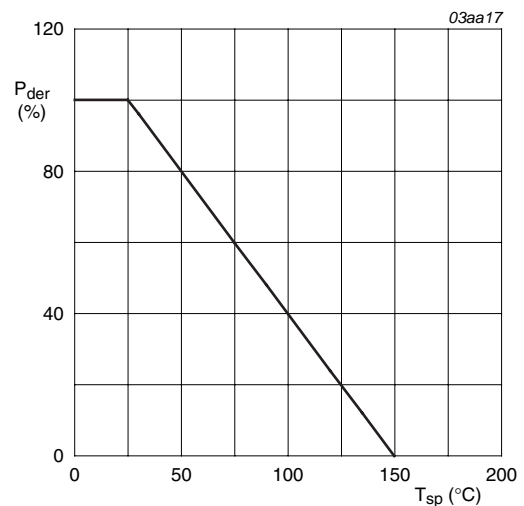
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 10\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped	-	-	100	mJ
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$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature

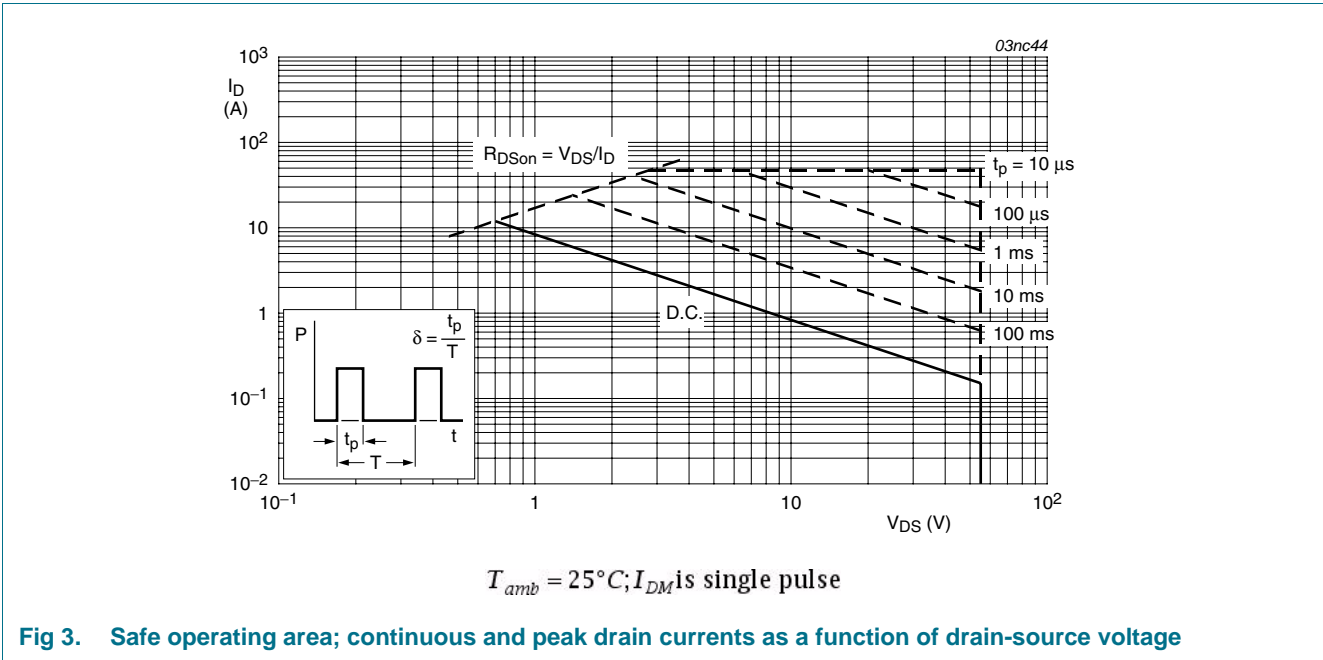


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	see Figure 4	-	70	-	K/W

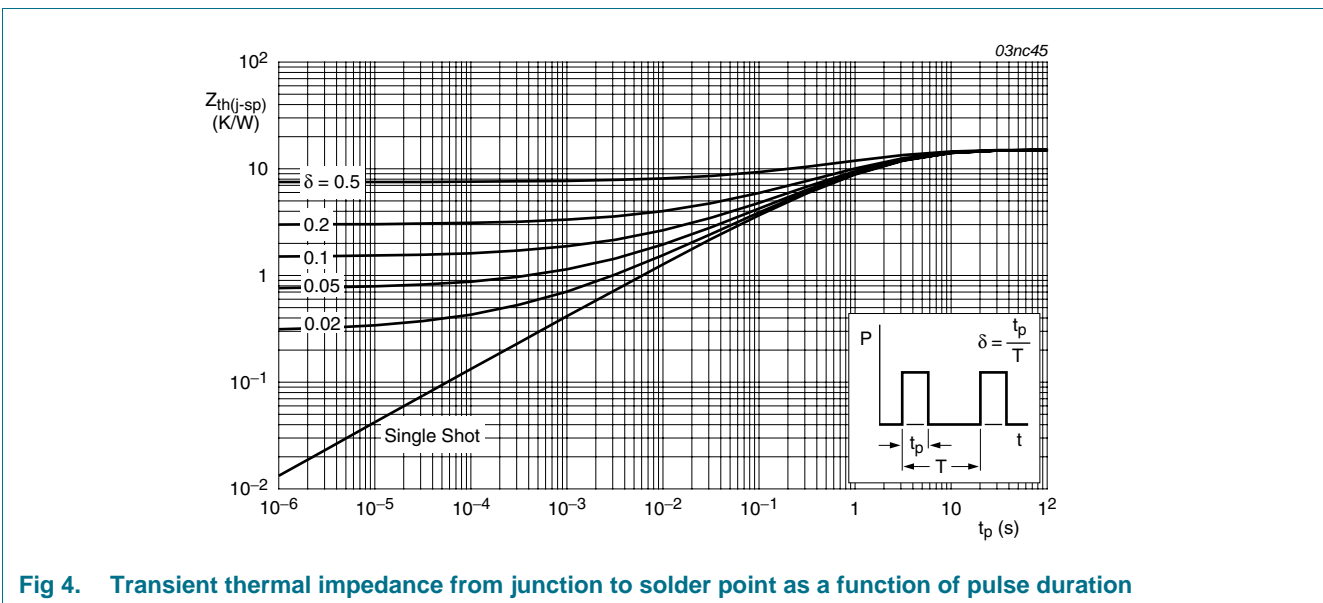
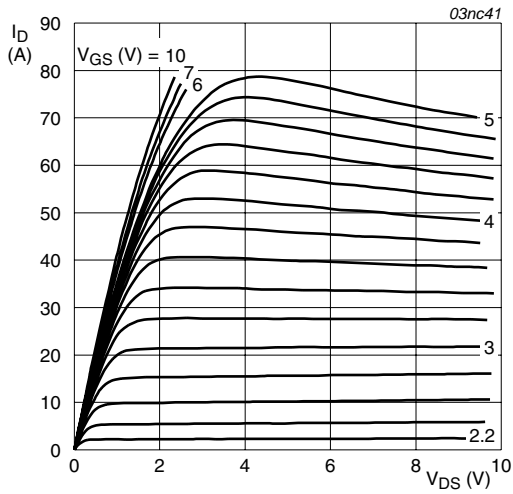


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

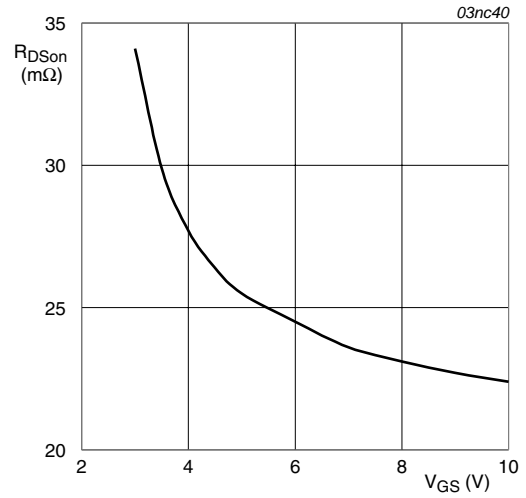
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 11	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 11	0.6	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	500	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	36	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 8 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	-	59	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	25	29	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	27	32	m Ω
Dynamic characteristics						
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	-	1195	1594	pF
C_{oss}	output capacitance		-	212	254	pF
C_{rss}	reverse transfer capacitance		-	144	198	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	14	-	ns
t_r	rise time		-	125	-	ns
$t_{d(off)}$	turn-off delay time		-	64	-	ns
t_f	fall time		-	68	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 18 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$ $V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	51	-	ns
Q_r	recovered charge		-	80	-	nC



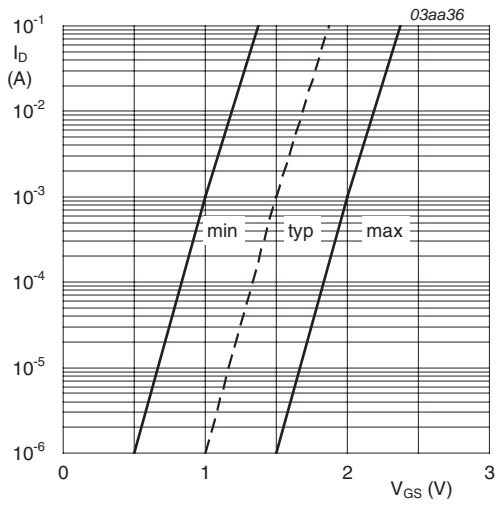
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



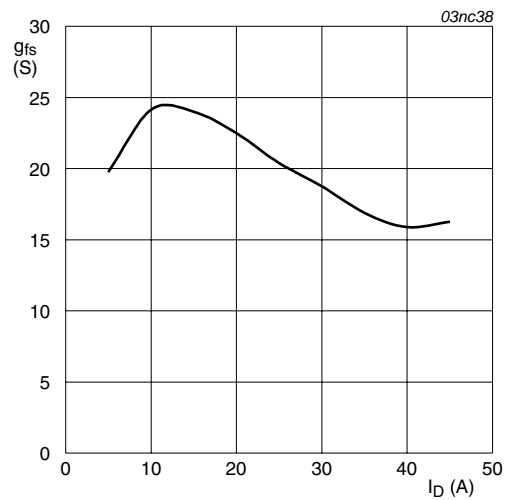
$T_j = 25^\circ\text{C}; I_D = 15\text{A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values

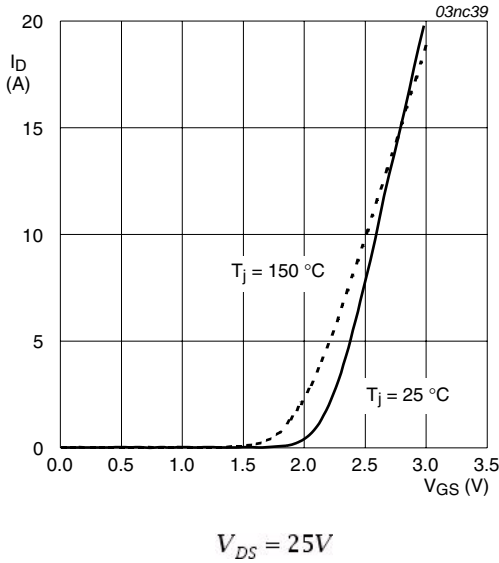


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

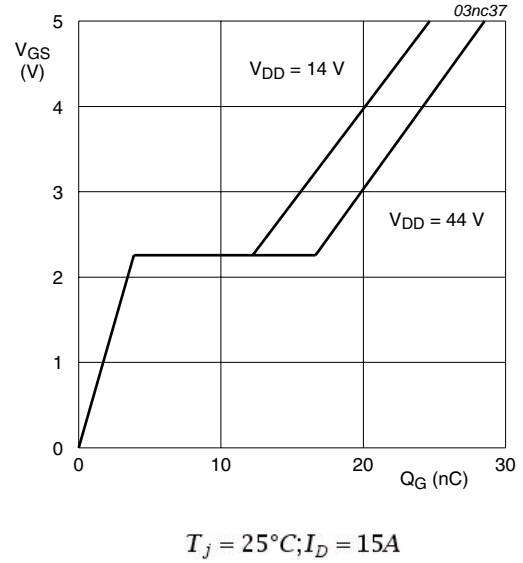


Fig 10. Gate-source voltage as a function of turn-on gate charge; typical values

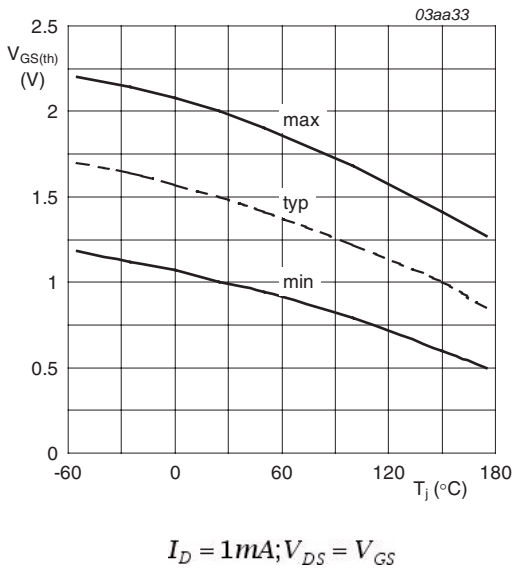


Fig 11. Gate-source threshold voltage as a function of junction temperature

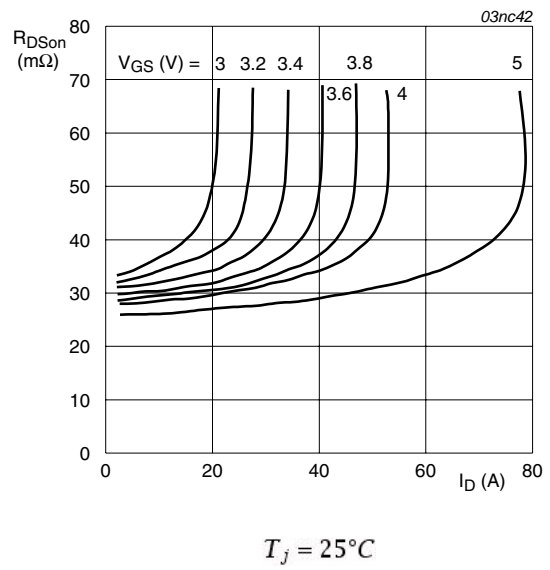
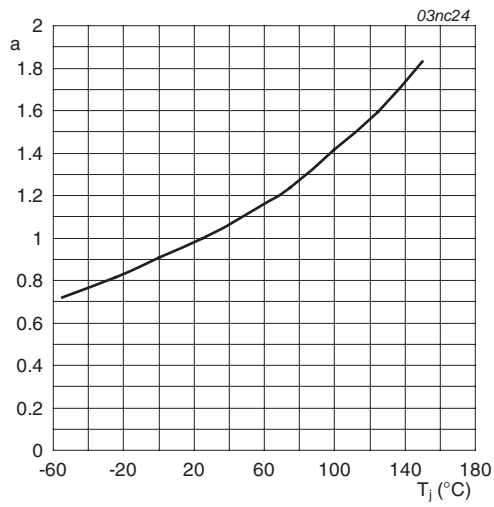
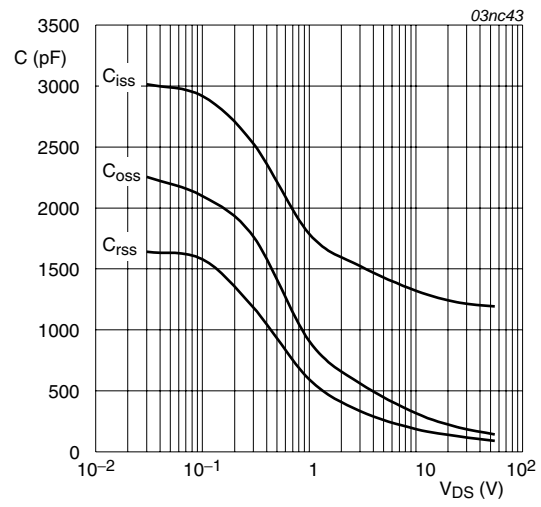


Fig 12. Drain-source on-state resistance as a function of drain current; typical values



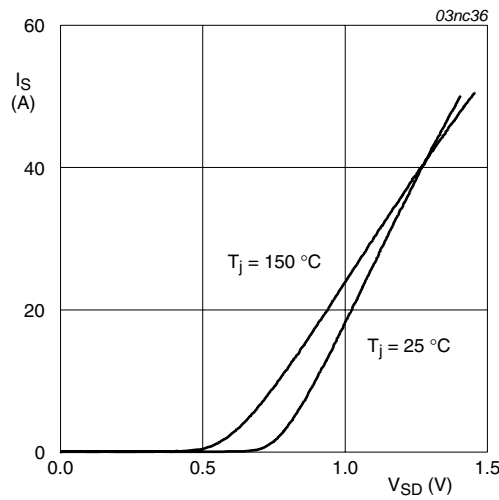
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 13. Normalized drain source on-state resistance factor as a function of junction temperature



$$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$$V_{GS} = 0 \text{ V}$$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical value

7. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

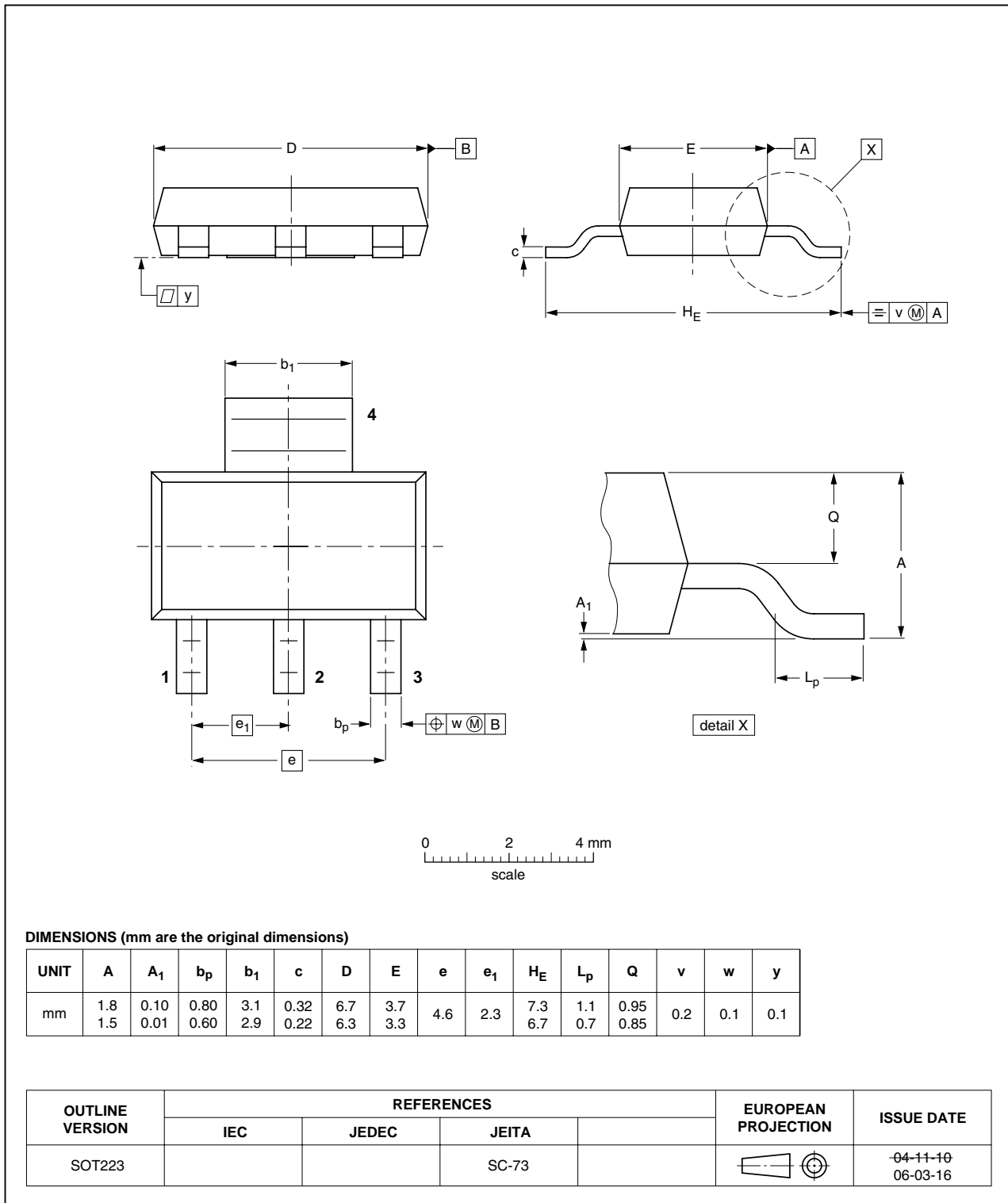


Fig 16. Package outline SOT223 (SC-73)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9832-55A v.2	20100601	Product data sheet	-	BUK9832-55A-01
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.			
BUK9832-55A-01 (9397 750 07734)	20010131	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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