

BUK9C07-65BIT

N-channel TrenchPLUS logic level FET

Rev. 02 — 17 June 2010

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode field-effect power transistor in SOT427. Device is manufactured using NXP High-Performance TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistor and over temperature protection diodes.

1.2 Features and benefits

- AEC-Q101 compliant
- Low conduction losses due to low on-state resistance

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

1.4 Quick reference data

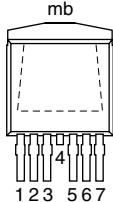
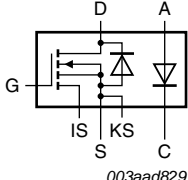
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12 ; see Figure 13	-	6	7	mΩ
I_D/I_{sense}	ratio of drain current to sense current	$T_j = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 14	1086	1206	1327	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ μA}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	65	-	-	V



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT427 (D2PAK)</p>	
2	IS	current sense		
3	A	anode		
4	D	drain		
5	K	cathode		
6	KS	Kelvin source		
7	S	source		
mb	D	mb		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9C07-65BIT	D2PAK	plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)	SOT427

4. Limiting values

Table 4. Limiting values

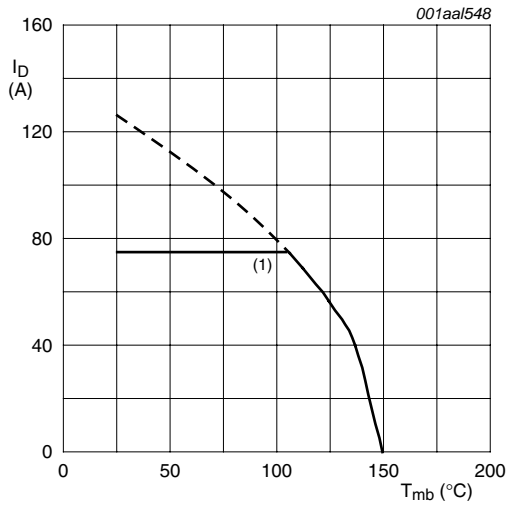
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
V_{GS}	gate-source voltage		-15	-	15	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	[1]	-	75	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	[1]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 4	-	-	550	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	245	W
T_{stg}	storage temperature		-55	-	150	°C
T_j	junction temperature		-55	-	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	-	100	V
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	75	A
I_{SM}	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	-	550	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 32.6\text{ A}$; $V_{sup} = 65\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; see Figure 3	[2]	[3]	0.605	J
Electrostatic discharge						
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 k Ω ; all pins	-	-	0.15	kV
		HBM; C = 100 pF; R = 1.5 k Ω ; pin 4 to pin 7	-	-	4	kV

[1] Current is limited by package.

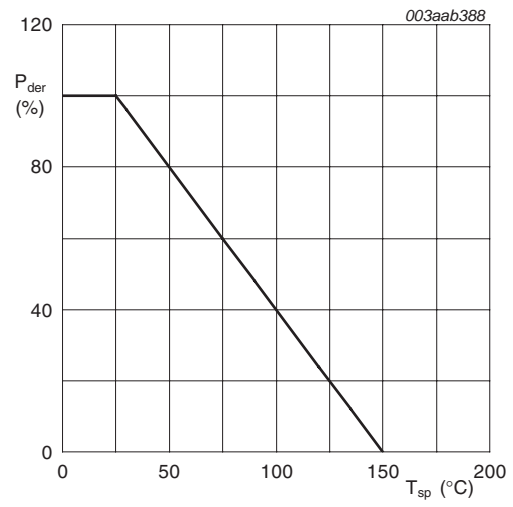
[2] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

[3] Refer to application note AN10273 for further information.



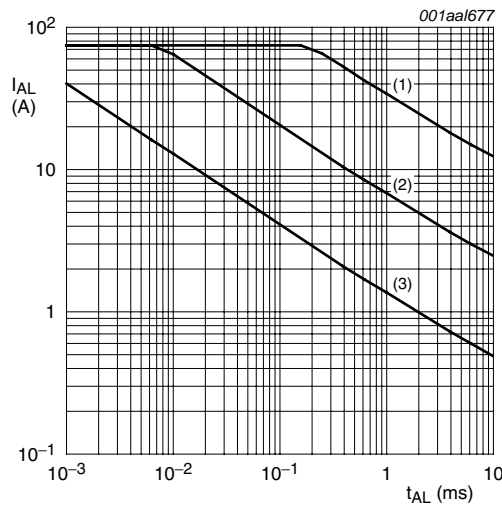
$$V_{GS} \geq 5V$$

Fig 1. Continuous drain current as a function of solder point temperature.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



- (1) Single-pulse; $T_j = 25^{\circ}C$.
- (2) Single-pulse; $T_j = 150^{\circ}C$.
- (3) Repetitive.

Fig 3. Single-Pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.

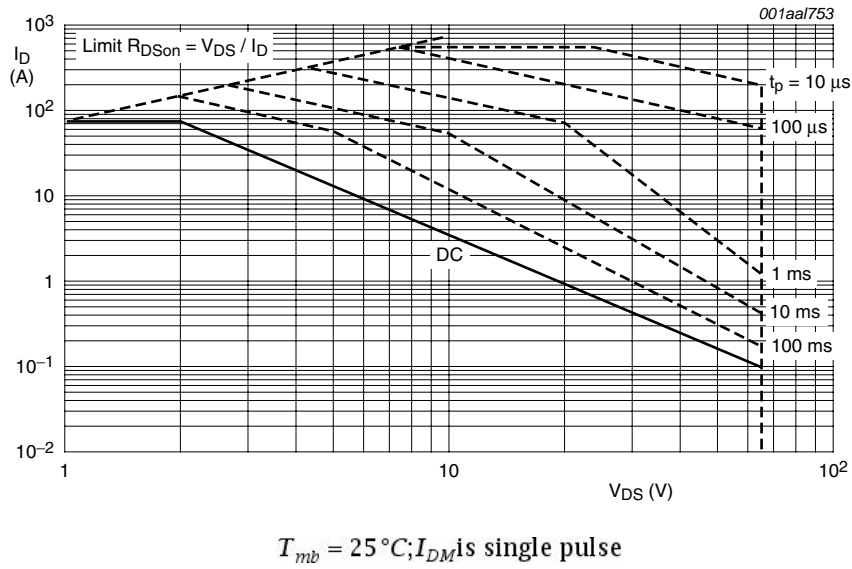


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.51	K/W

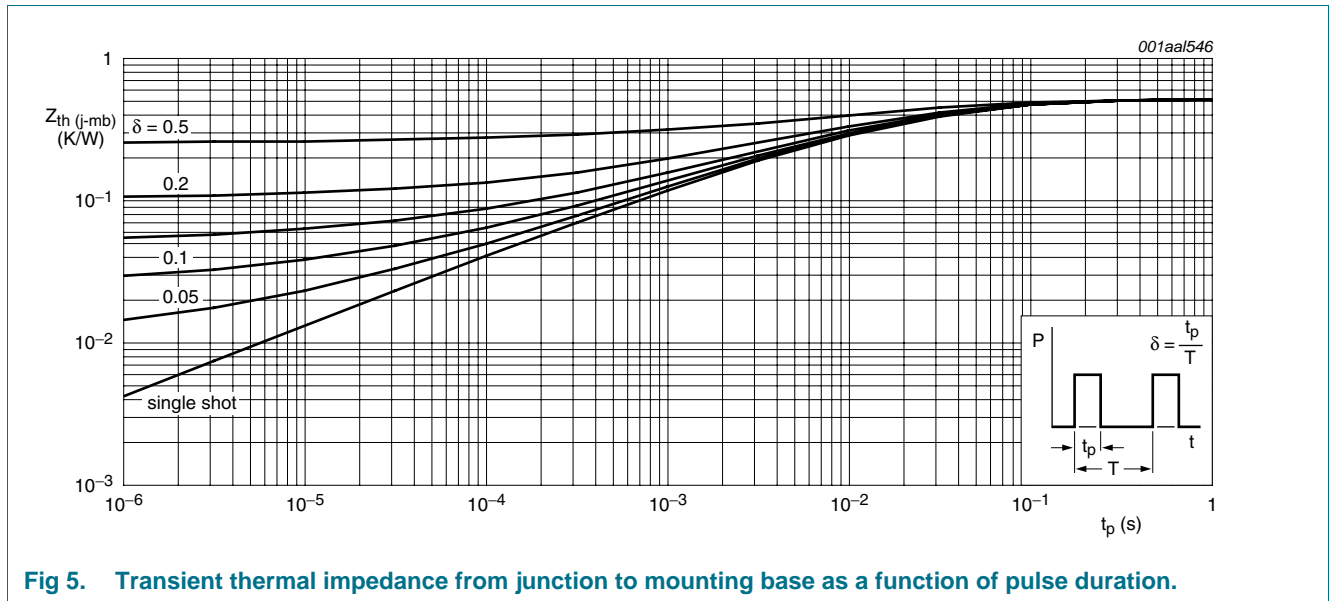


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

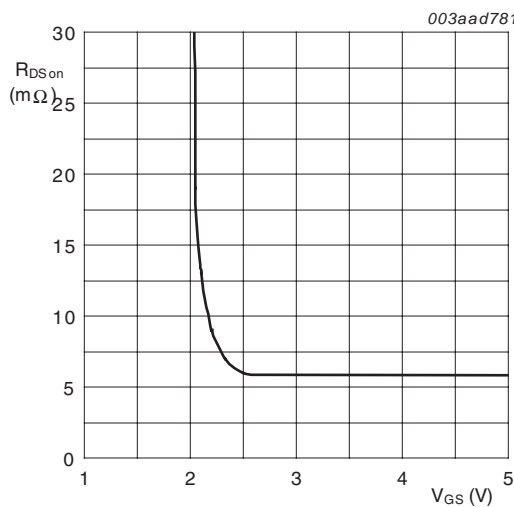
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	65	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	59	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	-	-	2.3	V
I_{DSS}	drain leakage current	$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	3	μA
		$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	125	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	300	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	-	7.6	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	6	7	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	-	13.5	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	-	6.5	m Ω
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	10861	12068	13275	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250 \mu\text{A}; 25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C};$ see Figure 15	-5.4	-5.7	-6	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250 \mu\text{A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 15	2.855	2.9	2.945	V
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 52 \text{ V}; V_{GS} = 5 \text{ V};$ see Figure 16	-	102.8	-	nC
Q_{GS}	gate-source charge		-	16.4	-	nC
Q_{GD}	gate-drain charge		-	36.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 17	-	7127	-	pF
C_{oss}	output capacitance		-	900	-	pF
C_{rss}	reverse transfer capacitance		-	354	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega$	-	59	-	ns
t_r	rise time		-	180	-	ns
$t_{d(off)}$	turn-off delay time		-	328	-	ns
t_f	fall time		-	173	-	ns
L_D	internal drain inductance	from pin to center of die	-	0.9	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	2	-	nH

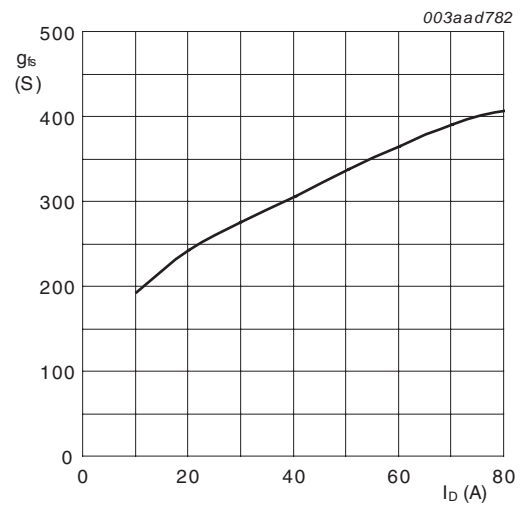
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 18	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$	-	60.1	-	ns
Q_r	recovered charge		-	0.161	-	nC



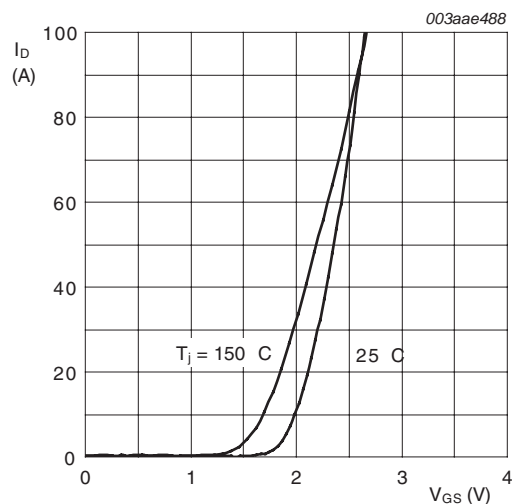
$$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage



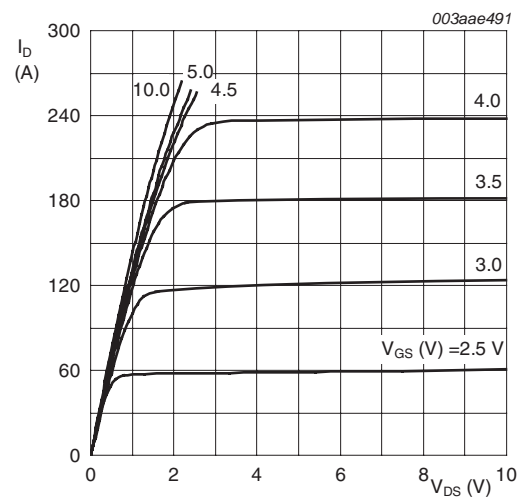
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$$

Fig 7. Forward transconductance as a function of drain current; typical values



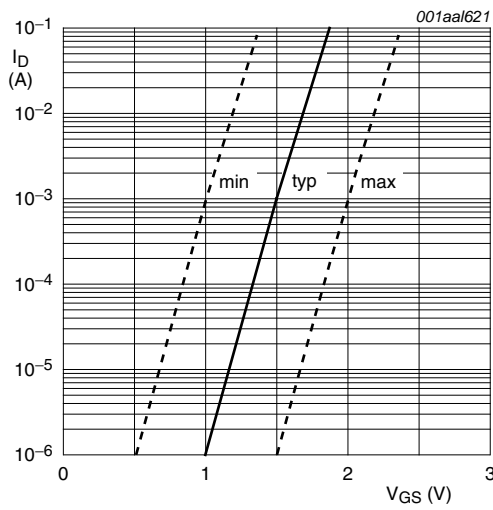
$$V_{DS} = 25\text{ V}$$

Fig 8. Transfer characteristics; drain current as a function of gate-source voltage



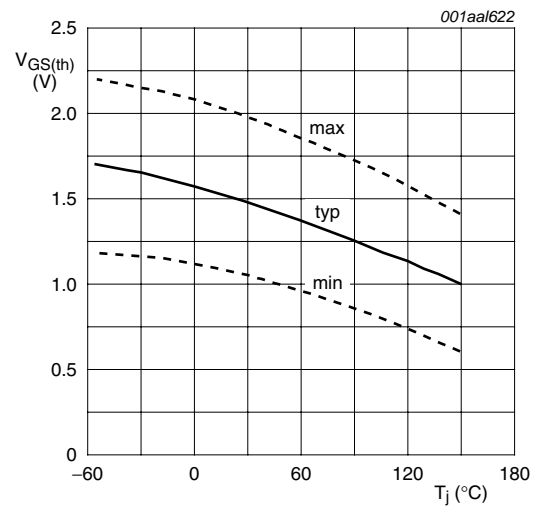
$$T_j = 25\text{ }^\circ\text{C}; t_p = 300\mu\text{s}$$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values.



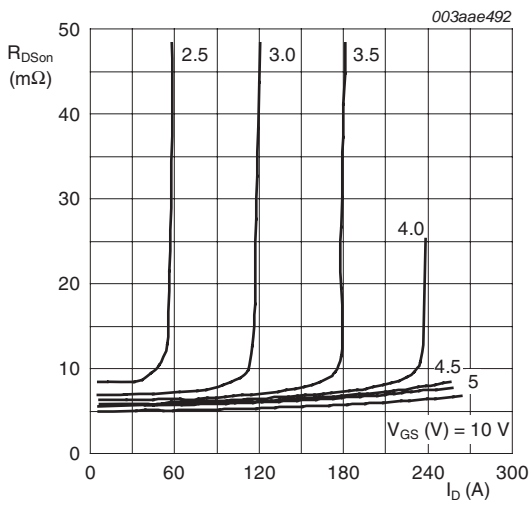
$$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



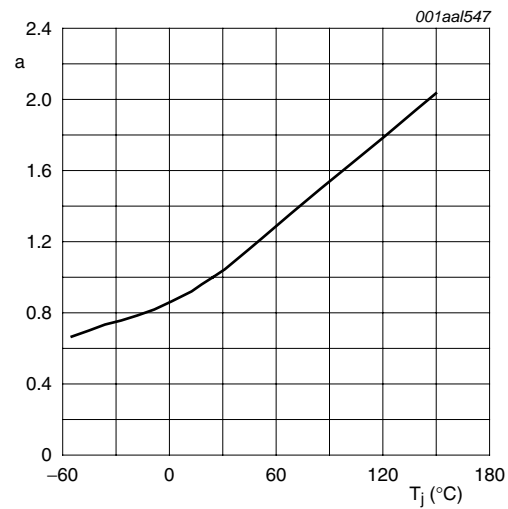
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

Fig 11. Gate-source threshold voltage as a function of junction temperature.



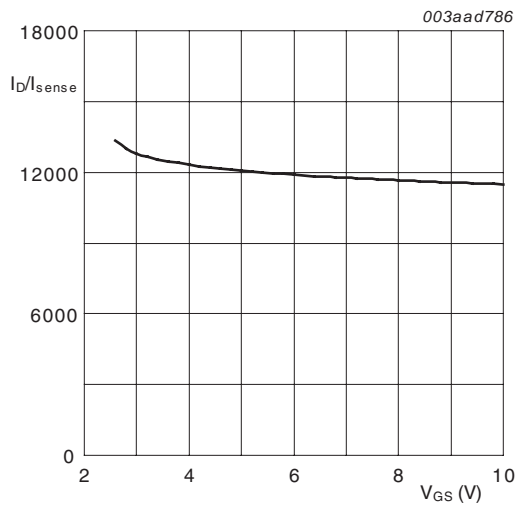
$$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$$

Fig 12. Drain-source on-state resistance as a function of drain current



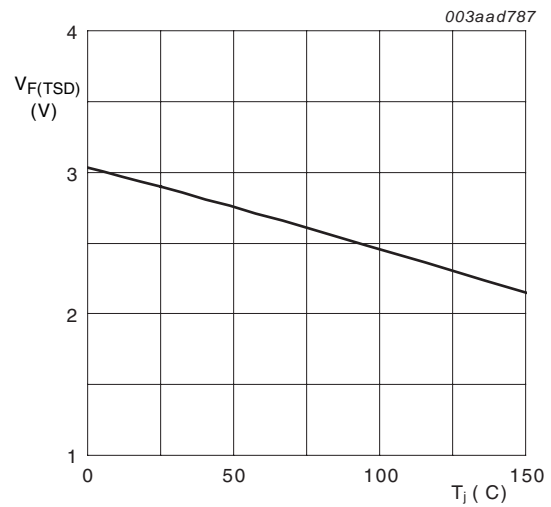
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 13. Normalized Drain-Source on-state resistance factor as a function of junction temperature.



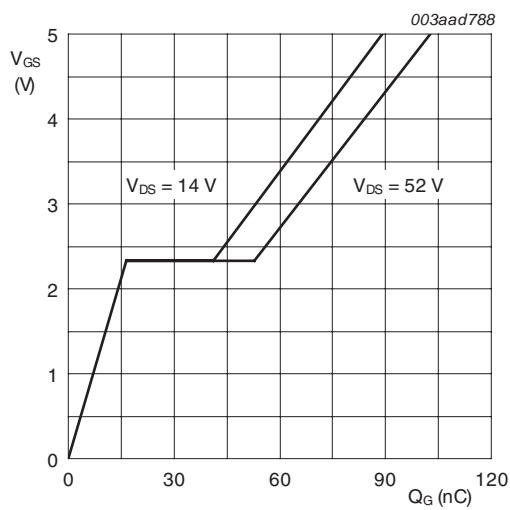
$T_j = 25^\circ\text{C}; I_D = 5\text{A}$

Fig 14. Ratio of drain current to sense current as a function of gate-source voltage



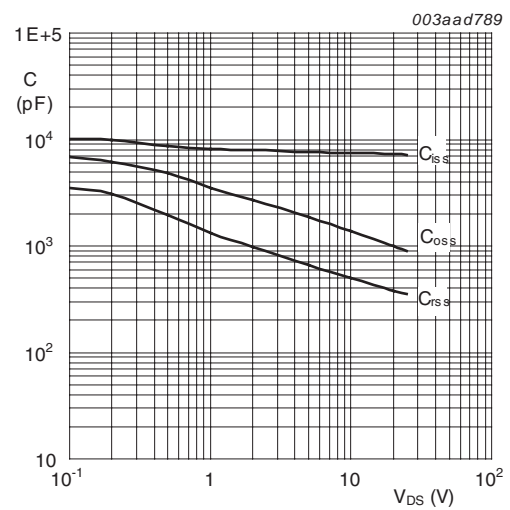
$I_F = 250\mu\text{A}$

Fig 15. Temperature sense diode forward voltage as a function of junction temperature



$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 16. Gate-source voltage as a function of turn-on gate charge



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage

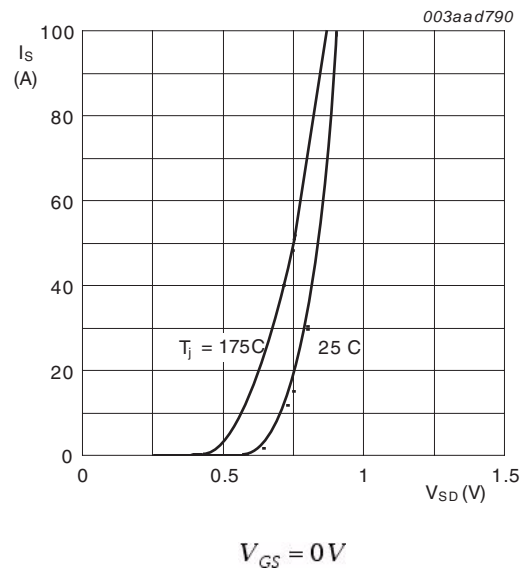


Fig 18. Source (diode forward) current as a function of source-drain (diode forward) voltage

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)

SOT427

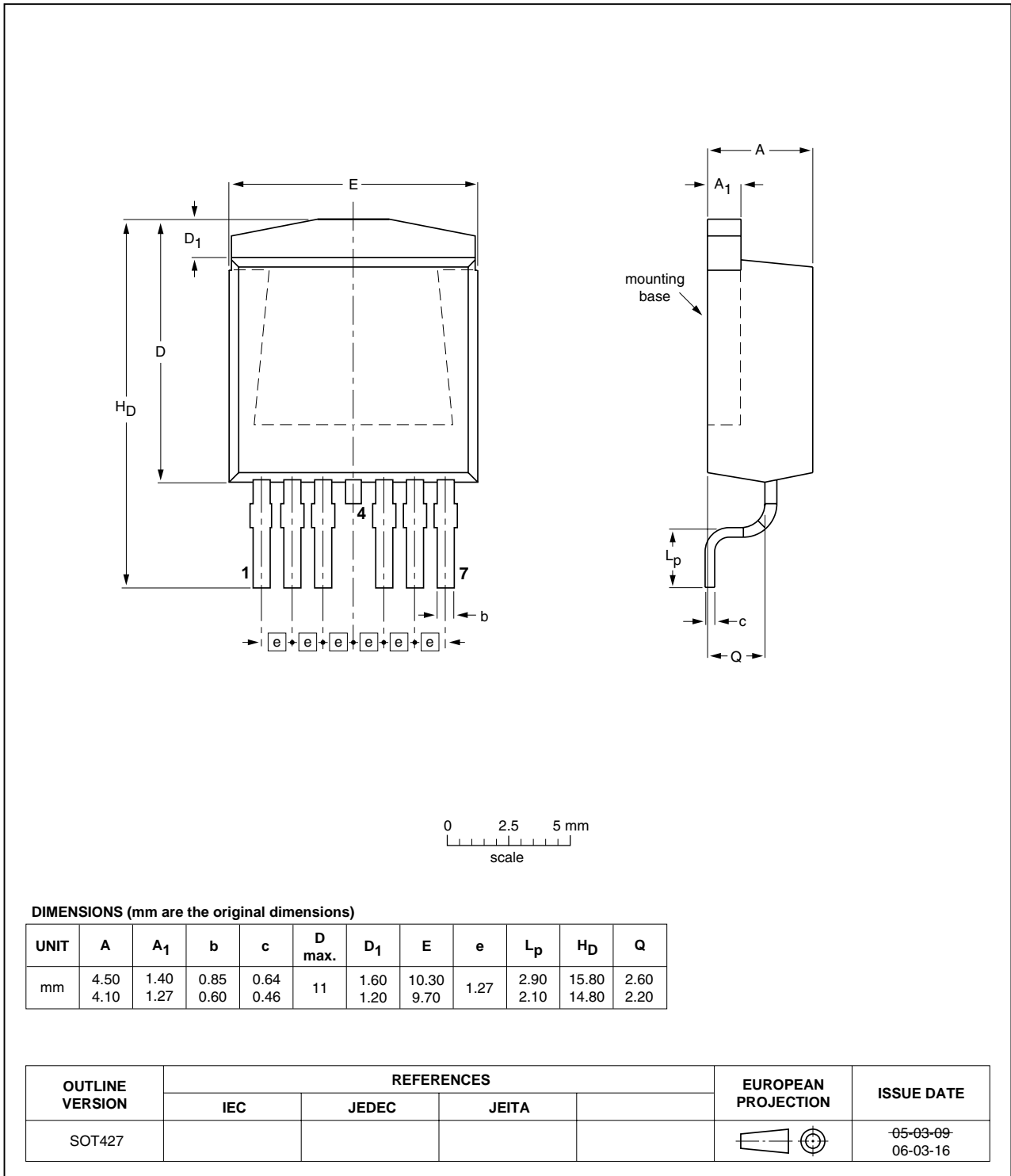


Fig 19. Package outline SOT427 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9C07-65BIT v.2	20100617	Product data sheet	-	BUK9C07-65BIT v.1
Modifications:	<ul style="list-style-type: none">• Status changed from preliminary to product.• Various changes to content.			
BUK9C07-65BIT v.1	20100531	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

9.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding. **Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Adelante, Bitport, Bitsound, CoolFlux, CoReUse, DESFire, EZ-HV, FabKey, GreenChip, HiPerSmart, HITAG, I²C-bus logo, ICODE, I-CODE, ITEC, Labelution, MIFARE, MIFARE Plus, MIFARE Ultralight, MoReUse, QLPK, Silicon Tuner, SiliconMAX, SmartXA, STARplug, TOPFET, TrenchMOS, TriMedia and UCODE — are trademarks of NXP B.V.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

HD Radio and **HD Radio logo** — are trademarks of iBiquity Digital Corporation.

10. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	3
5	Thermal characteristics	6
6	Characteristics	7
7	Package outline	12
8	Revision history	13
9	Legal information	14
9.1	Data sheet status	14
9.2	Definitions	14
9.3	Disclaimers	14
9.4	Trademarks	15
10	Contact information	15

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 June 2010

Document identifier: BUK9C07-65BIT