

BUK9506-55A; BUK9606-55A; BUK9E06-55A

TrenchMOS™ logic level FET

Rev. 03 — 23 July 2001

Product data

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance.

Product availability:

BUK9506-55A in SOT78 (TO-220AB); BUK9606-55A in SOT404 (D²-PAK);

BUK9E06-55A in SOT226 (I²-PAK).

2. Features

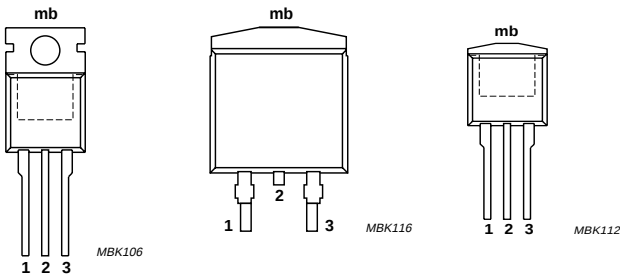
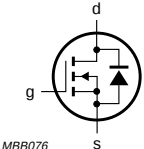
- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching:
 - ◆ 12 V and 24 V loads
 - ◆ Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT226 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base, connected to drain (d)		
		SOT78 (TO-220AB) SOT404 (D²-PAK) SOT226 (I²-PAK)	

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		–	55	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$	[1] –	154	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	–	300	W
T_j	junction temperature		–	175	°C
$R_{DS(on)}$	drain-source on-state resistance	$T_j = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$	5.3	6.3	mΩ
		$T_j = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$	5.5	6.7	mΩ
		$T_j = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$	4.8	5.8	mΩ

6. Limiting values

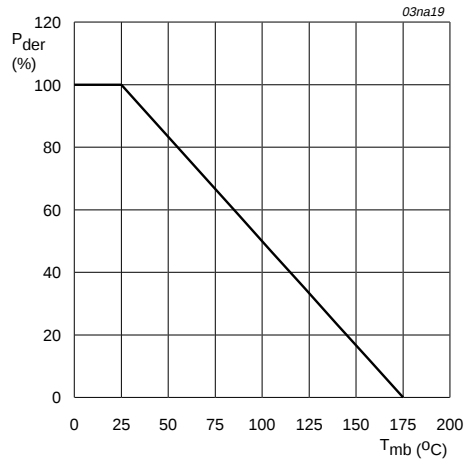
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		–	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	–	55	V
V_{GS}	gate-source voltage (DC)		–	±15	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2 and 3	[1] –	154	A
			[2] –	75	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2	[2] –	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	–	616	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	–	300	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	[1] –	154	A
			[2] –	75	A
I_{DRM}	pulsed reverse drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	616	A
Avalanche ruggedness					
W_{DSS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 75\text{ A}$; $V_{DS} \leq 55\text{ V}$; $V_{GS} = 5\text{ V}$; $R_{GS} = 50\text{ }\Omega$; starting $T_{mb} = 25\text{ °C}$	–	1.1	J

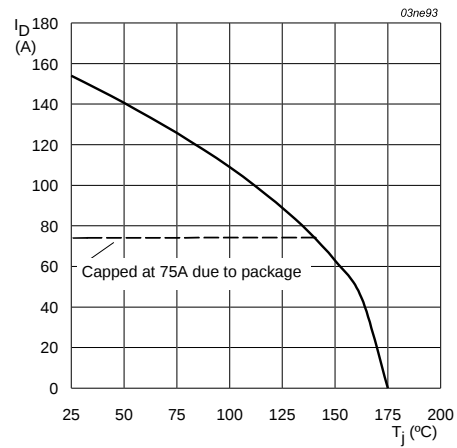
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

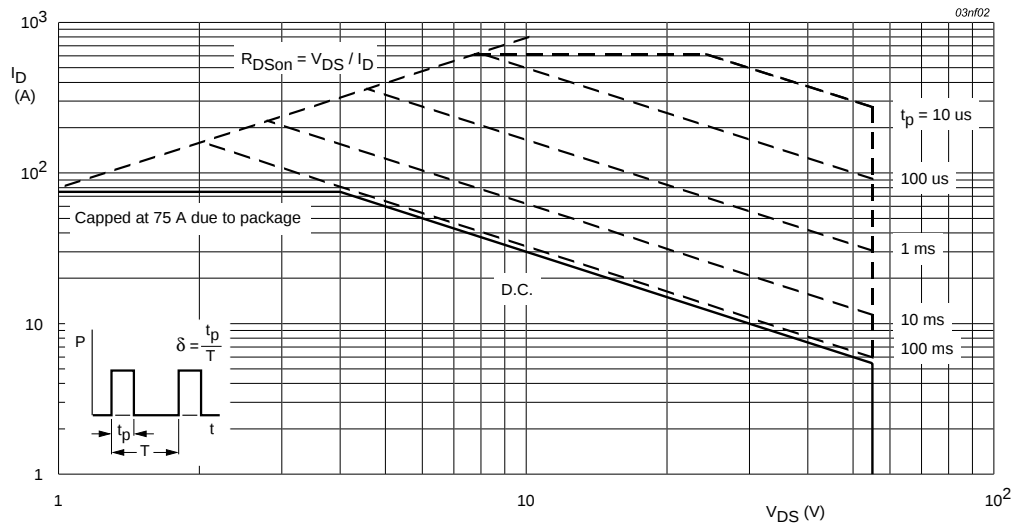
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25$ °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 and SOT226 packages	60	K/W
		mounted on printed circuit board; minimum footprint; SOT404 package	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	0.5	K/W

7.1 Transient thermal impedance

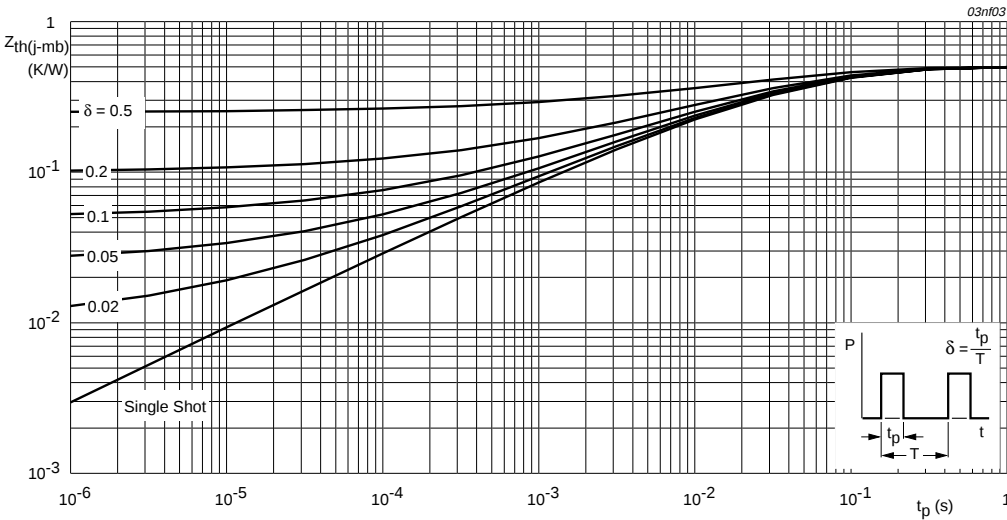


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

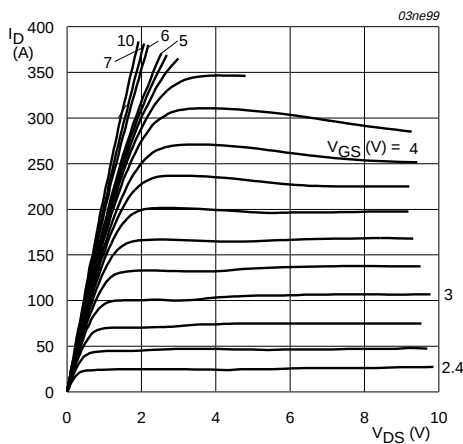
Table 5: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V				
		T _j = 25 °C	55	–	–	V
		T _j = –55 °C	50	–	–	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9				
		T _j = 25 °C	1	1.5	2	V
		T _j = 175 °C	0.5	–	–	V
		T _j = –55 °C	–	–	2.3	V
I _{DSS}	drain-source leakage current	V _{DS} = 55 V; V _{GS} = 0 V				
		T _j = 25 °C	–	0.05	10	μA
		T _j = 175 °C	–	–	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	–	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; Figure 7 and 8				
		T _j = 25 °C	–	5.3	6.3	mΩ
		T _j = 175 °C	–	–	13.2	mΩ
		V _{GS} = 4.5 V; I _D = 25 A	–	–	6.7	mΩ
		V _{GS} = 10 V; I _D = 25 A	–	4.8	5.8	mΩ
Dynamic characteristics						
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V;	–	6500	8600	pF
C _{oss}	output capacitance	f = 1 MHz; Figure 12	–	1000	1200	pF
C _{rss}	reverse transfer capacitance		–	650	850	pF
t _{d(on)}	turn-on delay time	V _{DD} = 30 V; R _L = 1.2 Ω;	–	45	–	ns
t _r	rise time	V _{GS} = 5 V; R _G = 10 Ω	–	180	–	ns
t _{d(off)}	turn-off delay time		–	420	–	ns
t _f	fall time		–	235	–	ns
L _d	internal drain inductance	from drain lead 6 mm from package to centre of die	–	4.5	–	nH
		from contact screw on mounting base to centre of die SOT78	–	3.5	–	nH
		from upper edge of drain mounting base to centre of die SOT404 / SOT226	–	2.5	–	nH
L _s	internal source inductance	from source lead to source bond pad	–	7.5	–	nH

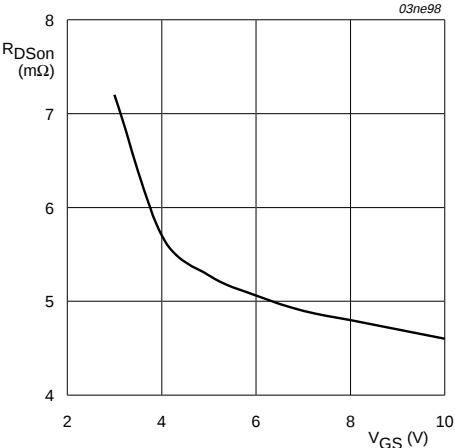
Table 5: Characteristics...continued
 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 30\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 15	—	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$	—	80	—	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$	—	200	—	nC



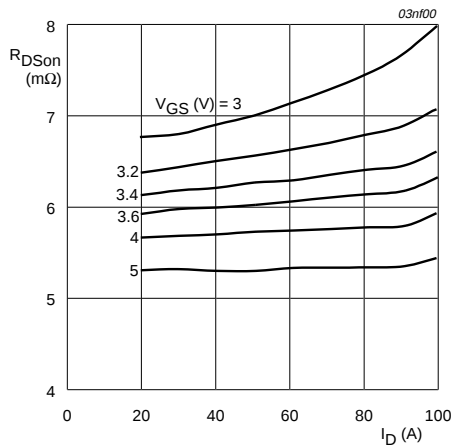
$T_j = 25\text{ }^{\circ}\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



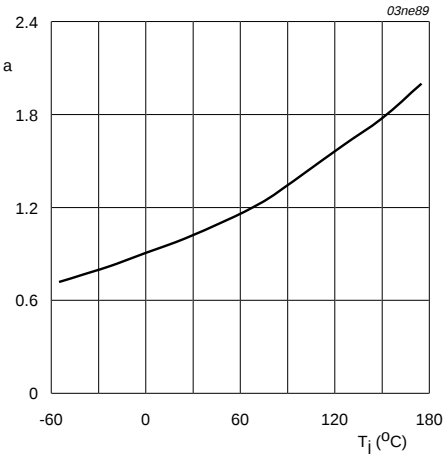
$T_j = 25\text{ }^{\circ}\text{C}$; $I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



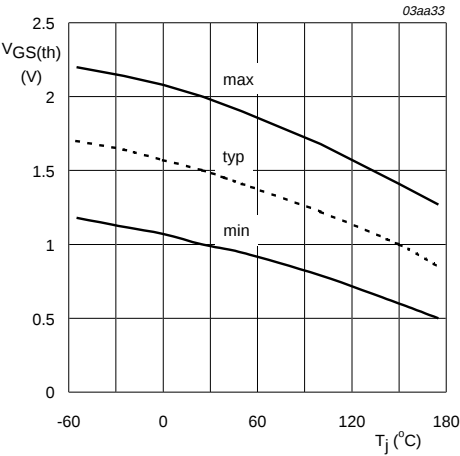
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



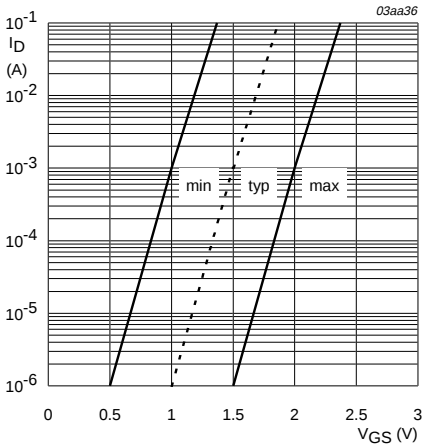
$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



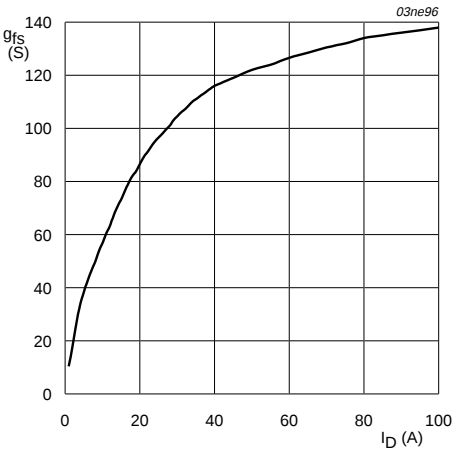
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



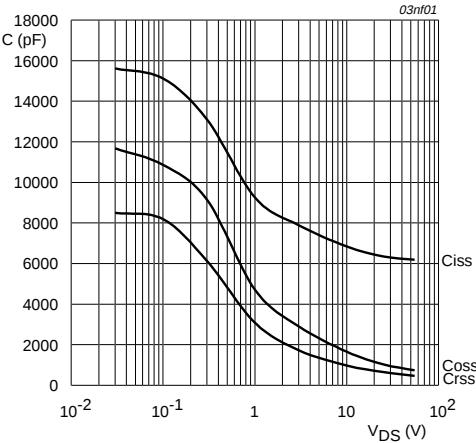
$T_j = 25 \text{ }^{\circ}\text{C}$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



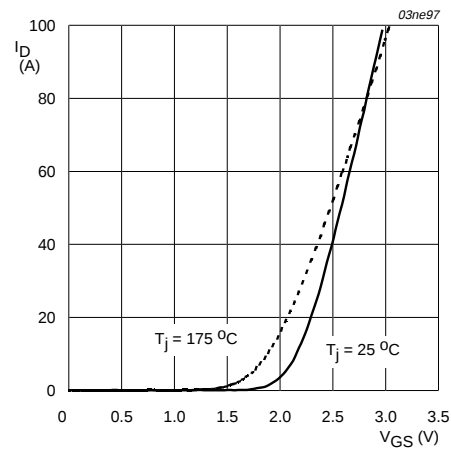
$T_j = 25 \text{ }^{\circ}\text{C}$; $V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



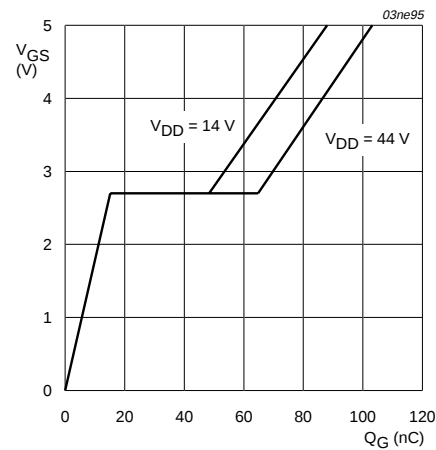
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



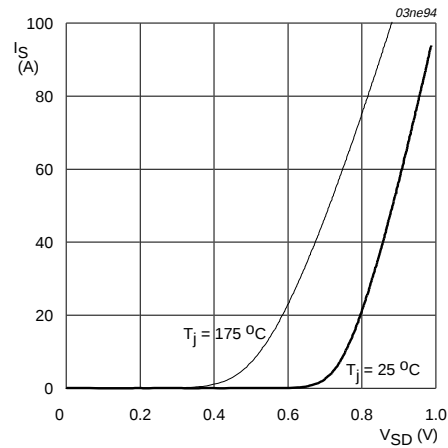
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



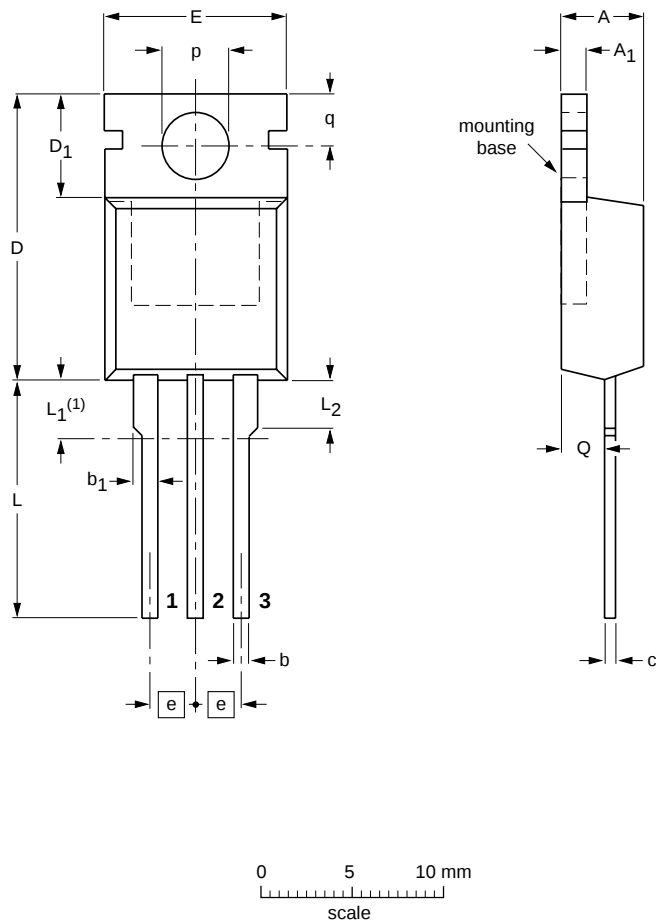
$V_{GS} = 0\text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

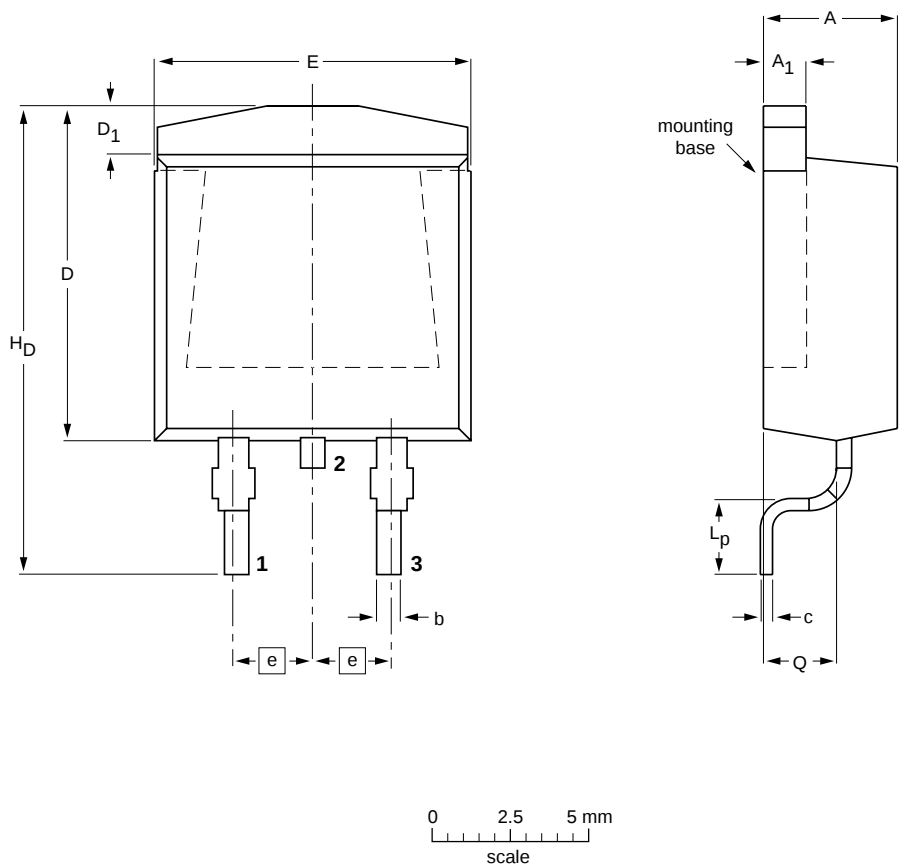
Note
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			00-09-07- 01-02-16

Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

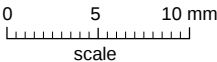
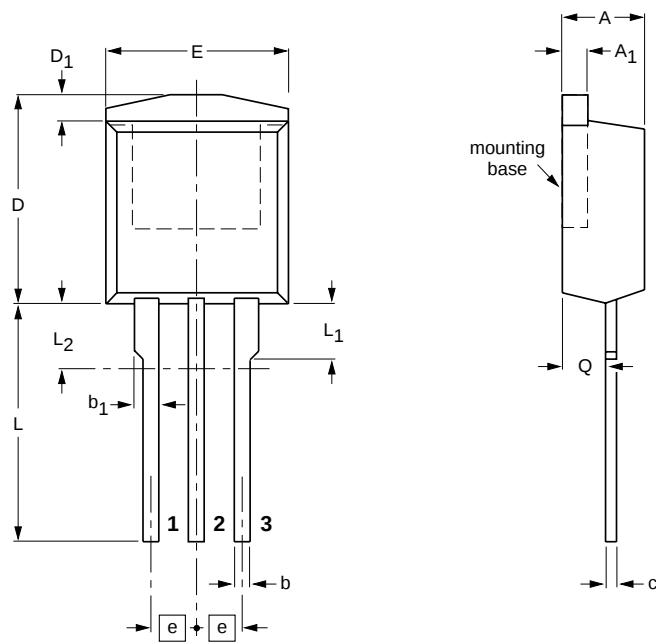
UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						99-06-25 01-02-12

Fig 17. SOT404 (D²-PAK).

Plastic single-ended package; low-profile 3 lead TO-220AB

SOT226



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁	L ₂ ⁽¹⁾ max	Q
mm	4.5 4.1	1.40 1.27	0.9 0.7	1.3 1.0	0.7 0.4	9.65 8.65	1.5 1.1	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	2.6 2.2

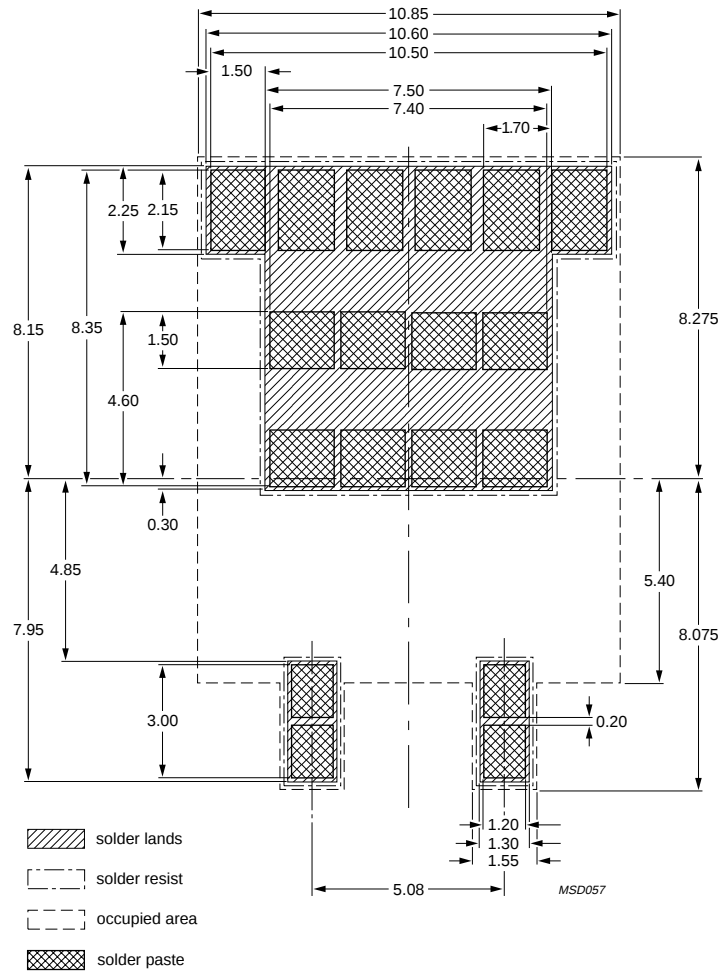
Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT226		low-profile 3-lead TO-220AB				99-05-27 99-09-13

Fig 18. SOT226 (I²-PAK).

10. Soldering



Dimensions in mm.

Fig 19. Reflow soldering footprint for SOT404.

11. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20010723	-	Product data; third version. Data sheet updated to Data Builder Two format, with the addition of SOT226 part.
02	19991202	-	Product Specification; second version
01	19981011	-	Product Specification; initial version

12. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Argentina: see South America

Australia: Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Tel. +43 160 101, Fax. +43 160 101 1210

Belarus: Tel. +375 17 220 0733, Fax. +375 17 220 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Tel. +359 268 9211, Fax. +359 268 9102

Canada: Tel. +1 800 234 7381

China/Hong Kong: Tel. +852 2 319 7888, Fax. +852 2 319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Tel. +45 3 288 2636, Fax. +45 3 157 0044

Finland: Tel. +358 961 5800, Fax. +358 96 158 0920

France: Tel. +33 1 4728 6600, Fax. +33 1 4728 6638

Germany: Tel. +49 40 23 5360, Fax. +49 402 353 6300

Hungary: Tel. +36 1 382 1700, Fax. +36 1 382 1800

India: Tel. +91 22 493 8541, Fax. +91 22 493 8722

Indonesia: see Singapore

Ireland: Tel. +353 17 64 0000, Fax. +353 17 64 0200

Israel: Tel. +972 36 45 0444, Fax. +972 36 49 1007

Italy: Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Tel. +81 33 740 5130, Fax. +81 3 3740 5057

Korea: Tel. +82 27 09 1412, Fax. +82 27 09 1415

Malaysia: Tel. +60 37 50 5214, Fax. +60 37 57 4880

Mexico: Tel. +9-5 800 234 7381

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For all other countries apply to: Philips Semiconductors,
Marketing Communications,
Building BE, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 272 4825

Netherlands: Tel. +31 40 278 2785, Fax. +31 40 278 8399

New Zealand: Tel. +64 98 49 4160, Fax. +64 98 49 7811

Norway: Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Tel. +63 28 16 6380, Fax. +63 28 17 3474

Poland: Tel. +48 22 5710 000, Fax. +48 22 5710 001

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Russia: Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Tel. +34 33 01 6312, Fax. +34 33 01 4107

Sweden: Tel. +46 86 32 2000, Fax. +46 86 32 2745

Switzerland: Tel. +41 14 88 2686, Fax. +41 14 81 7730

Taiwan: Tel. +886 22 134 2451, Fax. +886 22 134 2874

Thailand: Tel. +66 23 61 7910, Fax. +66 23 98 3447

Turkey: Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: Tel. +381 11 3341 299, Fax. +381 11 3342 553

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(SCA72)

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