

BUK9MHH-65PNN

Dual TrenchPLUS FET Logic Level FET

Rev. 02 — 19 May 2010

Objective data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance Architecture (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

1.4 Quick reference data

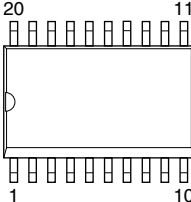
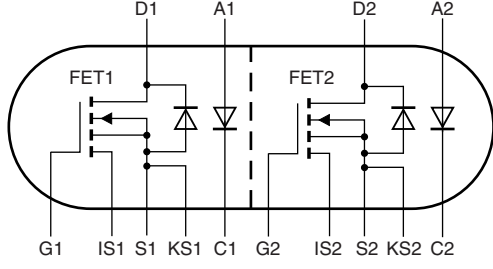
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; see Figure 15 ; see Figure 16	-	9.8	11.5	mΩ
I_D/I_{sense}	ratio of drain current to sense current	$T_j = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 17	6193	6881	7569	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	65	-	-	V



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1	 <p>SOT163-1 (SO20)</p>	 <p>003aaa745</p>
2	IS1	current sense 1		
3	D1	drain		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9MHH-65PNN	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2						
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
V_{GS}	gate-source voltage		-15	-	15	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{sp} = 25\text{ °C}$; see Figure 1 [1][2]	-	-	15	A
		$V_{GS} = 5\text{ V}$; $T_{sp} = 100\text{ °C}$; see Figure 1 [1][2]	-	-	9.5	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 4	-	-	319	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	-	5	W
T_{stg}	storage temperature		-55	-	150	°C
T_j	junction temperature		-55	-	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	-	100	V
FET1 and FET2 source-drain diode						
I_S	source current	$T_{sp} = 25\text{ °C}$	[1][3]	-	7	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{sp} = 25\text{ °C}$	-	-	319	A
FET1 and FET2 avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 15.1\text{ A}$; $V_{sup} = 65\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; see Figure 3 [4][5][6]	-	-	878	mJ
FET1 and FET2 electrostatic discharge						
V_{ESD}	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; all pins	-	-	0.15	kV
		HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; pins 8, 11 and 15 to pins 6, 7, 12, 13 and 14 shorted	-	-	4	kV
		HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted	-	-	4	kV

[1] Single device conducting.

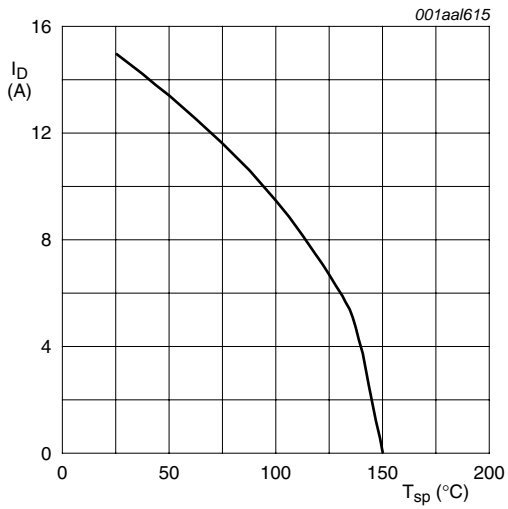
[2] Continuous current is limited by package.

[3] Current is limited by chip power dissipation rating.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

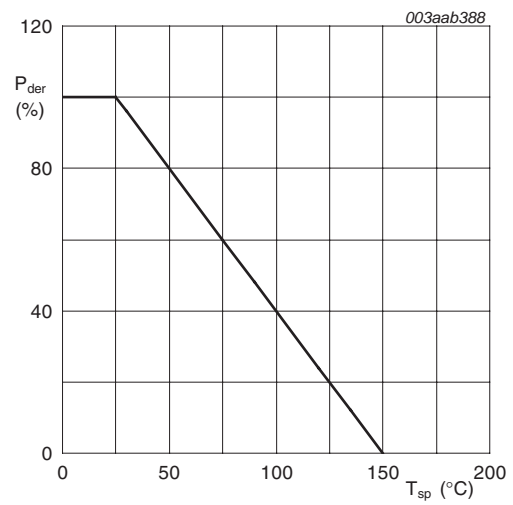
[5] Repetitive rating defined in avalanche rating figure.

[6] Refer to application note AN10273 for further information.



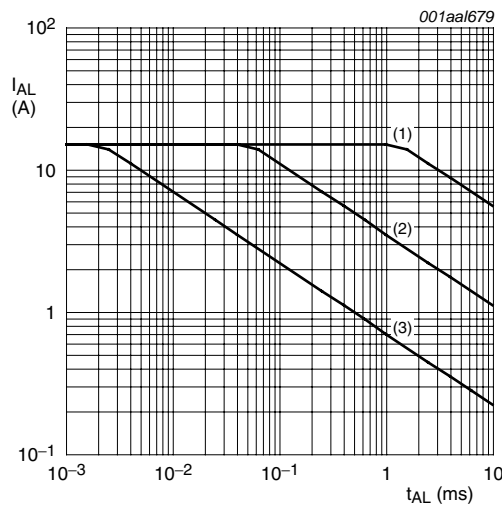
$V_{GS} \geq 5V$

Fig 1. Continuous drain current as a function of solder point temperature, FET1 and FET2



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature, FET1 and FET2



- (1) Single-pulse; $T_j = 25^{\circ}C$.
- (2) Single-pulse; $T_j = 150^{\circ}C$.
- (3) Repetitive.

Fig 3. Single-Pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

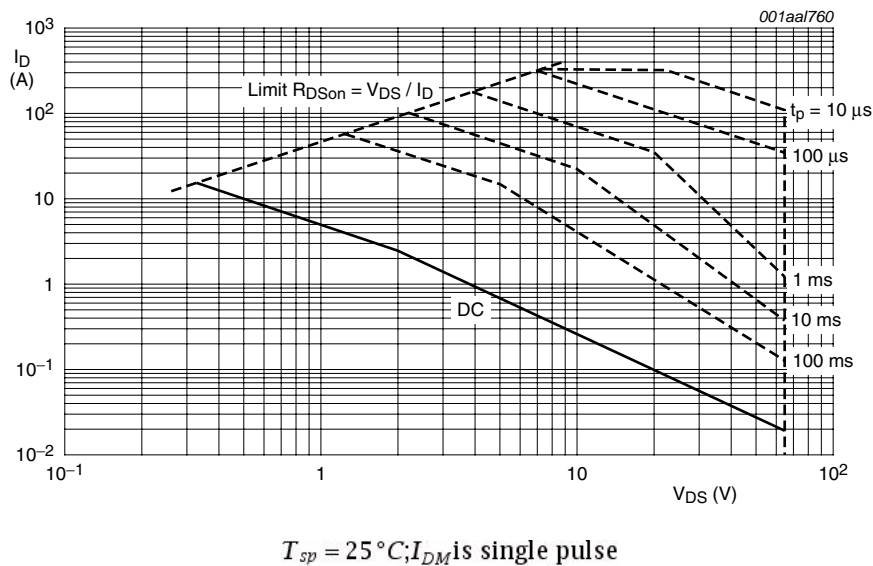
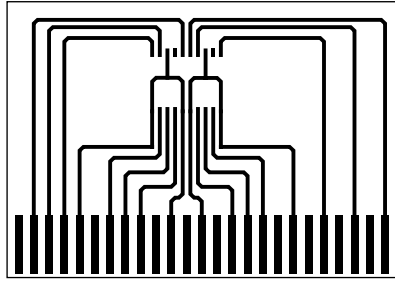


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

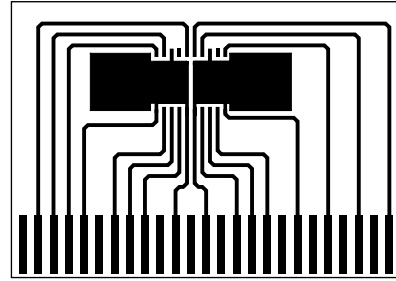
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	25	K/W
		FET2	-	-	25	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; both channels conducting; zero heat sink area; see Figure 5	-	73	-	K/W
		mounted on a printed-circuit board; both channels conducting; 200 mm ² copper heat sink area; see Figure 6	-	60	-	K/W
		mounted on a printed-circuit board; both channels conducting; 400 mm ² copper heat sink area; see Figure 7	-	51	-	K/W
		mounted on a printed-circuit board; one channel conducting; zero heat sink area; see Figure 5	-	105	-	K/W
		mounted on a printed-circuit board; one channel conducting; 200 mm ² copper heat sink area; see Figure 6	-	90	-	K/W
		mounted on a printed-circuit board; one channel conducting; 400 mm ² copper heat sink area; see Figure 7	-	70	-	K/W



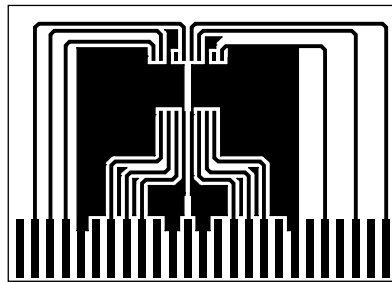
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Fig 5. PCB used for thermal tests; zero heat sink area



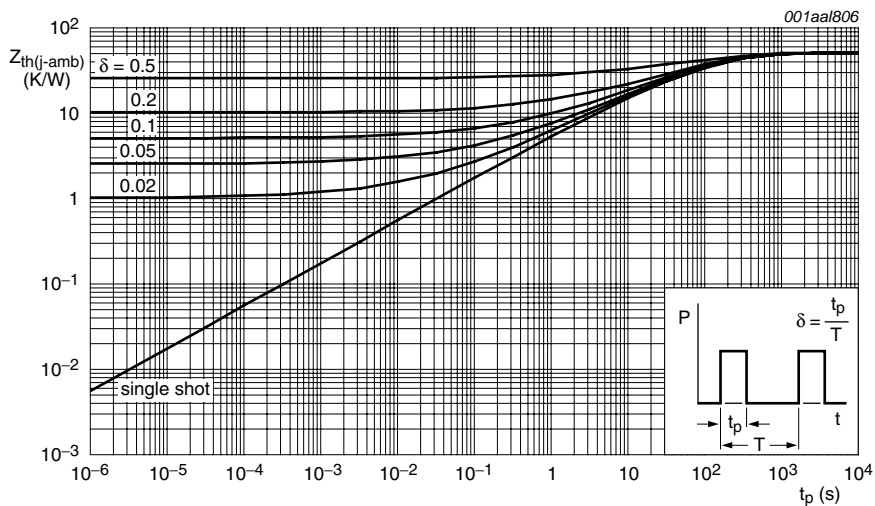
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Fig 6. PCB used for thermal tests; heat sink area 200 mm²



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Fig 7. PCB used for thermal tests; heat sink area 400 mm²



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Fig 8. Transient thermal impedance from junction to ambient as a function of pulse duration

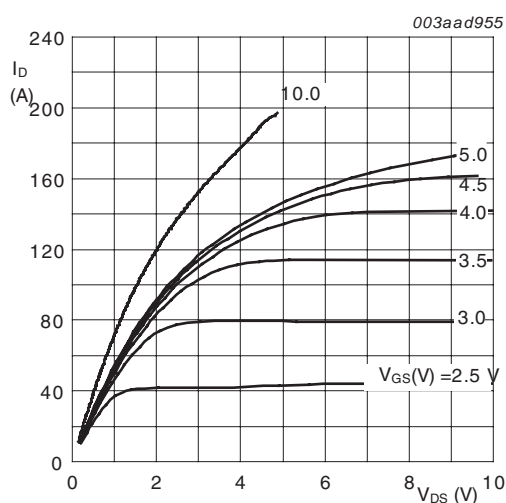
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	65	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	59	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13 ; see Figure 14	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 13 ; see Figure 14	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 13 ; see Figure 14	-	-	2.3	V
I_{DSS}	drain leakage current	$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	3	μA
		$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	125	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	300	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 15 ; see Figure 16	-	-	12.6	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 15 ; see Figure 16	-	9.8	11.5	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 15 ; see Figure 16	-	-	21.9	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 15 ; see Figure 16	-	-	10.6	m Ω
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 17	6193	6881	7569	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250 \mu\text{A}; 25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C};$ see Figure 18	-5.4	-5.7	-6	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250 \mu\text{A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 18	2.855	2.9	2.945	V

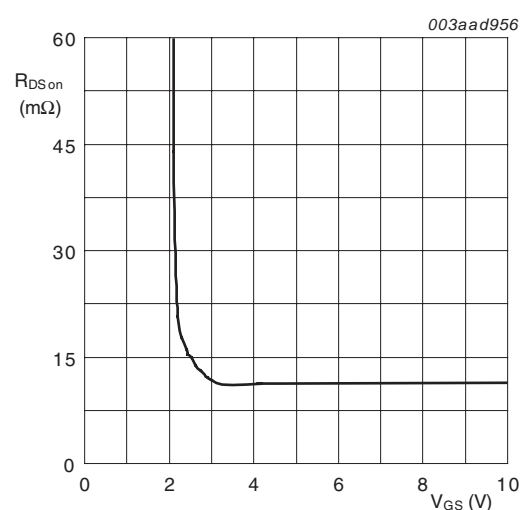
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 dynamic characteristics						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10 \text{ A}$; $V_{DS} = 52 \text{ V}$; $V_{GS} = 5 \text{ V}$; see Figure 19	-	44.6	-	nC
Q_{GS}	gate-source charge		-	7.22	-	nC
Q_{GD}	gate-drain charge		-	16.8	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}$; $V_{DS} = 25 \text{ V}$; $f = 1 \text{ MHz}$;	-	3643	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$; see Figure 20	-	496	-	pF
C_{rss}	reverse transfer capacitance		-	186	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 30 \text{ V}$; $R_L = 3 \text{ } \Omega$; $V_{GS} = 5 \text{ V}$;	-	40	-	ns
t_r	rise time	$R_{G(\text{ext})} = 10 \text{ } \Omega$	-	76	-	ns
$t_{d(\text{off})}$	turn-off delay time	$V_{DS} = 30 \text{ V}$; $V_{GS} = 5 \text{ V}$; $R_{G(\text{ext})} = 10 \text{ } \Omega$	-	188	-	ns
t_f	fall time	$V_{DS} = 30 \text{ V}$; $R_L = 3 \text{ } \Omega$; $V_{GS} = 5 \text{ V}$; $R_{G(\text{ext})} = 10 \text{ } \Omega$	-	108	-	ns
L_D	internal drain inductance	from pin to center of die	-	0.9	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	2	-	nH
FET1 and FET2 source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 21	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 10 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$;	-	54	-	ns
Q_r	recovered charge	$V_{GS} = -10 \text{ V}$; $V_{DS} = 30 \text{ V}$	-	0.131	-	nC



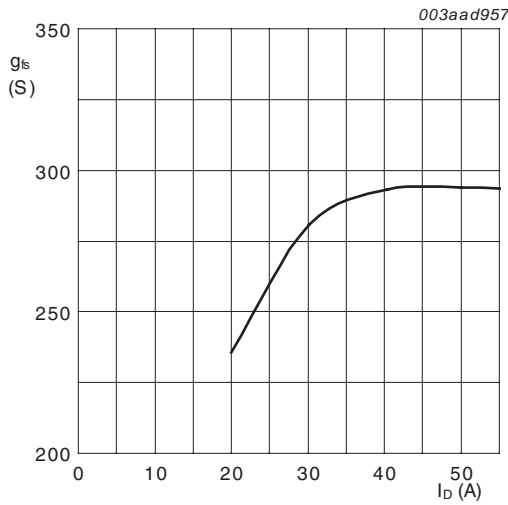
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 300 \mu\text{s}$

Fig 9. Output characteristics: drain current as a function of drain current; typical values, FET1 and FET2



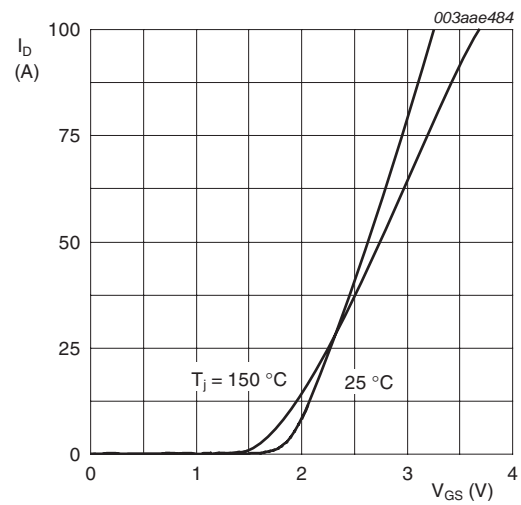
$T_j = 25 \text{ }^\circ\text{C}$; $I_D = 10 \text{ A}$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2



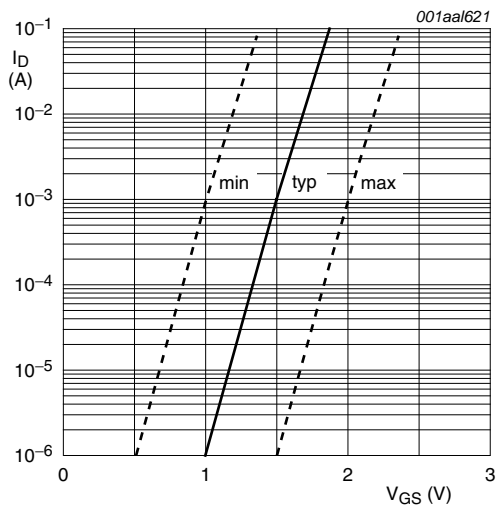
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 11. Forward transconductance as a function of drain current; typical values, FET1 and FET2



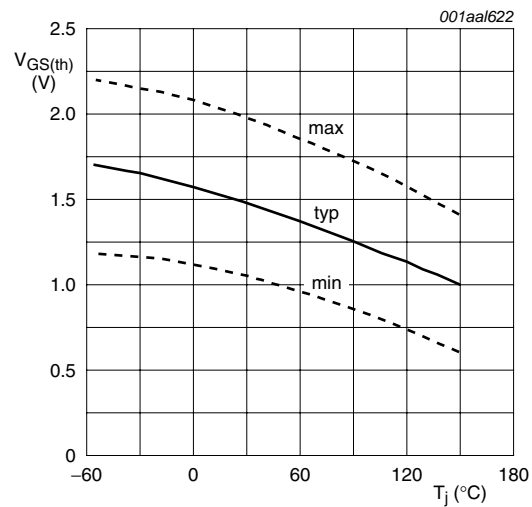
$V_{DS} = 25\text{V}$

Fig 12. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2



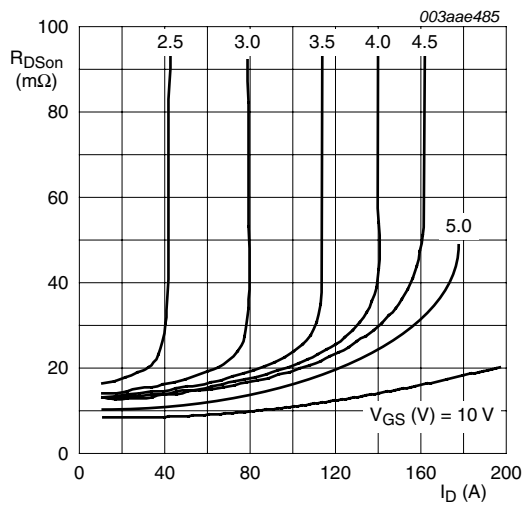
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 13. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2



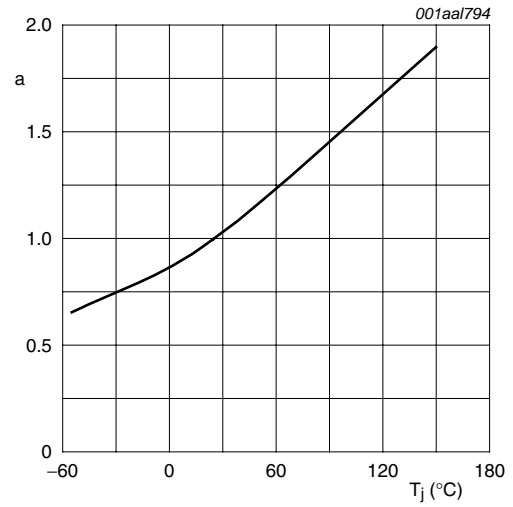
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 14. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2



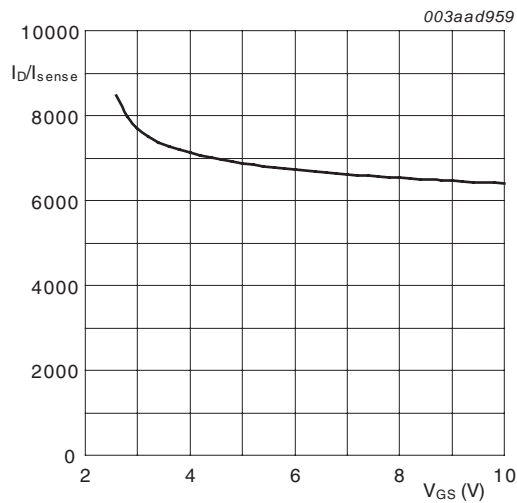
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

Fig 15. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



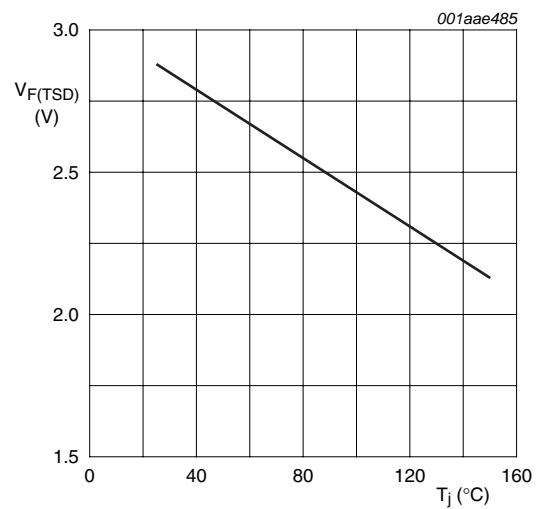
$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 16. Normalized Drain-source on-state resistance factor as a function of junction temperature



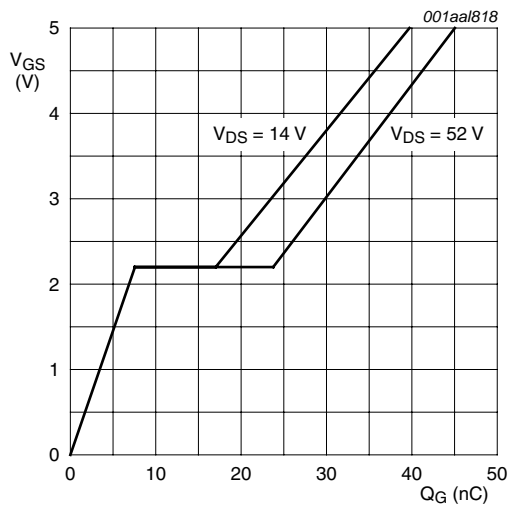
$T_j = 25^\circ\text{C}; I_D = 5\text{A}$

Fig 17. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1 and FET2



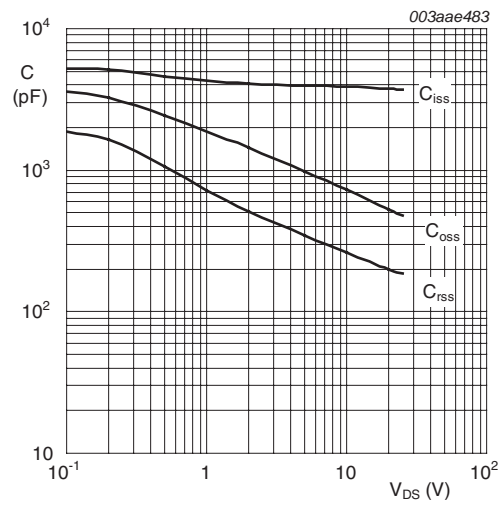
$I_F = 250\mu\text{A}$

Fig 18. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2



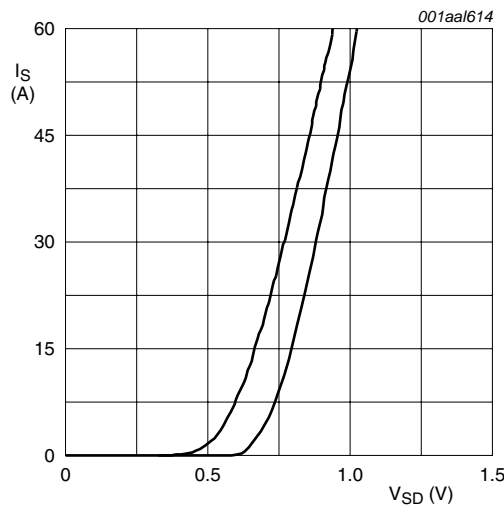
$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

Fig 19. Gate-source voltage as a function of turn-on gate charge; typical values, FET1 and FET2



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 20. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0\text{V}$

Fig 21. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

7. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

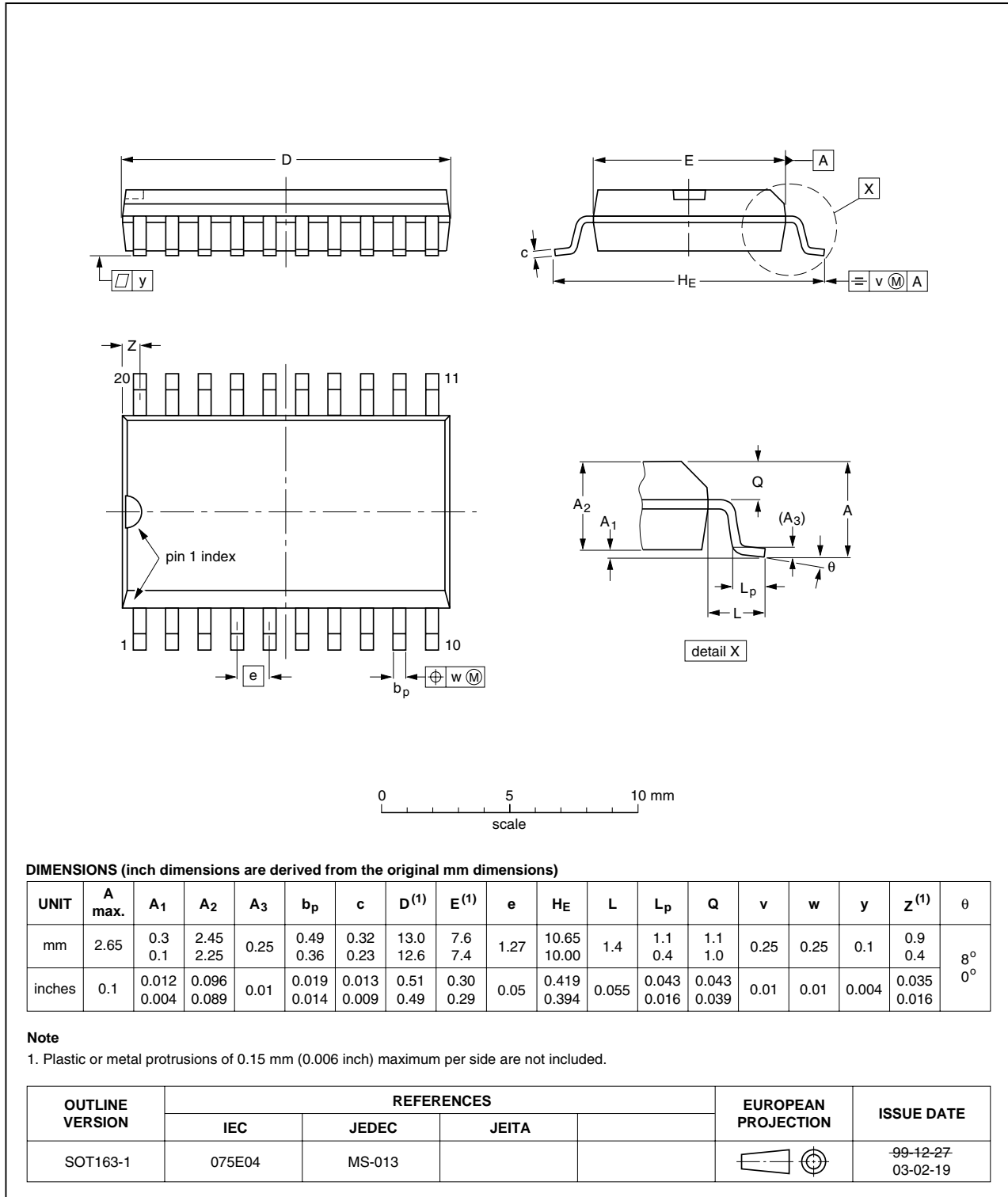


Fig 22. Package outline SOT163-1 (SO20)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MHH-65PNN v.2	20100519	Objective data sheet	-	BUK9MHH-65PNN_1
Modifications:	• Various changes to content.			
BUK9MHH-65PNN_1	20100511	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 19 May 2010

Document identifier: BUK9MHH-65PNN