BUK9MNN-65PKK

Dual TrenchPLUS FET Logic Level FET

Rev. 01 — 27 May 2010 | Objective data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

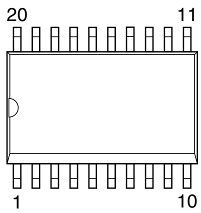
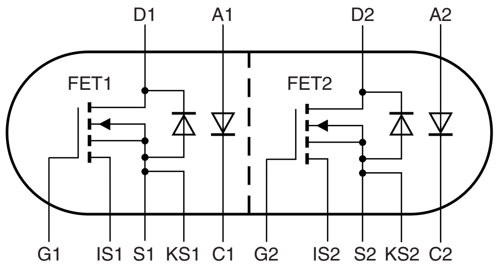
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; see Figure 16; see Figure 17	-	30.6	36	mΩ
I_D/I_{sense}	ratio of drain current to sense current	T_j = 25 °C; V_{GS} = 5 V; see Figure 18	2242	2491	2740	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	65	-	-	V

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1	 **SOT163-1 (SO20)**	 *003aaa745*
2	IS1	current sense 1		
3	D1	drain		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9MNN-65PKK	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
FET1 and FET2							
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	-	65	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ; 25 °C ≤ T_j ≤ 150 °C		-	-	65	V
V_{GS}	gate-source voltage			-15	-	15	V
I_D	drain current	V_{GS} = 5 V; T_{sp} = 25 °C; see Figure 1	[1]	-	-	7.1	A
		V_{GS} = 5 V; T_{sp} = 100 °C; see Figure 1	[2][1]	-	-	4.5	A
I_{DM}	peak drain current	T_{sp} = 25 °C; single pulse; t_p ≤ 10 µs; see Figure 4		-	-	96.6	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 2		-	-	3.57	W
T_{stg}	storage temperature			-55	-	150	°C
T_j	junction temperature			-55	-	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage			-	-	100	V
FET1 and FET2 source-drain diode							
I_S	source current	T_{sp} = 25 °C	[2][1]	-	-	5	A
I_{SM}	peak source current	single pulse; t_p ≤ 10 µs; T_{sp} = 25 °C		-	-	96.6	A
FET1 and FET2 avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 13.6 A; V_{sup} = 65 V; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; see Figure 3	[3][4][5]	-	-	165	mJ
FET1 and FET2 electrostatic discharge							
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; all pins		-	-	0.15	kV
		HBM; C = 100 pF; R = 1.5 kΩ; pins 8, 11 and 15 to pins 6, 7, 12, 13 and 14 shorted		-	-	4	kV
		HBM; C = 100 pF; R = 1.5 kΩ; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted		-	-	4	kV

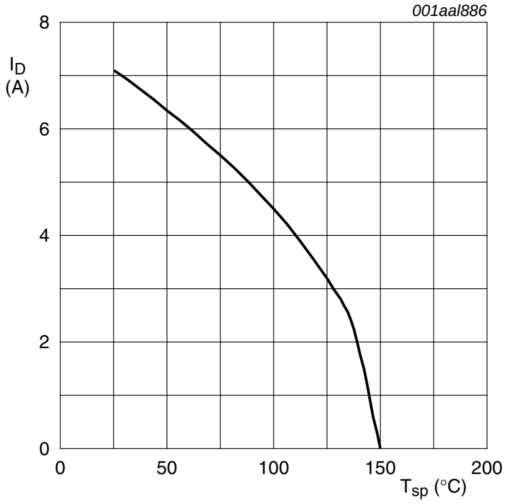
[1] Current is limited by package.

[2] Single device conducting.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

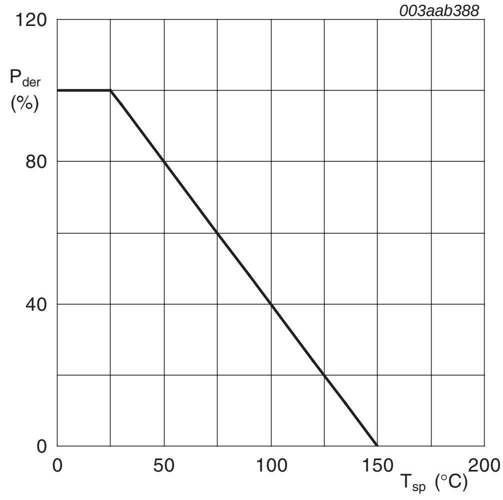
[4] Repetitive rating defined in avalanche rating figure.

[5] Refer to application note AN10273 for further information.



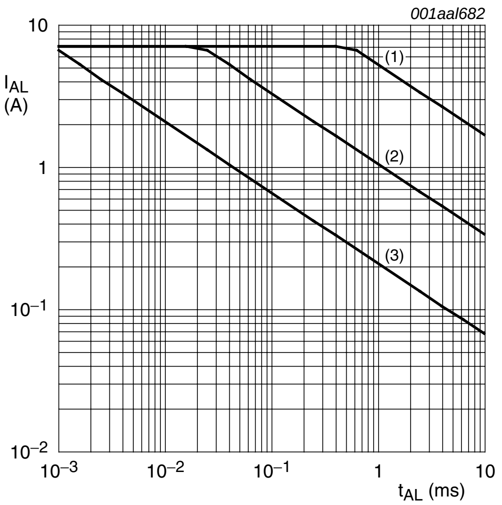
$$V_{GS} \geq 5V$$

Fig 1. Continuous drain current as a function of solder point temperature, FET1 and FET2



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature, FET1 and FET2

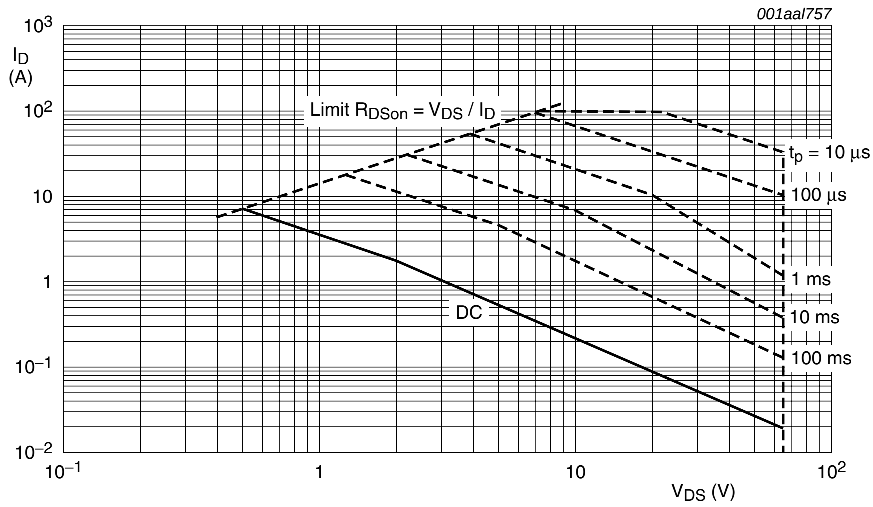


(1) Single-pulse; $T_j = 25\,°C$.

(2) Single-pulse; $T_j = 150\,°C$.

(3) Repetitive.

Fig 3. Single-Pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



$T_{sp} = 25\,°C; I_{DM}$ is single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	35	K/W
		FET2	-	-	35	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; both channels conducting; zero heat sink area; see Figure 5; see Figure 6	-	73	-	K/W
		mounted on a printed-circuit board; both channels conducting; 200 mm² copper heat sink area; see Figure 7; see Figure 6	-	60	-	K/W
		mounted on a printed-circuit board; both channels conducting; 400 mm² copper heat sink area; see Figure 8; see Figure 6	-	51	-	K/W
		mounted on a printed-circuit board; one channel conducting; zero heat sink area; see Figure 5; see Figure 6	-	105	-	K/W
		mounted on a printed-circuit board; one channel conducting; 200 mm² copper heat sink area; see Figure 7; see Figure 6	-	90	-	K/W
		mounted on a printed-circuit board; one channel conducting; 400 mm² copper heat sink area; see Figure 8; see Figure 6	-	70	-	K/W

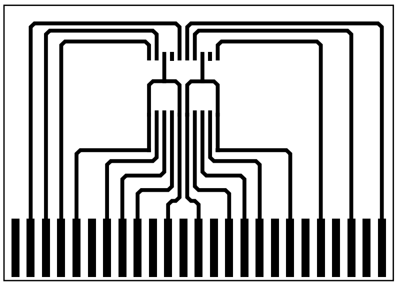


Fig 5. PCB used for thermal tests; zero heat sink area

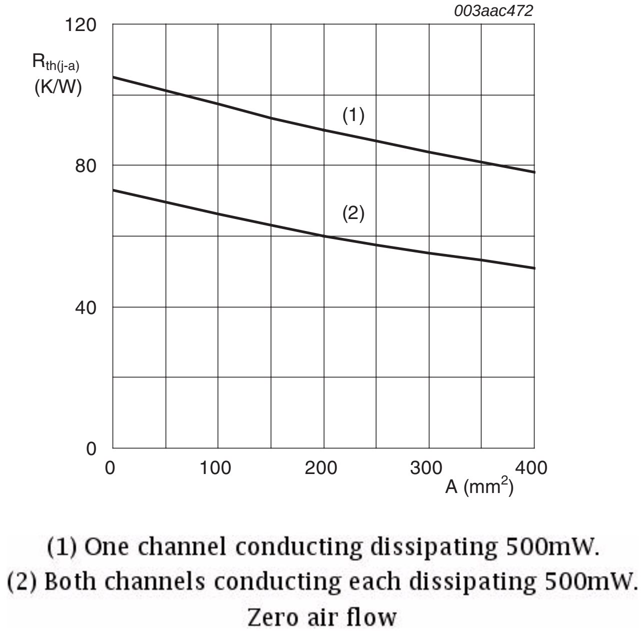


Fig 6. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area

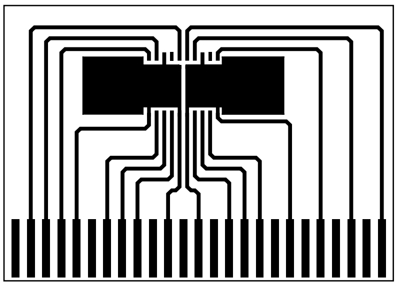


Fig 7. PCB used for thermal tests; heat sink area 200 mm²

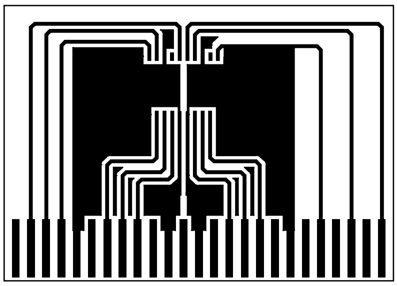


Fig 8. PCB used for thermal tests; heat sink area 400 mm²

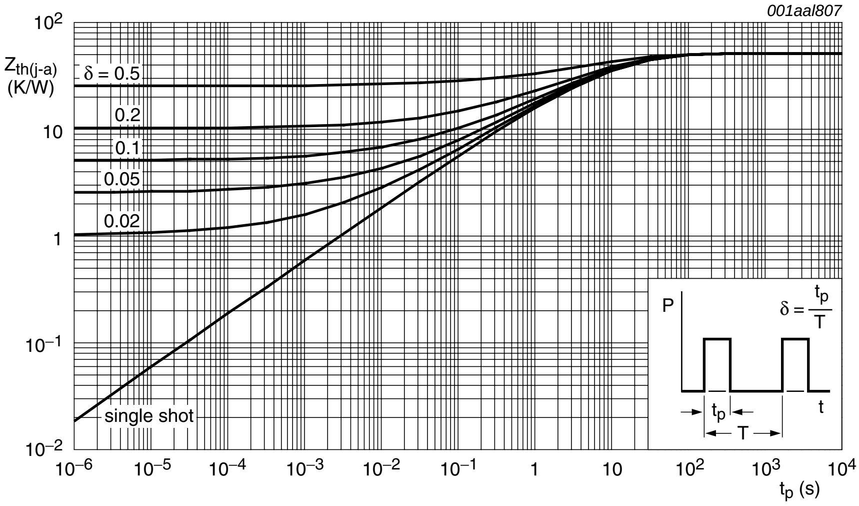


Fig 9. Transient thermal impedance from junction to ambient as a function of pulse duration, FET1 and FET2

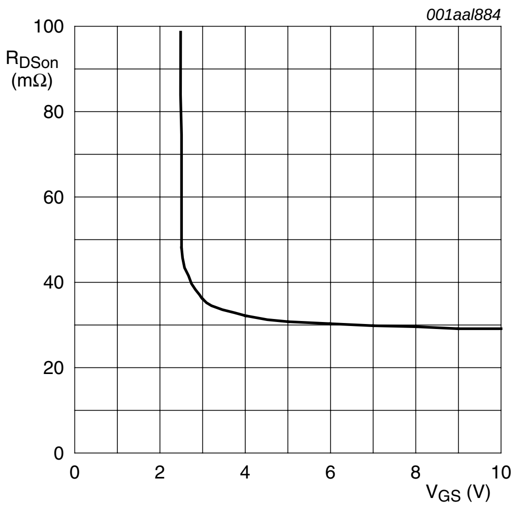
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	65	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	59	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 14; see Figure 15	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 14; see Figure 15	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 14; see Figure 15	-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 52 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	3	µA
		V_{DS} = 52 V; V_{GS} = 0 V; T_j = 150 °C	-	-	125	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 15 V; T_j = 25 °C	-	2	300	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C; see Figure 16; see Figure 17	-	-	39.8	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; see Figure 16; see Figure 17	-	30.6	36	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 150 °C; see Figure 16; see Figure 17	-	-	70.8	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; see Figure 16; see Figure 17	-	-	32.8	mΩ
I_D/I_{sense}	ratio of drain current to sense current	V_{GS} = 5 V; T_j = 25 °C; see Figure 18	2242	2491	2740	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	I_F = 250 µA; 25 °C ≤ T_j ≤ 150 °C; see Figure 19	-5.4	-5.7	-6	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	I_F = 250 µA; T_j = 25 °C; see Figure 19	2.855	2.9	2.945	V
FET1 and FET2 dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 52 V; V_{GS} = 5 V; see Figure 20	-	15	-	nC
Q_{GS}	gate-source charge		-	3.9	-	nC
Q_{GD}	gate-drain charge		-	5.9	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 21	-	1180	-	pF
C_{oss}	output capacitance		-	169	-	pF
C_{rss}	reverse transfer capacitance		-	56	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 6 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	20	-	ns
t_r	rise time		-	25	-	ns
$t_{d(off)}$	turn-off delay time		-	86	-	ns
t_f	fall time		-	50	-	ns
L_D	internal drain inductance	from pin to center of die	-	0.9	-	nH

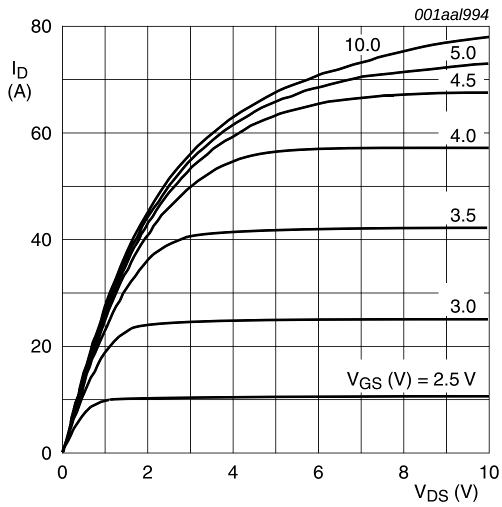
Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_S	internal source inductance	from source lead to source bonding pad	-	2	-	nH
FET1 and FET2 source-drain diode						
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 22	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V	-	39	-	ns
Q_r	recovered charge		-	0.073	-	nC



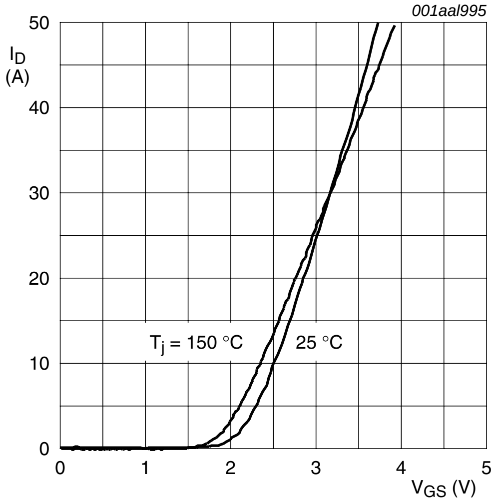
$T_j = 25°C; I_D = 5A$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



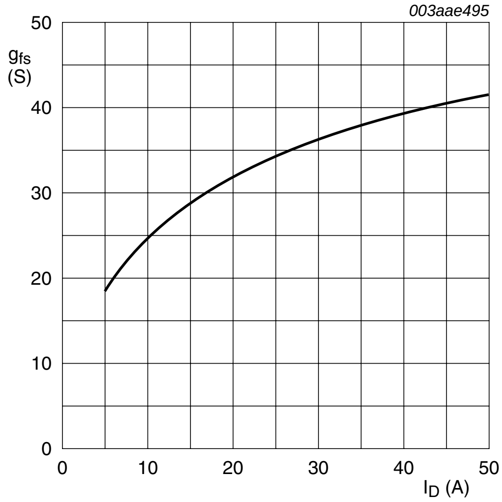
$T_j = 25°C$

Fig 11. Output characteristics: drain current as a function of drain-source voltage; typical values



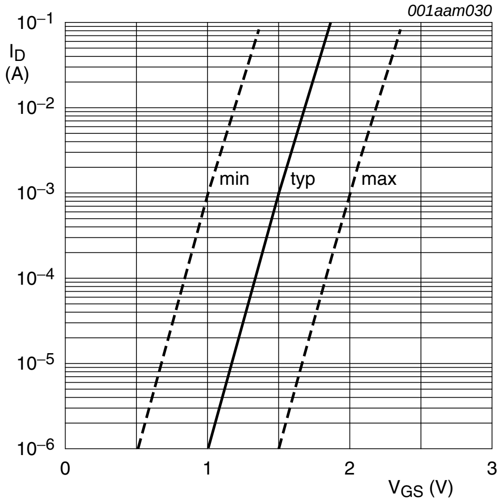
$V_{DS} = 25V$

Fig 12. Transfer characteristics: drain current as a function of gate-source voltage; typical values



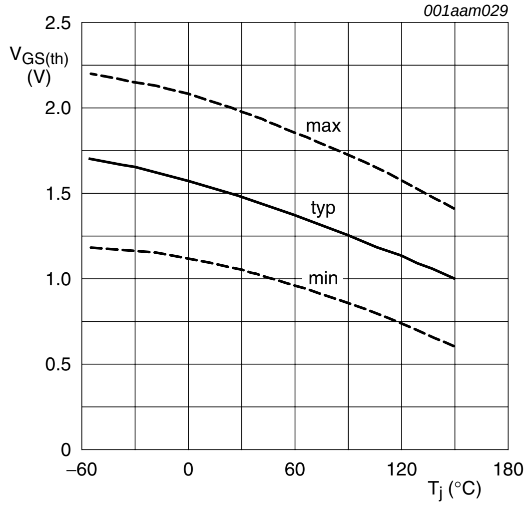
$T_j = 25°C; V_{DS} = 25V$

Fig 13. Forward transconductance as a function of drain current; typical values



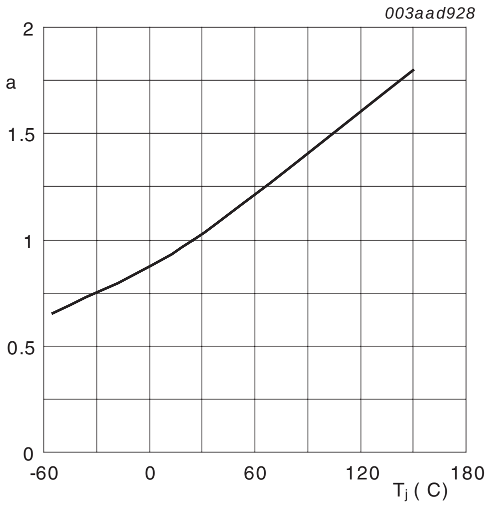
$$T_j = 25\,°C; V_{DS} = V_{GS}$$

Fig 14. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2



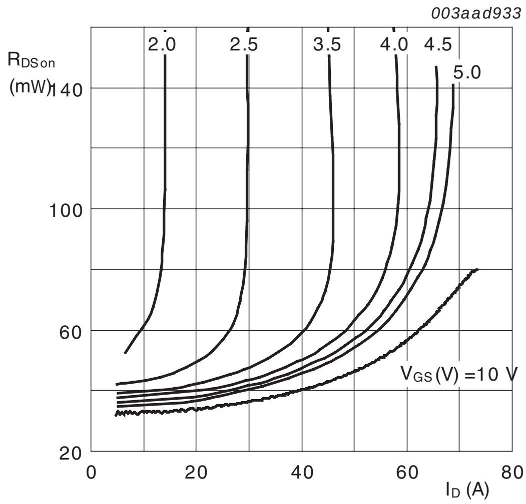
$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 15. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2



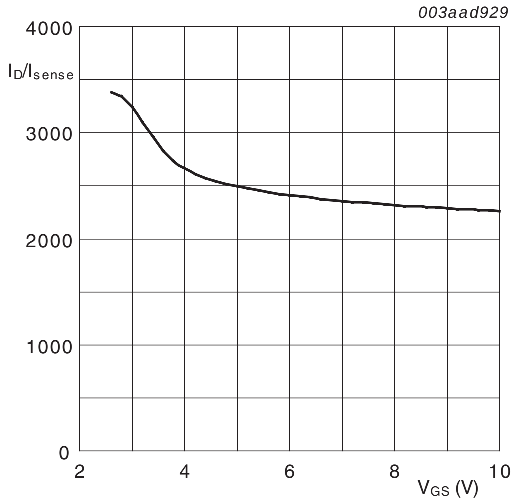
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 16. Normalized Drain-source on-state resistance factor as a function of junction temperature



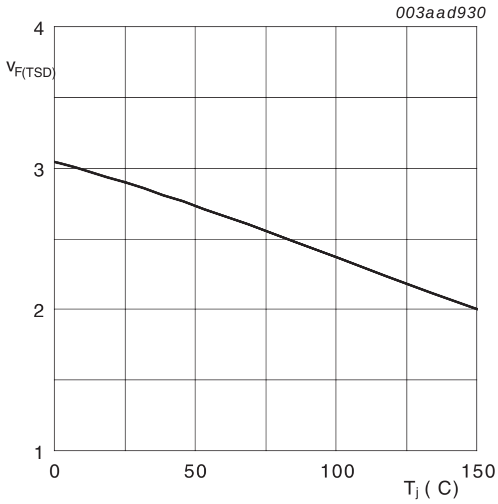
$$T_j = 25°C; t_p = 300\mu s$$

Fig 17. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



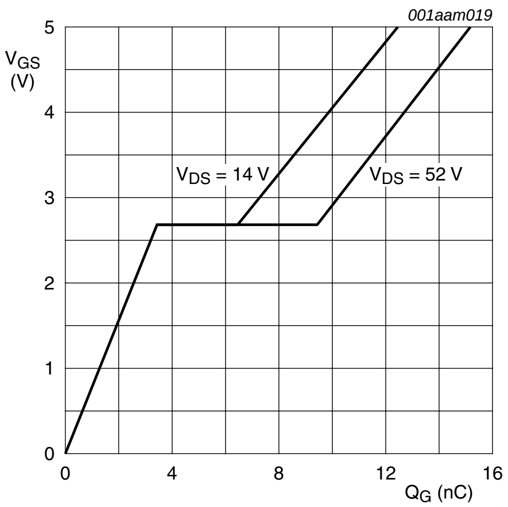
$T_j = 25\,°C;\ I_D = 5A$

Fig 18. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1 and FET2



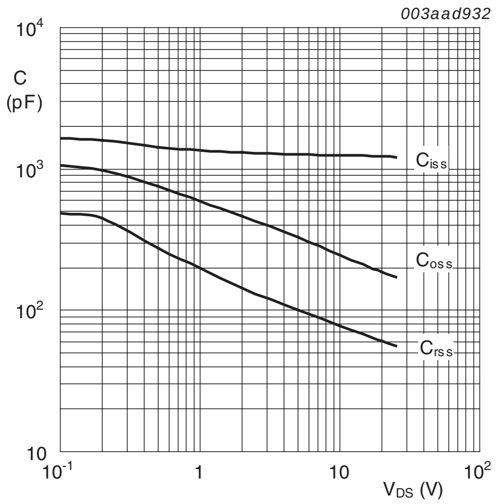
$I_F = 250\mu A$

Fig 19. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2



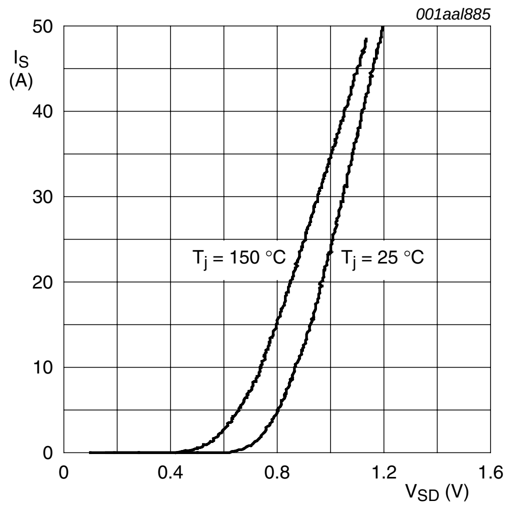
$T_j = 25\,°C; I_D = 5A$

Fig 20. Gate-source as a function of turn-on gate charge; typical values, FET1 and FET2



$V_{GS} = 0V; f = 1MHz$

Fig 21. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

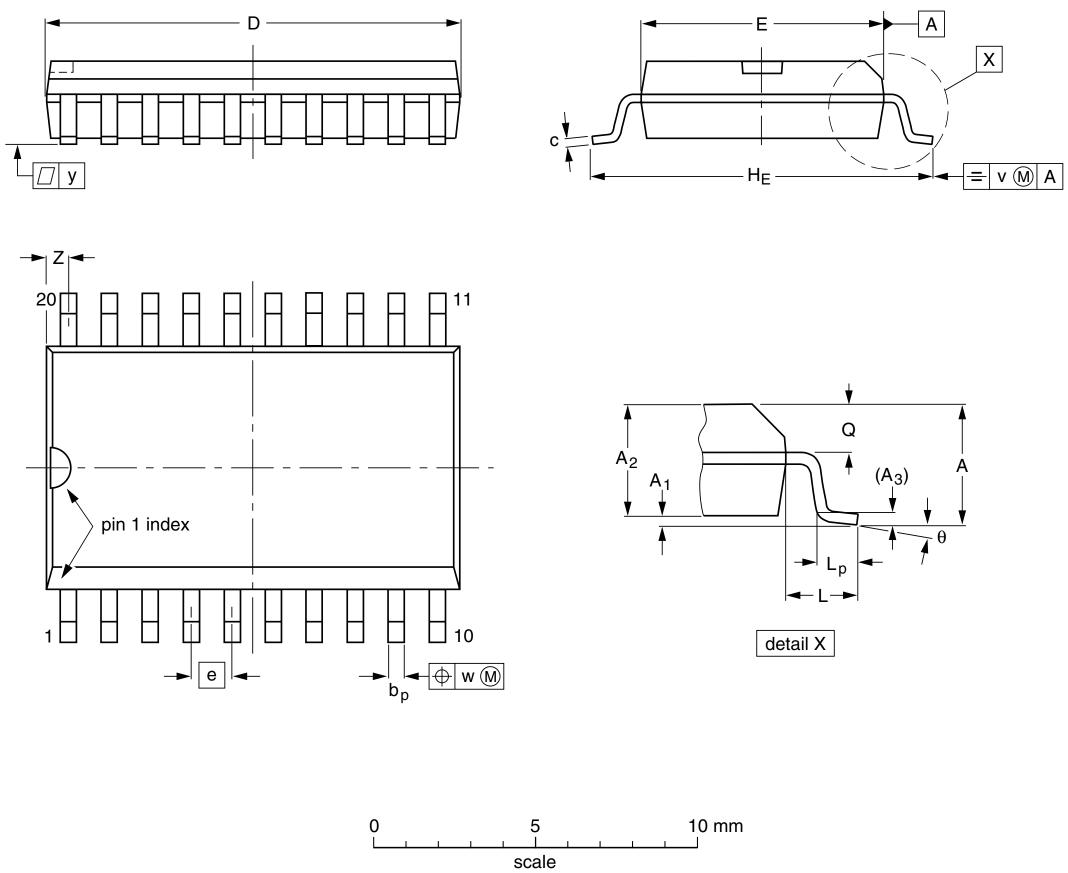


$V_{GS} = 0V$

Fig 22. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 23. Package outline SOT163-1 (SO20)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MNN-65PKK v.1	20100527	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

9.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding. Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Adelante, **Bitport**, **Bitsound**, **CoolFlux**, **CoReUse**, **DESFire**, **EZ-HV**, **FabKey**, **GreenChip**, **HiPerSmart**, **HITAG**, **I²C-bus** logo, **ICODE**, **I-CODE**, **ITEC**, **Labelution**, **MIFARE**, **MIFARE Plus**, **MIFARE Ultralight**, **MoReUse**, **QLPAK**, **Silicon Tuner**, **SiliconMAX**, **SmartXA**, **STARplug**, **TOPFET**, **TrenchMOS**, **TriMedia** and **UCODE** — are trademarks of NXP B.V.

HD Radio and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

11. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 May 2010

Document identifier: BUK9MNN-65PKK