

BUK9Y19-55B

N-channel TrenchMOS™ logic level FET

Rev. 01 — 28 May 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive (HPA) TrenchMOS™ technology.

1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Logic level compatible.

1.3 Applications

- Automotive systems
- Motors, lamps and solenoids
- 12 V and 24 V loads
- General purpose power switching.

1.4 Quick reference data

- $E_{DS(AL)S} \leq 91$ mJ
- $I_D \leq 40$ A
- $R_{DSon} = 16.3$ m Ω (typ)
- $P_{tot} \leq 75$ W.

2. Pinning information

Table 1: Pinning - SOT669 (LFPAK) simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBL286</p> <p>SOT669 (LFPAK)</p>	
4	gate (g)		
mb	mounting base, connected to drain (d)		

3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
BUK9Y19-55B	LFAK	Plastic single-ended surface mounted package (Philips version LFAK); 4 leads	SOT669

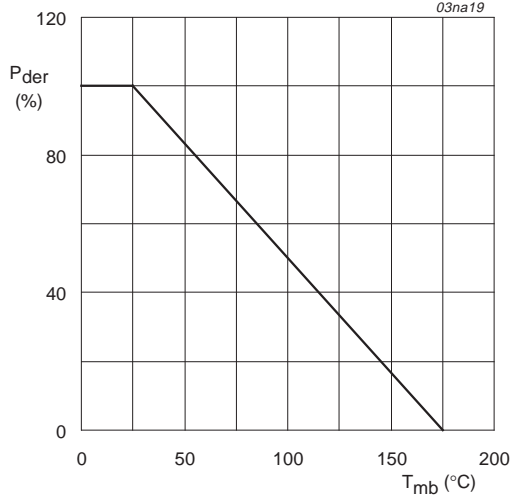
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

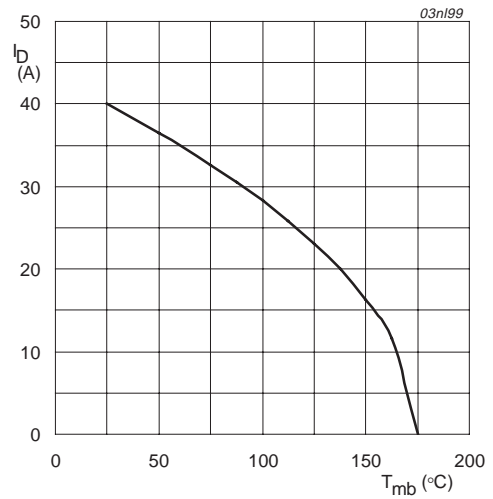
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage (DC)		-	± 15	V
I_D	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 5 \text{ V}$; Figure 2 and 3	-	40	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$; $V_{GS} = 5 \text{ V}$; Figure 2	-	28	A
I_{DM}	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; Figure 3	-	160	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Figure 1	-	75	W
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$
T_j	junction temperature		-55	+175	$^\circ\text{C}$
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	40	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	160	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 40 \text{ A}$; $V_{DS} \leq 55 \text{ V}$; $V_{GS} = 5 \text{ V}$; $R_{GS} = 50 \text{ }\Omega$; starting $T_{mb} = 25 \text{ }^\circ\text{C}$	-	91	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		-	[1]	-

- [1] Maximum value not quoted. Repetitive rating defined in Figure 16.
 Single-shot avalanche rating limited by $T_{j(max)}$ of 175 $^\circ\text{C}$.
 Repetitive avalanche rating limited by $T_{j(avg)}$ of 170 $^\circ\text{C}$.
 Refer to http://www.semiconductors.philips.com/acrobat/applicationnotes/AN10273_1.pdf for further information.



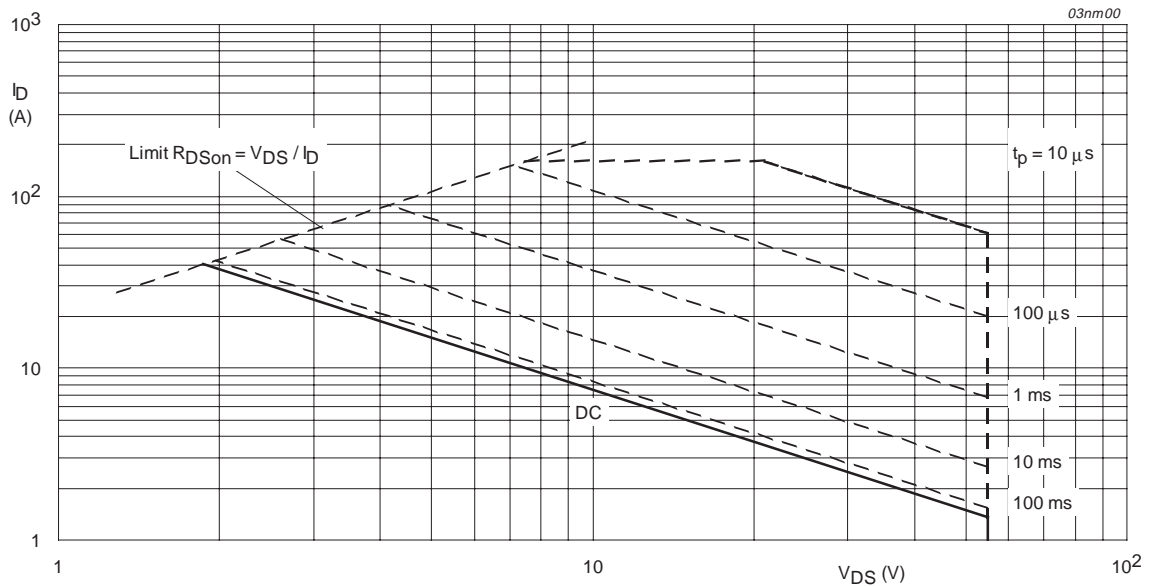
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



V_{GS} ≥ 5 V

Fig 2. Continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

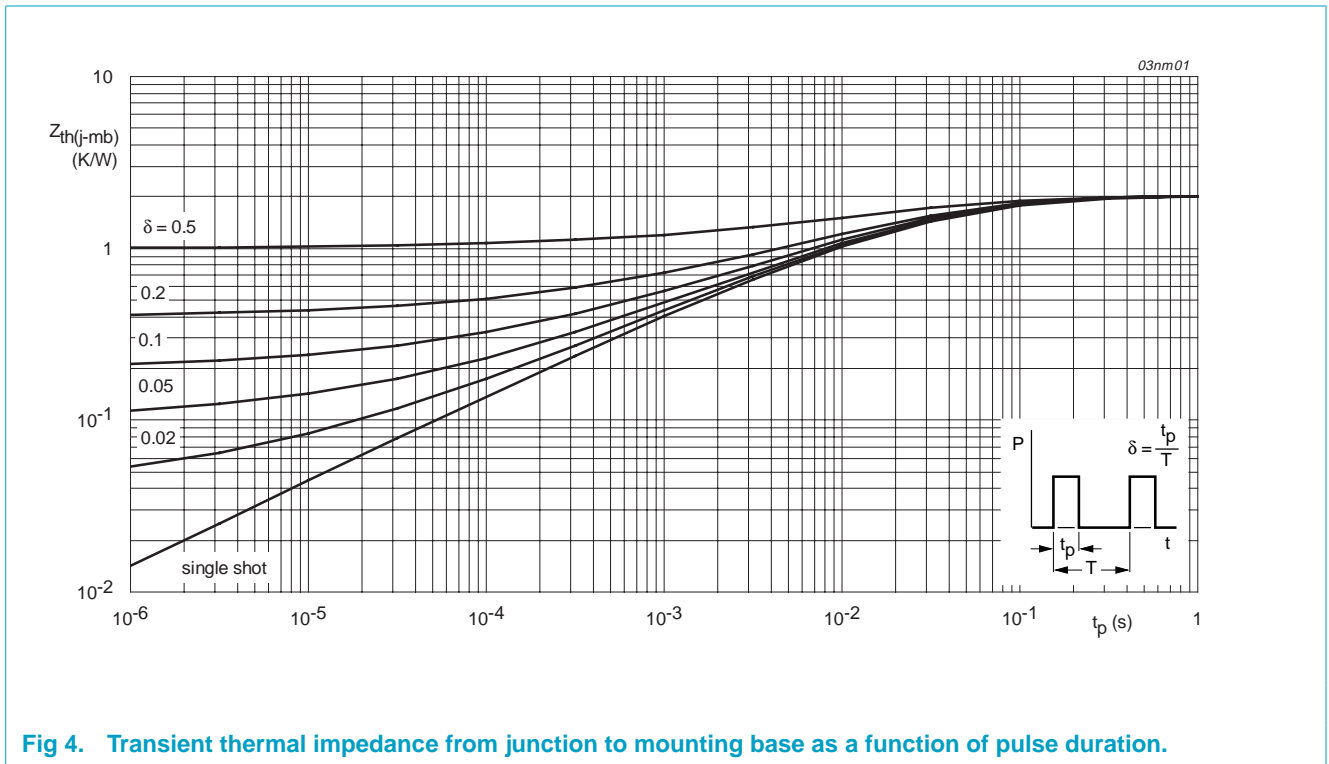
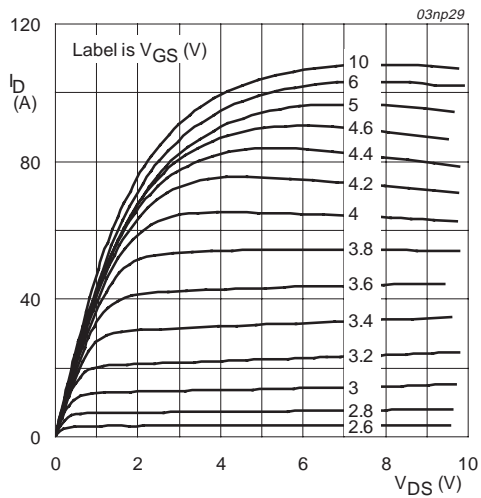


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

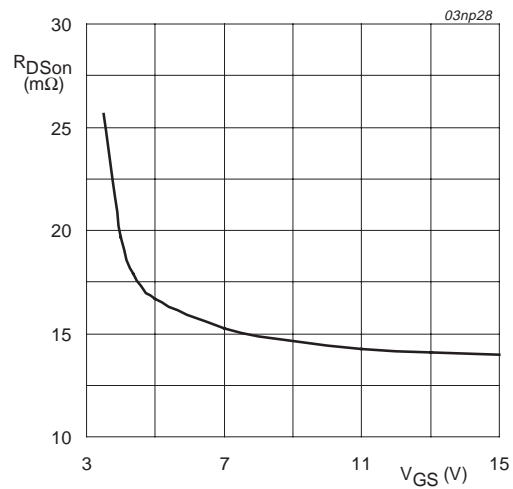
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	1.1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.02	1	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 20\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	16.3	19	m Ω
		$T_j = 175\text{ °C}$	-	-	40	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$	-	-	21	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$	-	14.3	17.3	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 5\text{ V}$; $V_{DD} = 44\text{ V}$; $I_D = 25\text{ A}$; Figure 14	-	18	-	nC
Q_{gs}	gate-to-source charge		-	5	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	8	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 12	-	1494	1992	pF
C_{oss}	output capacitance		-	217	260	pF
C_{riss}	reverse transfer capacitance		-	86	118	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $R_G = 10\text{ }\Omega$	-	18	-	ns
t_r	rise time		-	180	-	ns
$t_{d(off)}$	turn-off delay time		-	44	-	ns
t_f	fall time		-	134	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$	-	52	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$	-	38	-	nC



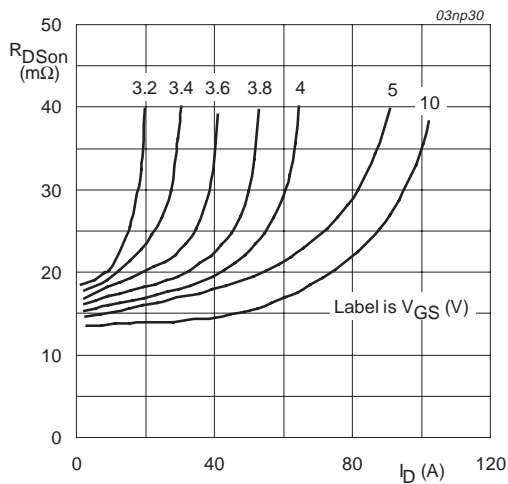
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



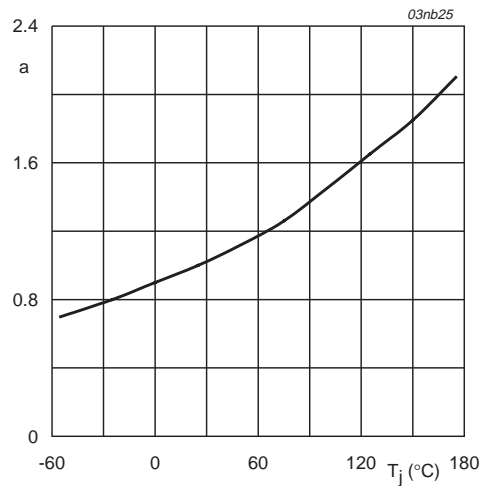
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 20\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



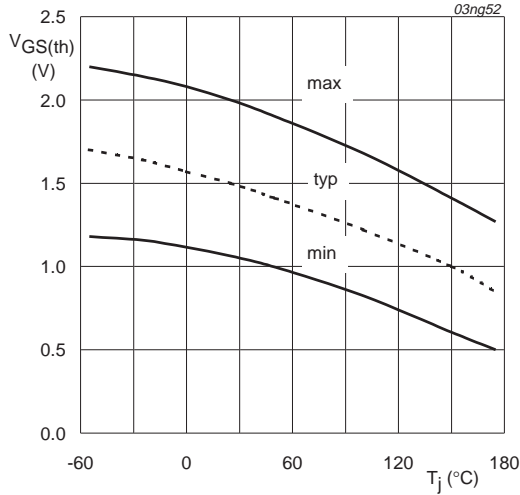
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



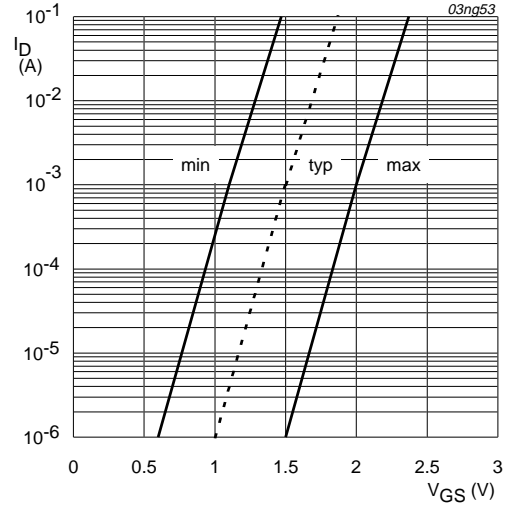
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



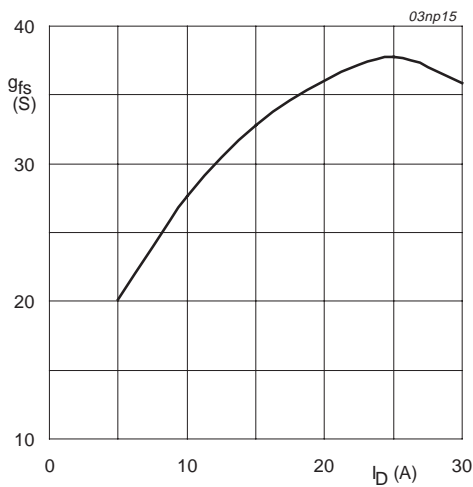
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



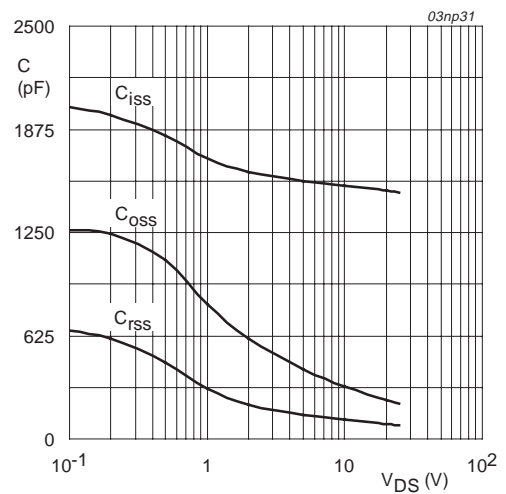
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



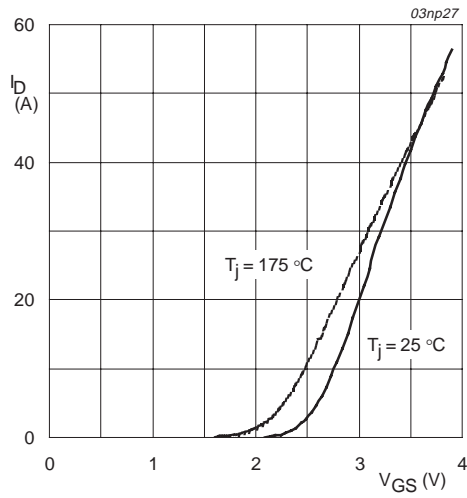
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



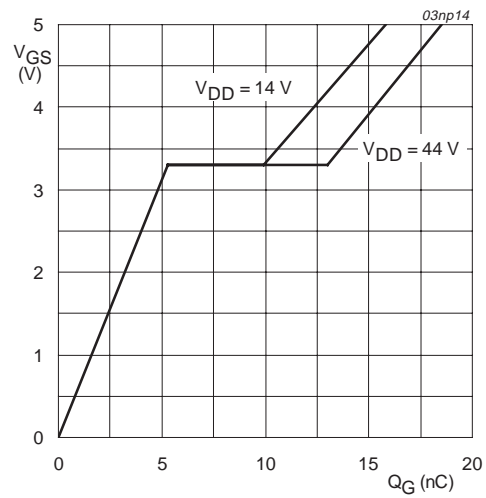
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



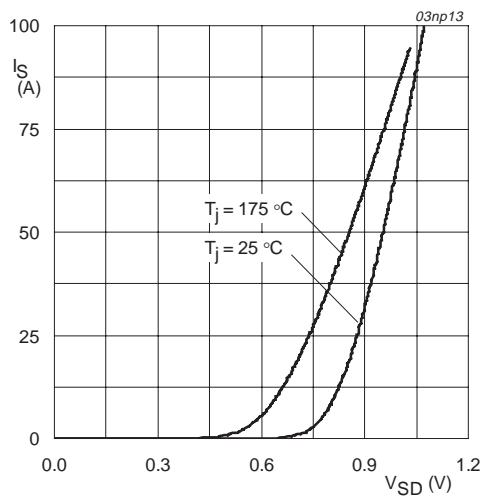
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



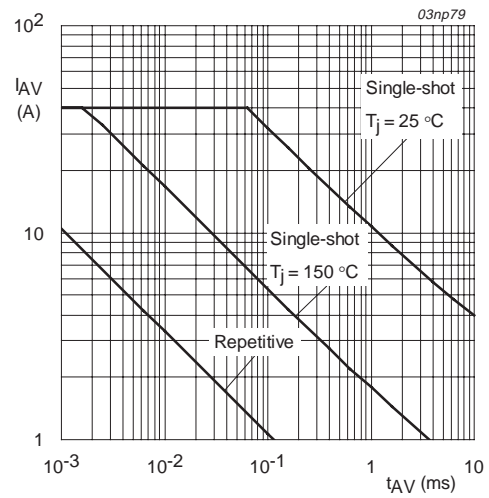
$T_j = 25 \text{ }^\circ\text{C}; I_D = 25 \text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



$V_{GS} = 0 \text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



See [Table note \[1\]](#) to [Table 3 "Limiting values"](#)

Fig 16. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period.

7. Package outline

Plastic single-ended surface mounted package (Philips version LFPAK); 4 leads

SOT669

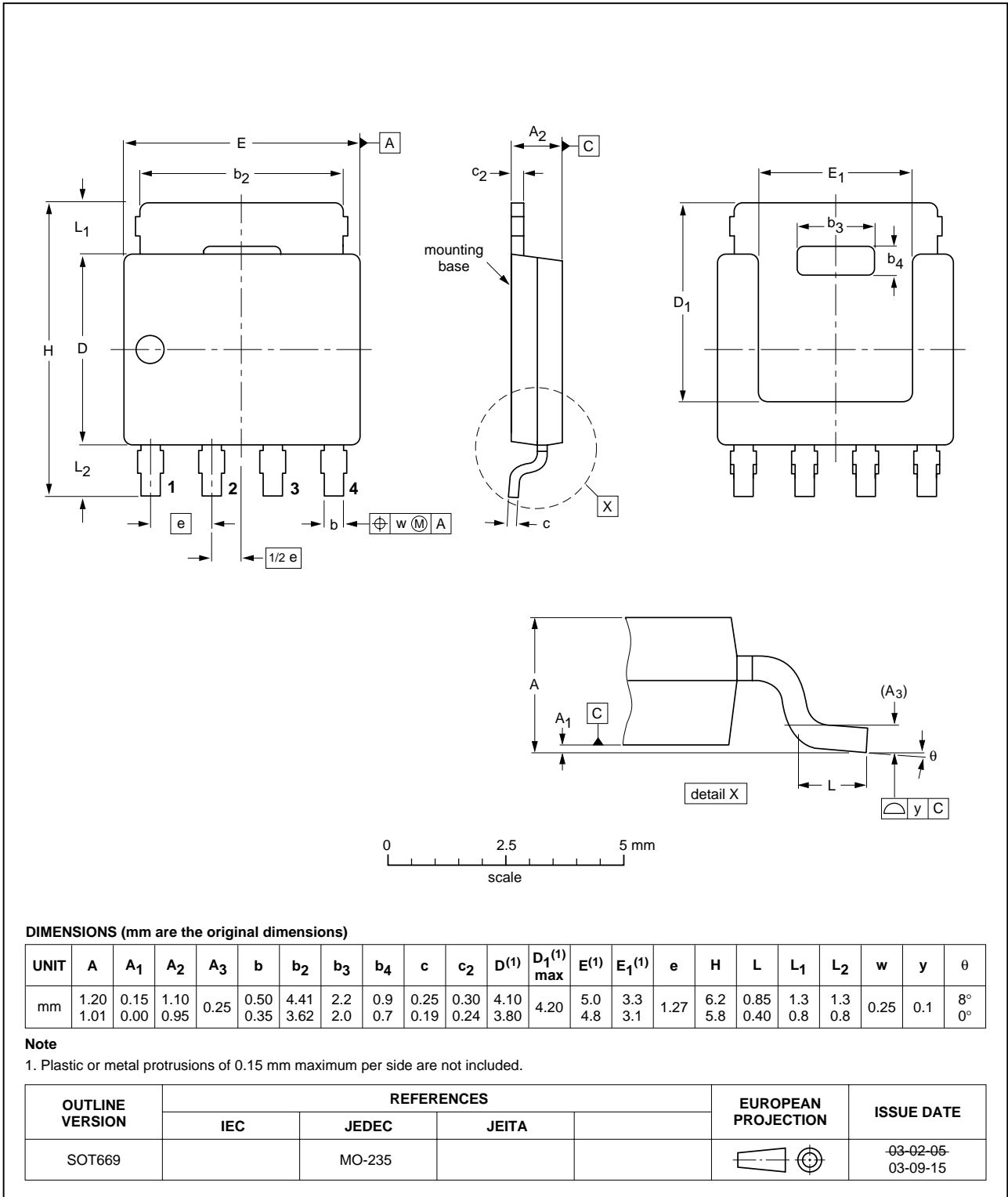


Fig 17. SOT669 (LFPAK).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040528	-	Product data (9397 750 13188)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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