T-33-13

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

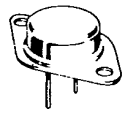
BUX42

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

. . . designed for high speed, high voltage, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.2 V at Ic = 4 A
- Very fast switching times:
  T_F max. = 0.4 μs at Ic = 6 A

12 AMPERES
NPN SILICON POWER METAL TRANSISTOR
250 VOLTS
120 WATTS



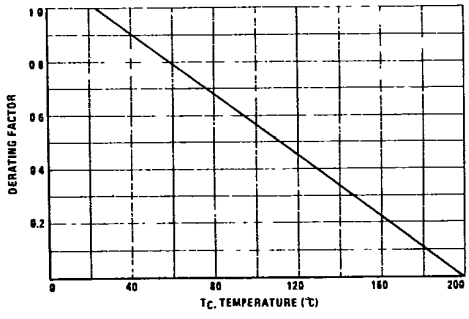
MAXIMUM RATINGS

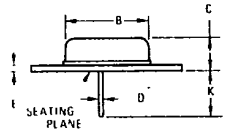
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −2.5 V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	290	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	12 15	Adc Apk
Base-Current continuous	I_B	2.4	Adc
Total Power Dissipation @ T_C = 25°C	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

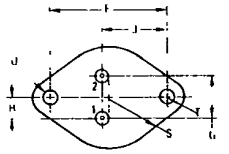
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

FIGURE 1 – POWER DERATING







STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

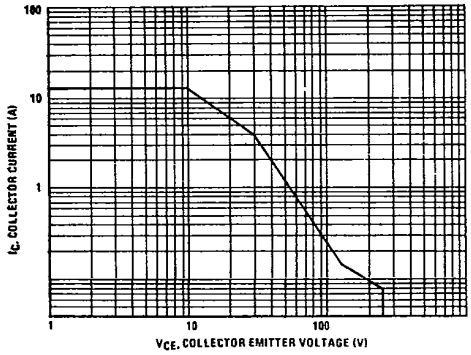
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1 03
(TO 3)

3

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on T_C = 25°C, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

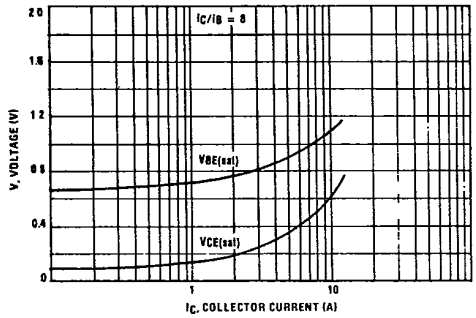


FIGURE 4 – DC CURRENT GAIN

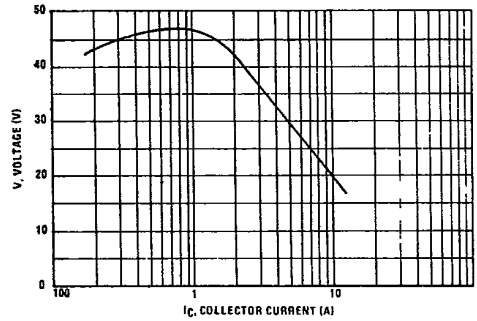


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

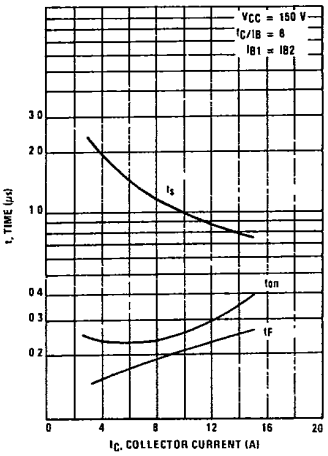
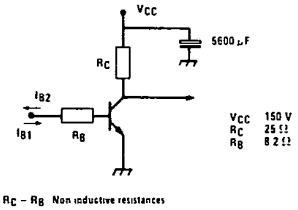


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



R_C – R_B Non-inductive resistances