High Power NPN Silicon Transistors
(15A, 400V and 450V, 175W)

FEATURES

- Designed for general-purpose switching applications.
- Collector-Emitter saturation voltage $V_{CE(sat)}$ = 1.5 V_{dc} (Max) @ I_C = 8 Adc
- High voltage capability, high current capability

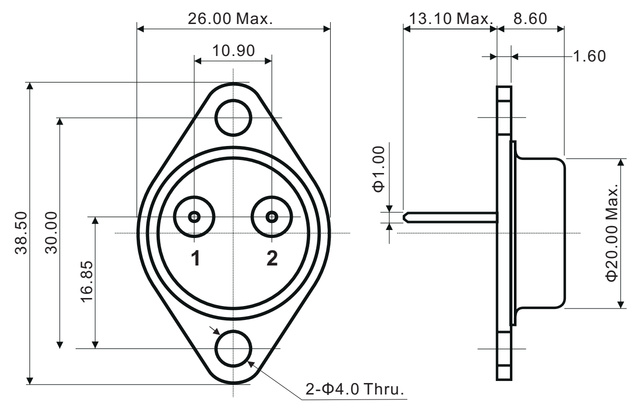
DESCRIPTION

The **BUX48** is a silicon epitaxial-base mesa NPN transistor mounted in JEDEC TO-3 metal case.

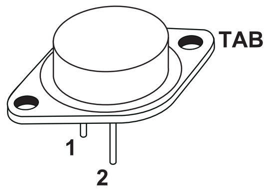
It is intended for power switching circuits and industrial applications from single and three-phase mains.

APPLICATIONS

- Switch mode power supplies
- Flyback and forward single transistor low power converters
- Inverters
- Solenoid and Relay drivers
- Motor controls
- Deflection circuits

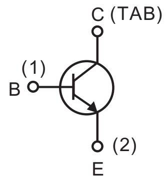


All dimensions in millimeters



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER		VALUE BUX48	VALUE BUX48A	UNIT
V_{CES}	Collector to emitter voltage (V_{BE} = 0)		850	1000	V
V_{CER}	Collector to emitter voltage (R_{BE} = 10Ω)		850	1000	V
V_{CEO}	Collector to emitter voltage (I_B = 0)		400	450	V
V_{EBO}	Emitter to base voltage (I_C = 0)		7		V
I_C	Collector current		15		A
I_{CM}	Collector peak current		30		A
I_{CP}	Collector peak current, non repetitive (t_p < 20μs)		55		A
I_B	Base current		4		A
I_{BM}	Base peak current		20		A
P_D	Total power dissipation	T_C= 25°C	175		W
		T_C= 100°C	100		W
	Derate above 25°C		1.0		W/ºC
T_j	Junction temperature		200		ºC
T_{stg}	Storage temperature		-65 to 200		ºC
T_L	Maximum lead temperature for soldering purposes : 1/8" from case for 5 seconds		275		ºC

THERMAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)			
SYMBOL	**PARAMETER**	**VALUE**	**UNIT**
$R_{th(j-c)}$	Thermal resistance, junction to case	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)						
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**MAX**	**UNIT**
◎ **OFF CHARACTERISTICS**						
I_{CES}	Collector cutoff current (V_{BE} = 0)	V_{CE} = rated V_{CES}			200	μA
		V_{CE} = rated V_{CES}, T_C = 125°C			2.0	mA
I_{CER}	Collector cutoff current (R_{BE} = 10Ω)	V_{CE} = rated V_{CER}			500	μA
		V_{CE} = rated V_{CER}, T_C = 125°C			4	mA
I_{EBO}	Emitter cutoff current	V_{EB} = 5V, I_C = 0			1.0	mA
$V_{CEO(SUS)}$*	Collector to emitter sustaining voltage	I_C = 200mA, I_B = 0, L = 25mH	BUX48	400		V
			BUX48A	450		
V_{CES}	Collector to emitter voltage	V_{BE} = 0	BUX48	850		
			BUX48A	1000		
V_{EBO}	Emitter to base voltage	I_C = 0, I_E = 50mA		7	30	
◎ **ON CHARACTERISTICS**						
$V_{CE(sat)}$*	Collector to emitter saturation voltage	I_C = 10A, I_B = 2A	BUX48		1.5	V
		I_C = 15A, I_B = 4A			3.5	
		I_C = 15A, I_B = 3A			5	
		I_C = 8A, I_B = 1.6A	BUX48A		1.5	
		I_C = 12A, I_B = 2.4A			5	
$V_{BE(sat)}$*	Base to emitter saturation voltage	I_C = 10A, I_B = 2A	BUX48		1.6	V
		I_C = 8A, I_B = 1.6A	BUX48A		1.6	
h_{FE}	DC current gain	I_C = 10A, V_{CE} = 5V	BUX48	8		
		I_C = 8A, V_{CE} = 5V	BUX48A	8		
◎ **DYNAMIC CHARACTERISTICS**						
C_{ob}	Output capacitance	V_{CB} = 10V, I_E = 0, f_{test} = 1 MHz			350	pF

*Pulsed : Pulse duration = 300 μs, duty cycle ≤ 2%, V_{c1} =300V, $V_{BE(off)}$ = 5V, L_C = 180μH

RESISTIVE SWITCHING TIMES

SYMBOL	PARAMETER	CONDITIONS		MIN	MAX	UNIT
t_{on}	Turn-on time	V_{CC} = 300V, I_C = 10A, I_{B1} = 2A	BUX48		1	μs
		V_{CC} = 300V, I_C = 8A, I_{B1} = 1.6A	BUX48A		1	
t_d	Delay time	V_{CC} = 300V, I_C = 10A, I_{B1} = 2A	BUX48		0.2	
		V_{CC} = 300V, I_C = 8A, I_{B1} = 1.6A	BUX48A		0.2	
t_r	Rise time	V_{CC} = 300V, I_C = 10A, I_{B1} = $-I_{B2}$ = 2A	BUX48		0.7	
		V_{CC} = 300V, I_C = 8A, I_{B1} = $-I_{B2}$ = 1.6A	BUX48A		0.7	
t_s	Storage time	V_{CC} = 300V, I_C = 10A, I_{B1} = $-I_{B2}$ = 2A	BUX48		2	
		V_{CC} = 300V, I_C = 8A, I_{B1} = $-I_{B2}$ = 1.6A	BUX48A		2	
t_f	Fall time	V_{CC} = 300V, I_C = 10A, I_{B1} = $-I_{B2}$ = 2A	BUX48		0.4	
		V_{CC} = 300V, I_C = 8A, I_{B1} = $-I_{B2}$ = 1.6A	BUX48A		0.4	

*V_{BE} = -5V, duty cycle = 2%, t_p = 30 μs

INDUCTIVE SWITCHING TIMES

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNIT
t_s	Storage time	V_{CC} = 300V, I_C = 10A, L_B = 3μH I_{B1} = 2A, V_{BE} = -5V	T_C = 25°C	BUX48		1.3		μs
			T_C = 125°C				2.5	
		V_{CC} = 300V, I_C = 8A, L_B = 3μH I_{B1} = 1.6A, V_{BE} = -5V	T_C = 25°C	BUX48A		1.5		
			T_C = 125°C				2.5	
t_f	Fall time	V_{CC} = 300V, I_C = 10A, L_B = 3μH I_{B1} = 2A, V_{BE} = -5V	T_C = 25°C	BUX48		0.10		μs
			T_C = 125°C				0.4	
		V_{CC} = 300V, I_C = 8A, L_B = 3μH I_{B1} = 1.6A, V_{BE} = -5V	T_C = 25°C	BUX48A		0.15		
			T_C = 125°C				0.4	

*Duty cycle = 2%, t_p = 30 μs

DC CHARACTERISTICS

Fig.1 DC current gain

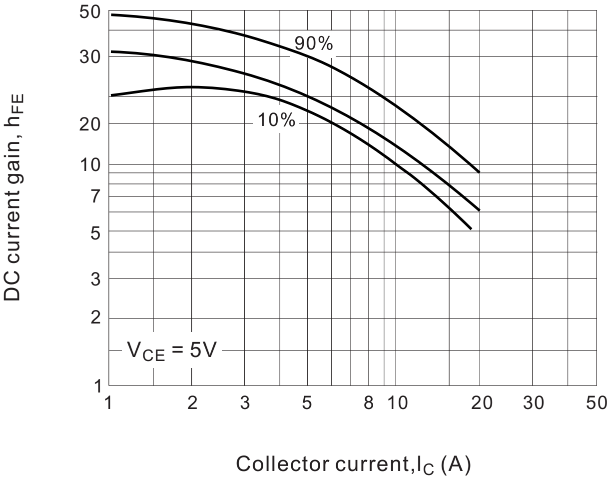


Fig.2 Collector saturation region

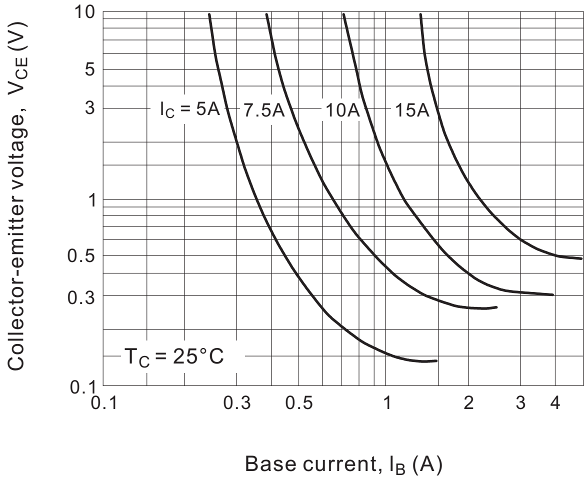


Fig.3 Collector-Emitter saturation voltage

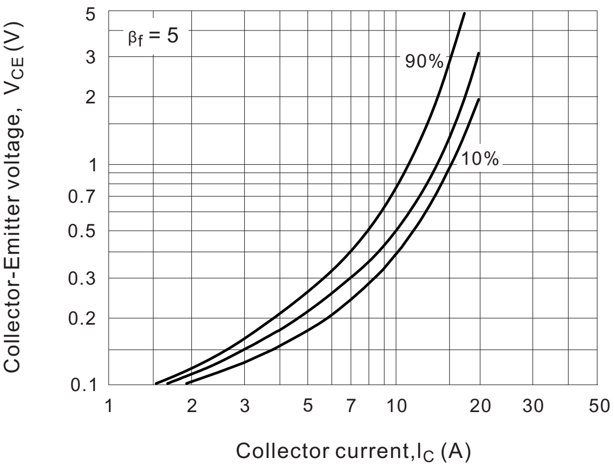


Fig.4 Base-Emitter voltage

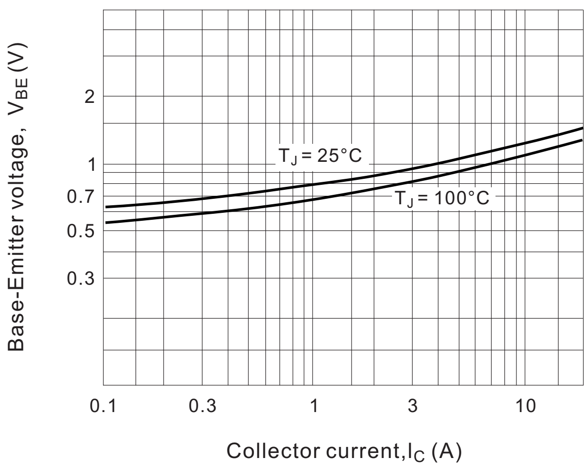


Fig.5 Collector cutoff region

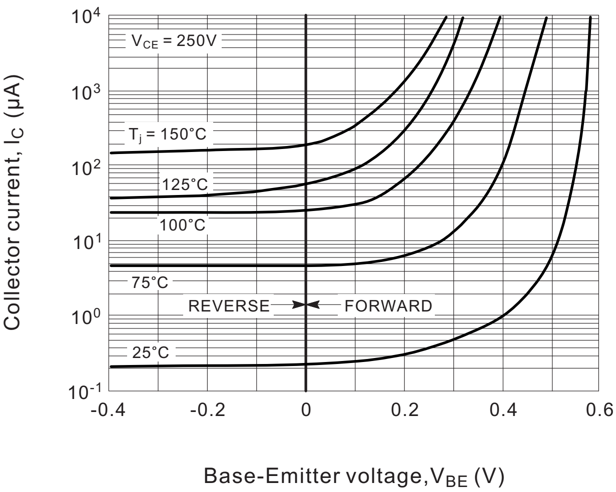


Fig.6 Capacitance

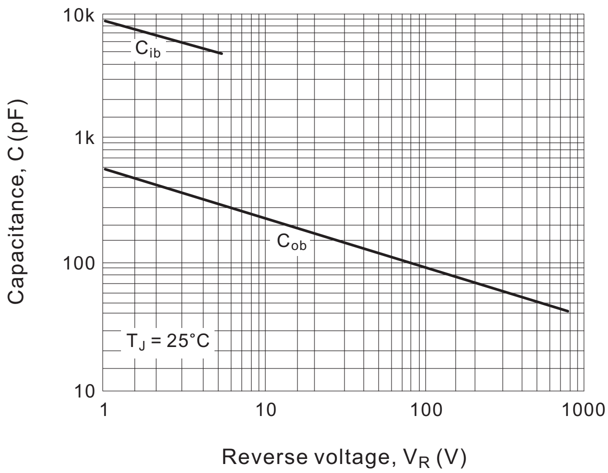


Table.1 Test Conditions for Dynamic Performance

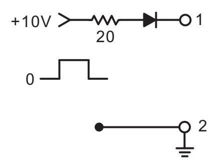
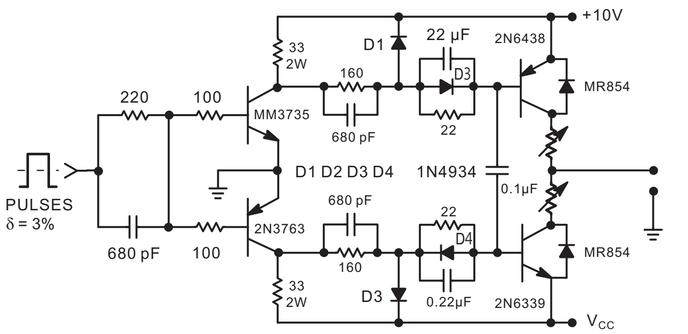
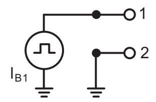
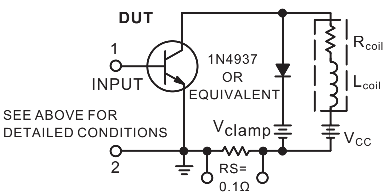
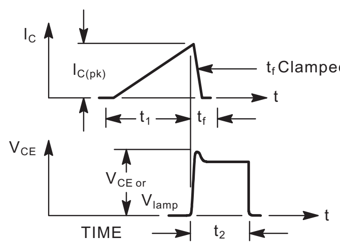
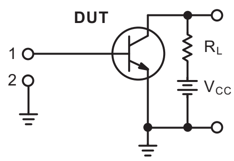
	$V_{CEO(SUS)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 200 mA		TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired. TURN-OFF TIME: Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 25 mH, V_{cc} = 10V; R_{coil} = 0.7Ω	L_{coil} = 180 μH; R_{coil} = 0.05Ω; V_{cc} = 20V; V_{clamp} = 300 V; R_B ADJUSTED TO ATTAIN DESIRED I_{B1}	V_{CC} = 300 V; R_L = 83Ω; Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to obtain I_C; $t_1 = \frac{L_{coil}(I_{Cpk})}{V_{CC}}$; $t_2 = \frac{L_{coil}(I_{Cpk})}{V_{Clamp}}$; Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

Fig.7 Inductive switching measurements

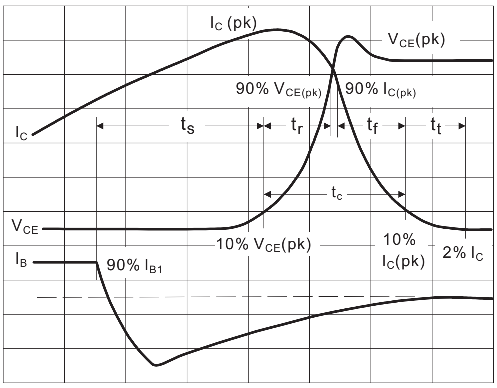
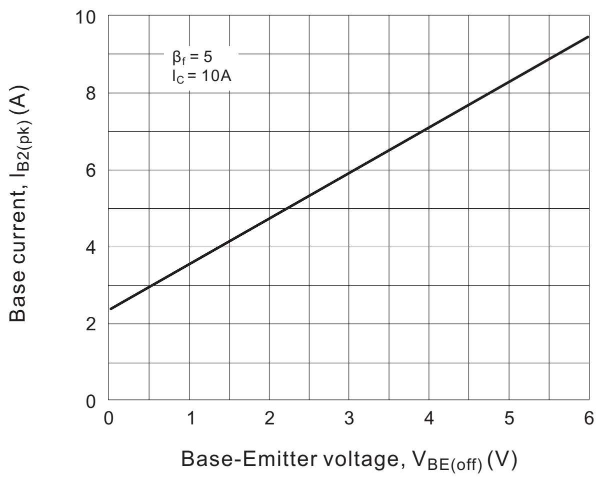


Fig.8. Peak-Reverse current



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time, For this reason, the following new terms have been defined.

t_S = Voltage storage time, 90% I_{B1} to 10% V_{clamp}

t_r = Voltage rise time, 10-90% V_{clamp}

t_f = Current fall time, 90-10% I_C

t_t = Current tail, 10-2% I_C

t_C = Crossover time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Fig.7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obatined using the standard equation from AN-222:

$$P_{SWT} = \frac{1}{2} V_{cc} \cdot I_c \cdot (t_c) f$$

In general, $t_r + t_f = t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmak for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_C and t_S) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

Fig.9 Storage time, t_S

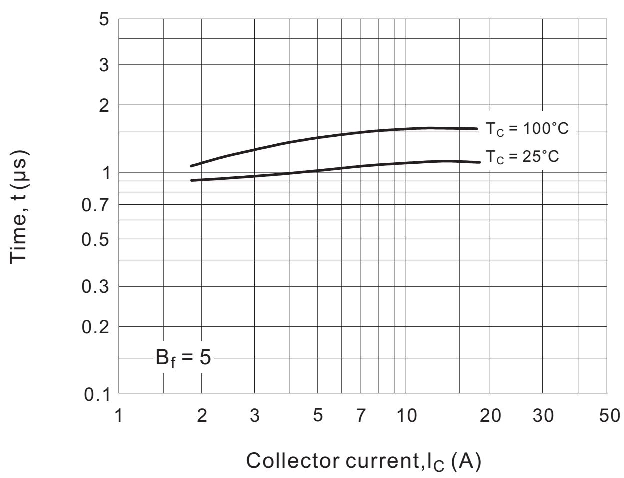


Fig.10 Crossover and fall times

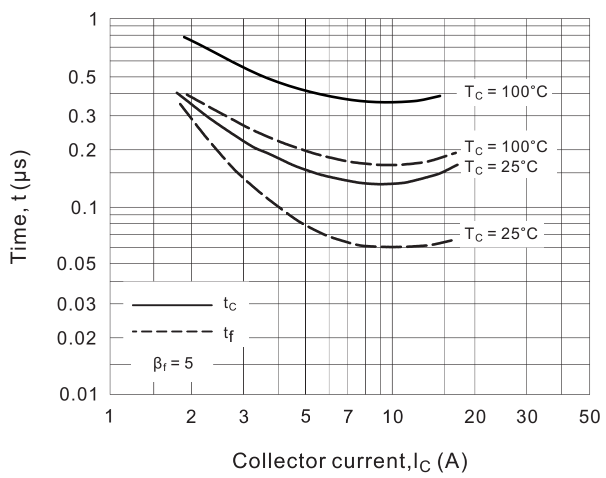


Fig.11a Turn-Off times versus forced gain

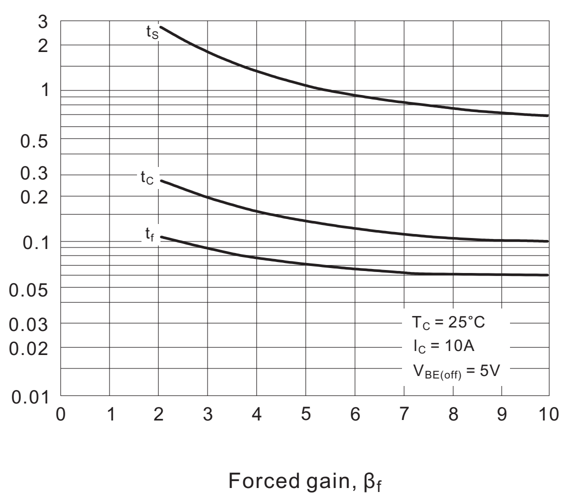
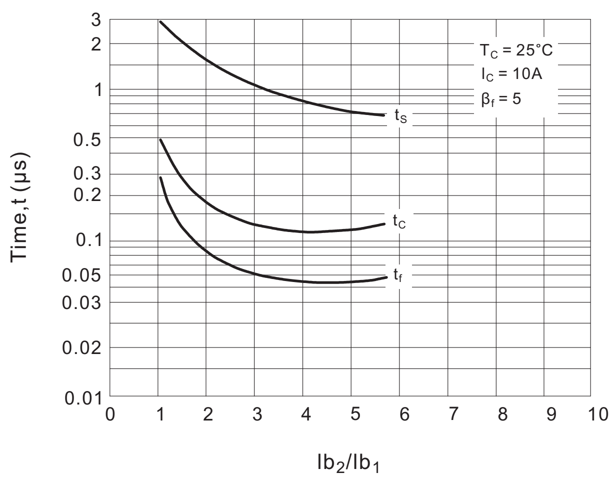


Fig.11b. Turn-Off times versus Ib_2/Ib_1



The safe operating area figures 12 and 13 are specified for these devices under the test conditions shown.

Fig.12 Forward bias safe operating area

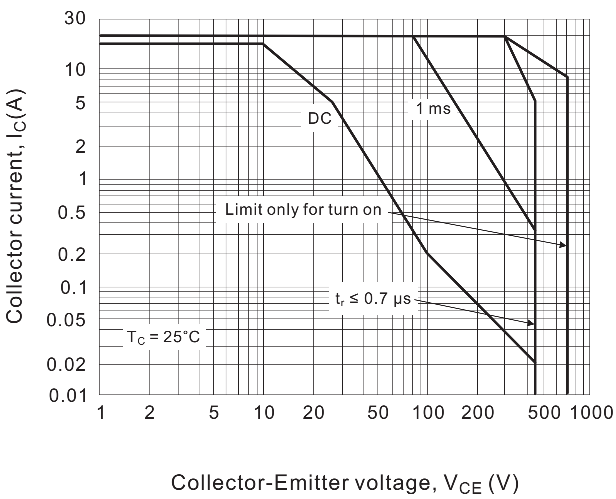
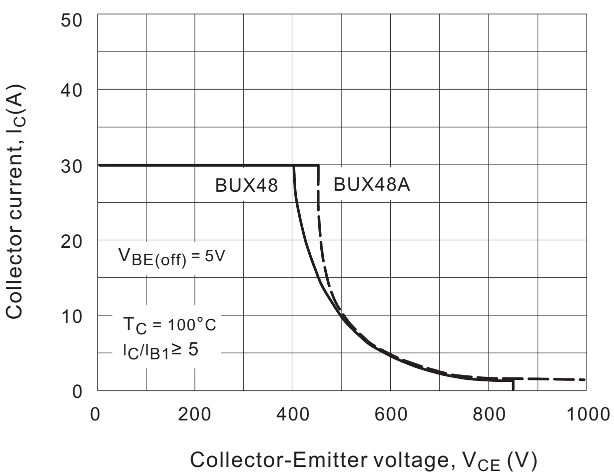


Fig.13 Reverse bias safe operating area



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handing ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation:i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig.12 is based on T_C =25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the voltages shown on Fig.12 may be found at any case temperature by using the appropriate curve on Fig.14

T_j (pk) may be caluclated from the data in Fig.11 at high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe leve for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Fig.13 gives RBSOA characteristics.

Fig.14 Power derating

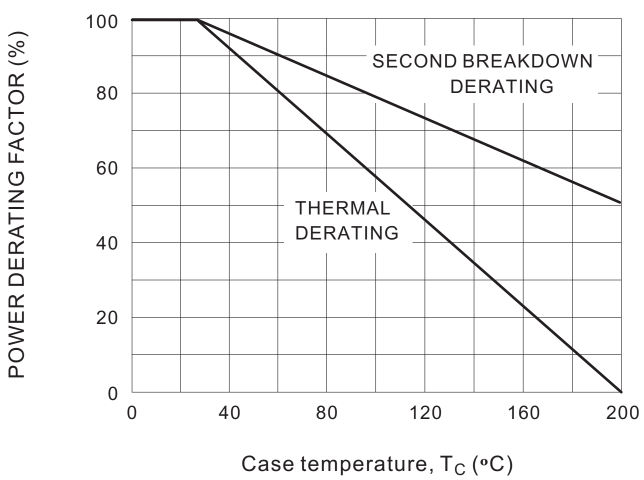
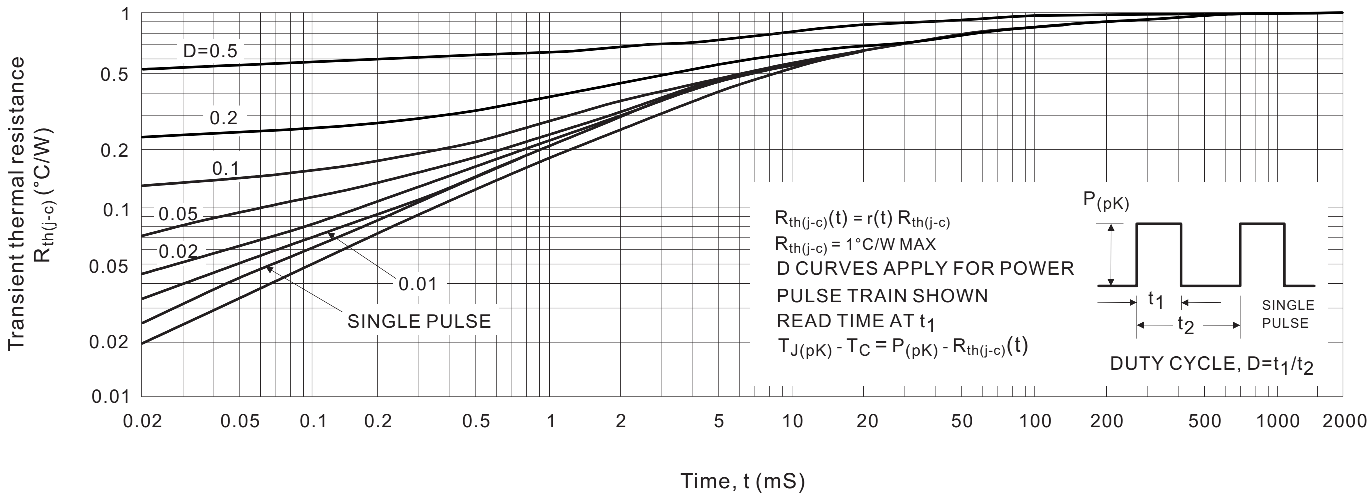
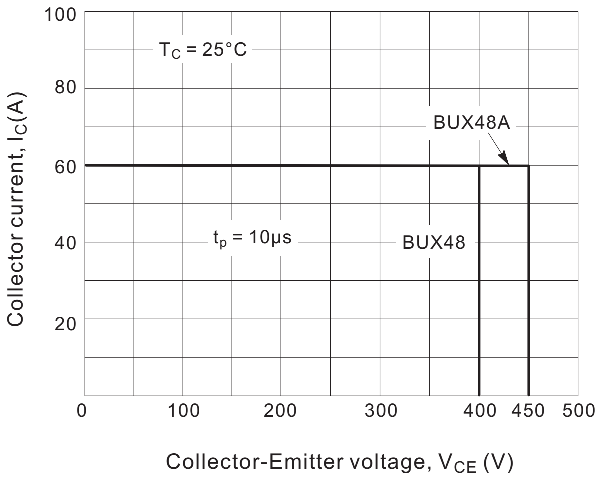


Fig.15 Thermal response



OVERLOAD CHARACTERISTICS

Fig.16 Rated overload safe operating area (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drieve.) Storage time of the transistor has been factored into the curve. Therefore. with bus voltage and maximum collector current known, Fig.16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (fig.18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

Fig.17 I_C = f(dV/dt)

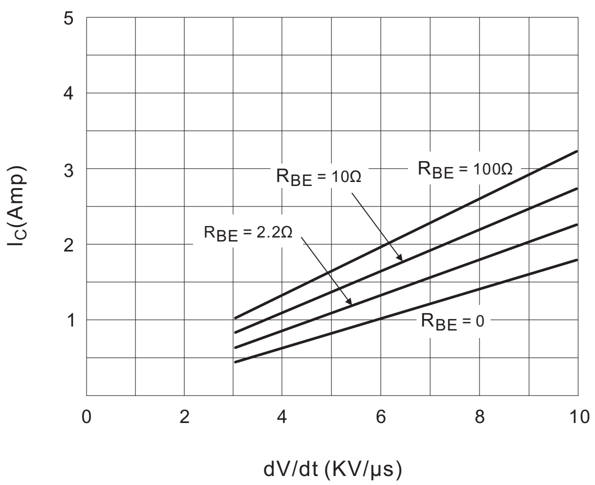


Fig.18 Overload SOA test circuit

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p