

Automotive IPD 1ch Low-Side Switch with Slew Rate Control and Output Diagnostic Function

BV1LF080EFJ-C

Features

- AEC-Q100 Qualified (Note 1)
- Built-in Dual TSD (Note 2)
- Built-in Over Current Protection Function (OCP)
- Built-in Thermal Shutdown Function (TSD)
- Built-in Active Clamp Function
- Built-in Diagnostic Function
- Built-in Slew Rate Control Function
- Directly Controllable from CMOS logic ICs
- On-Resistance $R_{DS(ON)} = 80\text{m}\Omega$ (Typ)
($V_{DD} = 5\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $T_j = 25\text{ }^\circ\text{C}$)
- Monolithic Power Management IC with Control Unit (CMOS) and Power MOSFET on a Single Chip

(Note 1) Grade 1

(Note 2) This IC has thermal shutdown (Junction temperature detect) and ΔT_j Protection (Power-MOS steep temperature rising detect).

Key Specifications

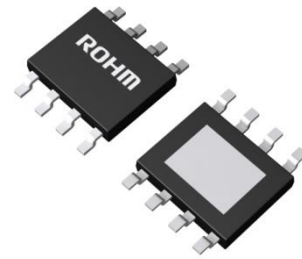
On-state Resistance ($T_j = 25\text{ }^\circ\text{C}$, Typ)	80 m Ω
Over Current Limitation Level ($T_j = 25\text{ }^\circ\text{C}$, Typ)	7.5 A
Output Clamp Voltage (Min)	42 V
Active Clamp Energy ($T_{j(\text{START})} = 25\text{ }^\circ\text{C}$)	200 mJ

Package

HTSOP-J8

W (Typ) x D (Typ) x H (Max)

4.9 mm x 6.0 mm x 1.0 mm



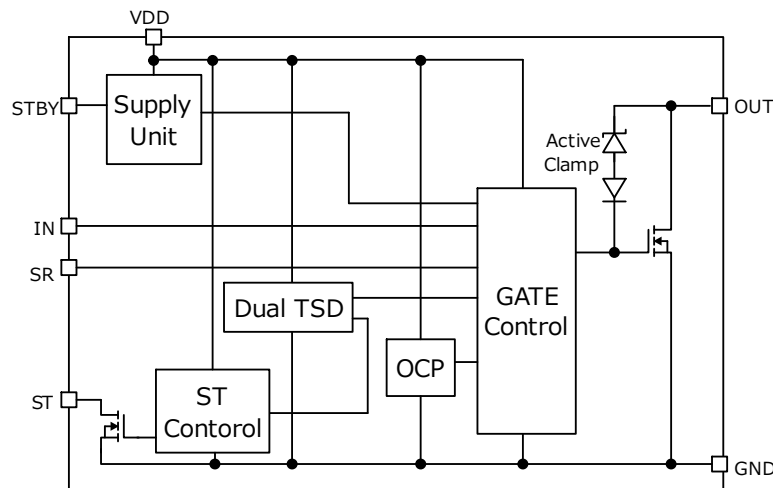
General Description

BV1LF080EFJ-C is a 1ch low-side switch for automotive application. Output slew rate are variably controlled by external resistance of the SR terminal. It has built-in OCP, Dual TSD and Active Clamp function. It is equipped with output diagnostic function for TSD

Application

- Driving Resistive, Inductive and Capacitive Loads

Block Diagram

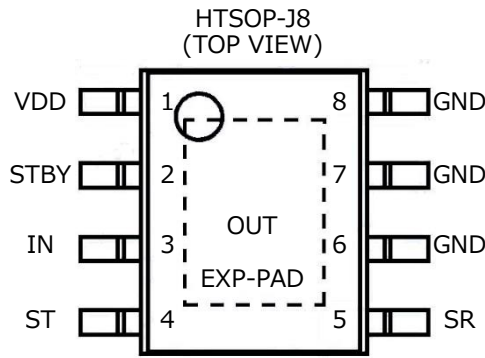


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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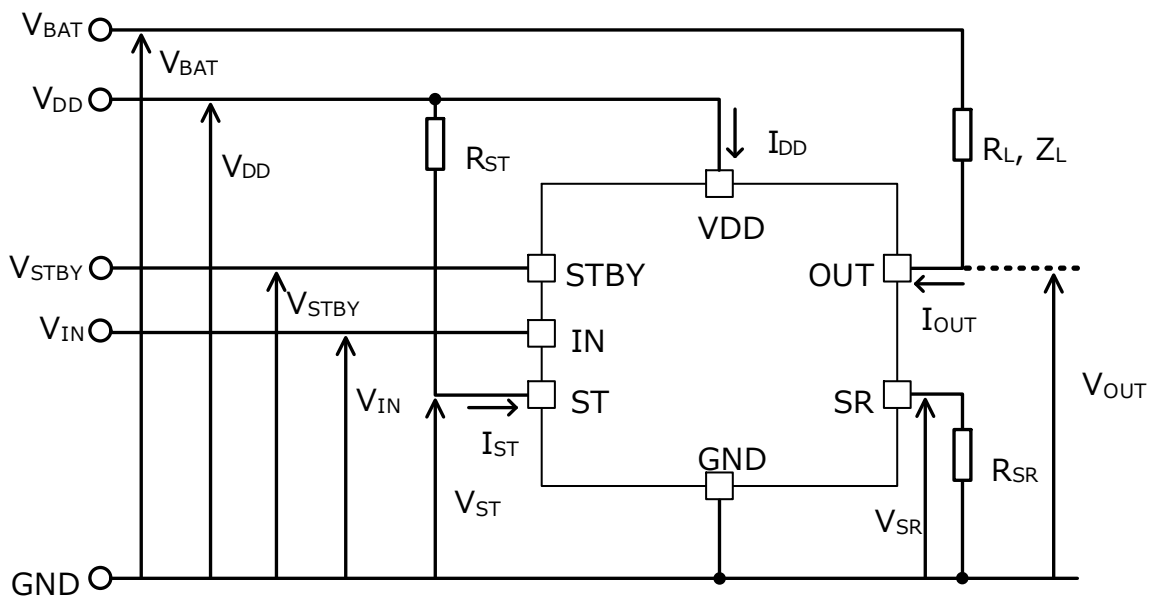
Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	VDD	Power supply pin.
2	STBY	Input pin. Pull-down resistor is internally connected
3	IN	Input pin. Pull-down resistor is internally connected
4	ST	Self-diagnostic output pin.
5	SR	Slew rate control pin
6	GND	Ground pin.
7	GND	Ground pin.
8	GND	Ground pin.
EXP-PAD	OUT	Output pin. When output pin is shorted to power supply and the output current is limited to protect IC.

Definition



Absolute Maximum Ratings (Tj = 25 °C)

Parameters	Symbol	Rating	Unit
Power Supply Voltage	V _{DD}	-0.3 to +7	V
Output Voltage	V _{OUT}	-0.3 to +42	V
	V _{SR}	-0.3 to V _{DD} + 0.3	V
Input Voltage	V _{IN}	-0.3 to +7	V
	V _{STBY}	-0.3 to +7	V
Output Current	I _{OUT}	5 (internal limit) ^(Note 1)	A
Diagnostic Output Voltage	V _{ST}	-0.3 to +7	V
Diagnostic Output Current	I _{ST}	10	mA
Active Clamp Energy (Single Pulse) T _{j(START)} = 25 °C ^(Note 2)	E _{AS(25 °C)}	200	mJ
Active Clamp Energy (Single Pulse) T _{j(START)} = 150 °C ^{(Note 2) (Note 3)}	E _{AS(150 °C)}	80	
Operating Temperature Range	T _j	-40 to +150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	T _{jmax}	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Internally limited by over current protection function.

(Note 2) Active clamp energy (Single Pulse), at the condition I_{OUT(START)} = 1.0 A, V_{BAT} = 16 V.

$$E_{AS} = \frac{1}{2} L I_{OUT(START)}^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CL)}} \right)$$

(Note 3) Not 100 % tested.

Recommended Operating Condition

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{DD}	3.5	5.0	6.5	V
Operating Temperature	T _j	-40	+25	+150	°C

Thermal Resistance *(Note 1)*

Parameter	Symbol	Typ	Unit	Condition
BV1LF080EFJ-C				
Between Junction and Surroundings Temperature Thermal Resistance	θ_{JA}	126.5	°C/W	1s <i>(Note 2)</i>
		37.8	°C/W	2s <i>(Note 3)</i>
		25.3	°C/W	2s2p <i>(Note 4)</i>

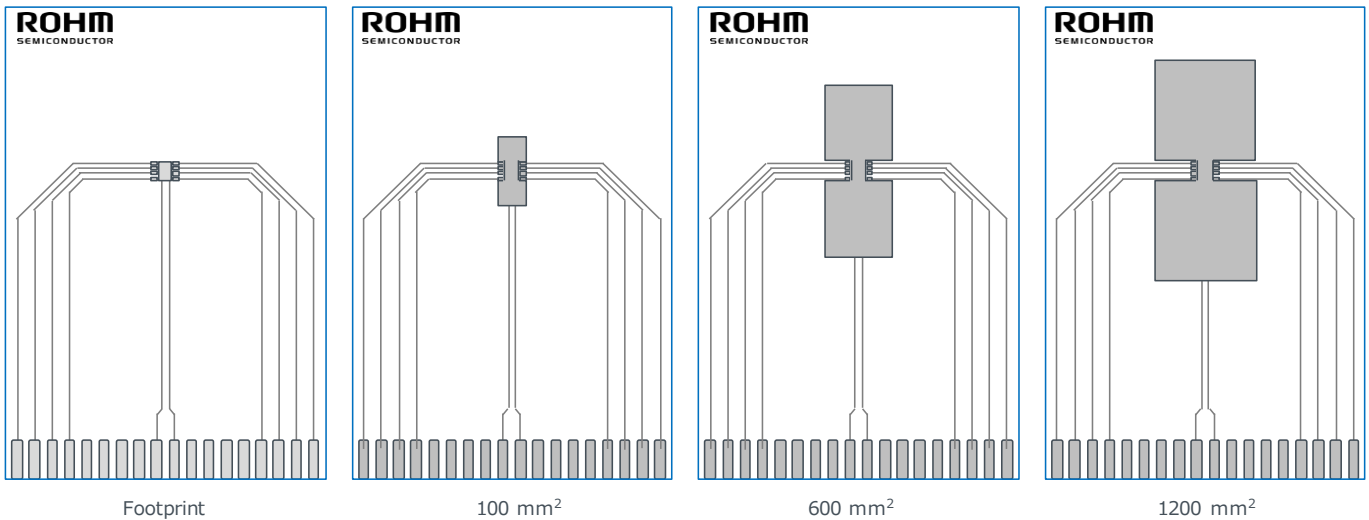
(Note 1) The thermal impedance is based on JESD51-2A (Still-Air) standard. It is used the chip of BV1LF080EFJ-C

(Note 2) JESD51-3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1-layer (1s)
(Top copper foil: ROHM recommended Footprint + wiring to measure, 2 oz. copper.)

(Note 3) JESD51-5 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 2-layers (2s)
(Top copper foil: ROHM recommended Footprint + wiring to measure/
Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,
copper (top & reverse side) 2 oz.)

(Note 4) JESD51-5/- 7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4-layers (2s2p)
(Top copper foil: ROHM recommended Footprint + wiring to measure/
2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,
copper (top & reverse side/inner layers) 2 oz./1 oz.)

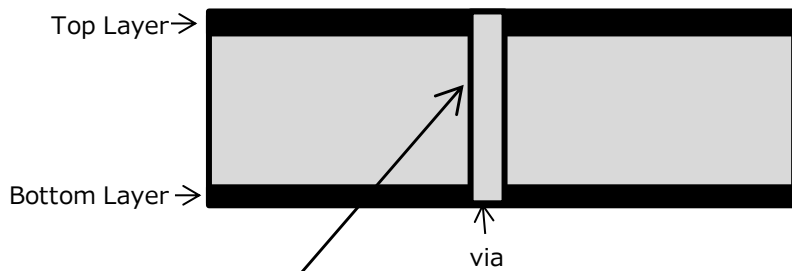
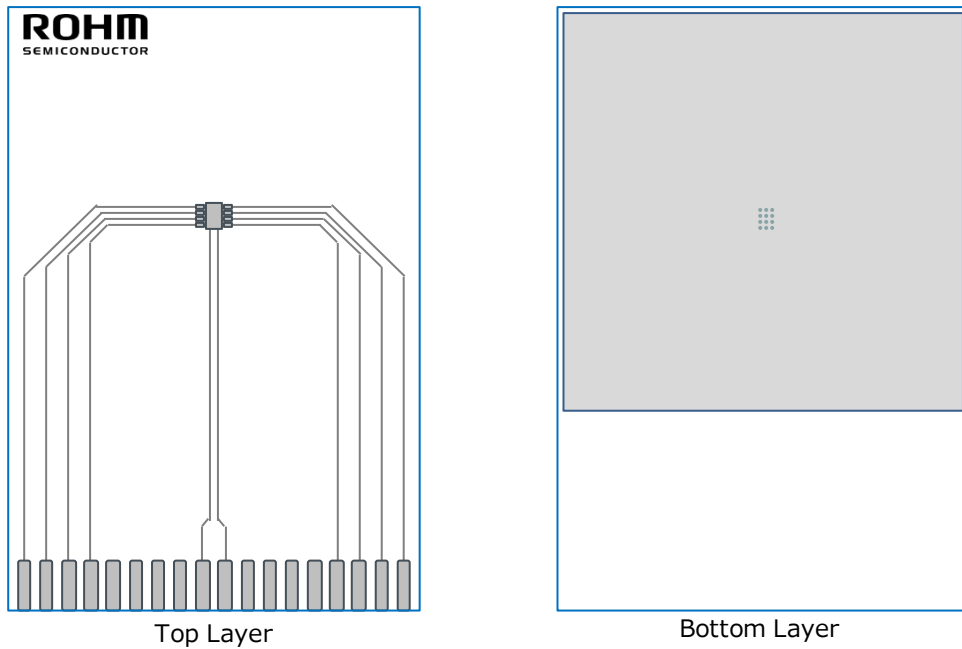
■ PCB Layout 1 Layer (1s)



Dimension	Value
Board Finish Thickness	1.57 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top Layer)	0.070 mm (Cu:2 oz)
Copper Foil Area Dimension	Footprint / 100 mm² / 600 mm² / 1200 mm²

Thermal Resistance – continued

- PCB Layout 2 Layers (2s)



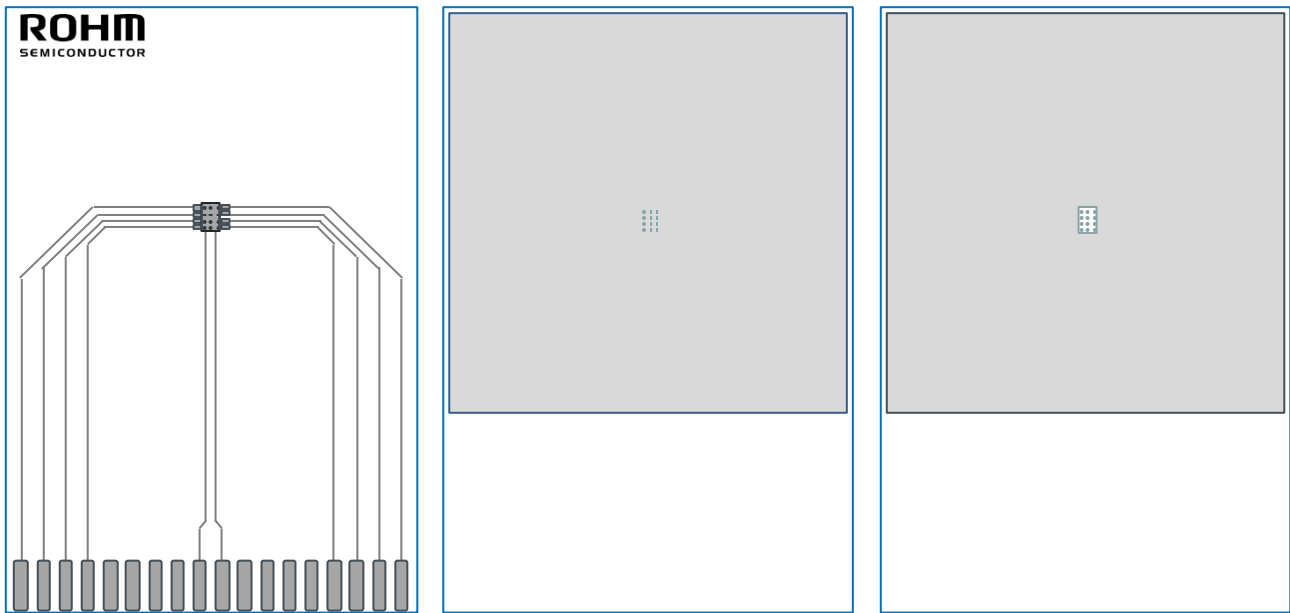
Isolation Clearance Diameter : ≥ 0.6 mm

Cross Section

Dimension	Value
Board Finish Thickness	1.60 mm \pm 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu +Plating)
Thermal Vias Separation/Diameter	1.2 mm / 0.3 mm

Thermal Resistance – continued

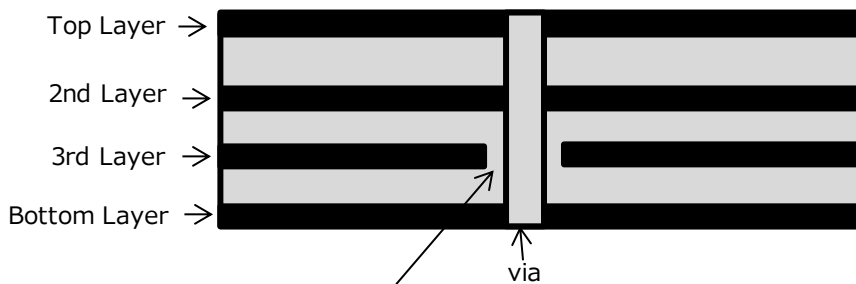
- PCB Layout 4 Layers (2s2p)



Top Layer

2nd / Bottom Layers

3rd Layer



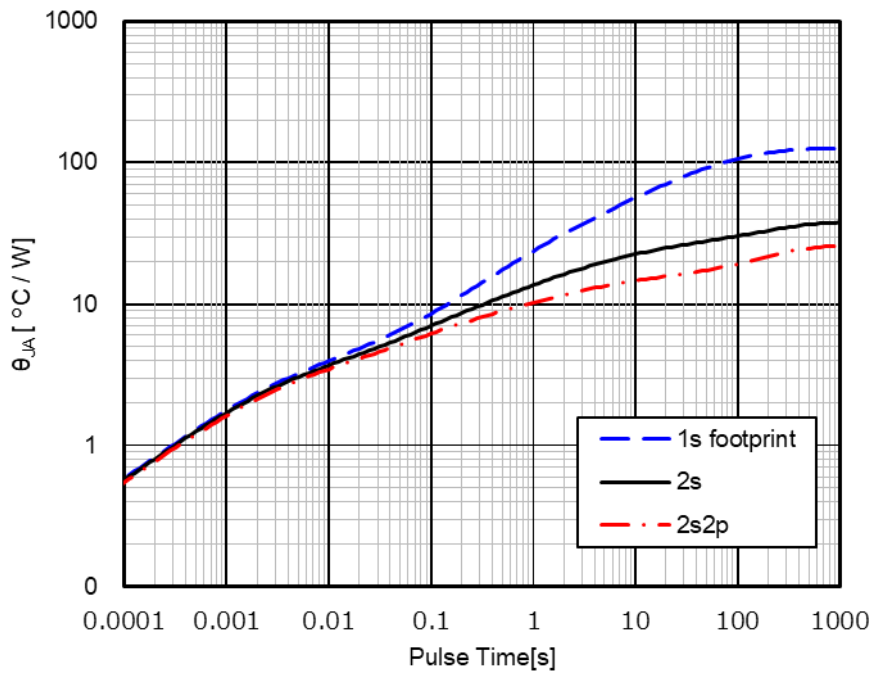
Isolation Clearance Diameter : ≥ 0.6 mm

Cross Section

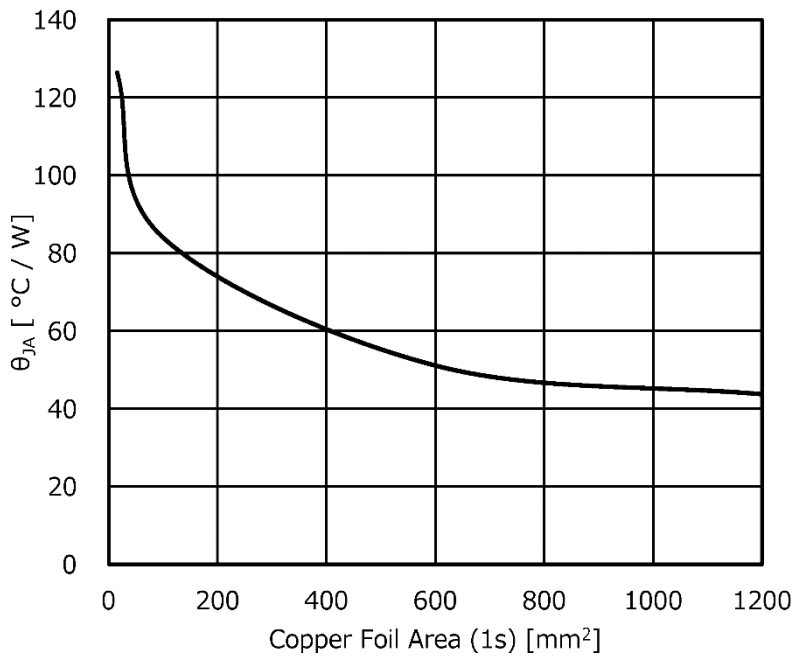
Dimension	Value
Board Finish Thickness	1.60 mm \pm 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu +Plating)
Thermal Vias Separation/Diameter	1.2 mm / 0.3 mm

Thermal Resistance – continued

- Transient Thermal Resistance (Single Pulse)



- Thermal Resistance (θ_{JA} vs. Copper Foil Area – (1s))



Electrical Characteristics

(Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$)

Parameters	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Power Supply						
Standby Current	$I_{VDD(S)}$	-	0	10	μA	$V_{DD} = 5\text{ V}$, $V_{STBY} = V_{IN} = 0\text{ V}$ $R_{SR} = 68\text{ k}\Omega$
Operating Current	I_{VDD}	-	200	500	μA	$V_{DD} = V_{STBY} = V_{IN} = 5\text{ V}$ $R_{SR} = 68\text{ k}\Omega$
Under Voltage Release Voltage	V_{UVLOR}	-	2.5	3.0	V	V_{DD} Sweep up
Under Voltage Hysteresis Voltage	$V_{UVLOHYS}$	-	0.2	0.4	V	
Input (STBY)						
High Level Input Voltage	$V_{STBY(H)}$	3.0	-	-	V	
Low Level Input Voltage	$V_{STBY(L)}$	-	-	1.5	V	
Input hysteresis Voltage	$V_{STBY(HYS)}$	-	0.2	-	V	
High Level Input Current	$I_{STBY(H)}$	-	50	150	μA	$V_{STBY} = 5\text{ V}$
Low Level Input Current	$I_{STBY(L)}$	-1	0	+1	μA	$V_{STBY} = 0\text{ V}$
Input (IN)						
High Level Input Voltage	V_{INH}	3.0	-	-	V	
Low Level Input Voltage	V_{INL}	-	-	1.5	V	
Input hysteresis Voltage	V_{INHYS}	-	0.2	-	V	
High Level Input Current	I_{INH}	-	50	150	μA	$V_{IN} = 5\text{ V}$
Low Level Input Current	I_{INL}	-1	0	+1	μA	$V_{IN} = 0\text{ V}$

Electrical Characteristics – Continued
(Unless otherwise specified, $-40\text{ °C} \leq T_j \leq +150\text{ °C}$, $V_{DD} = 5\text{ V}$)

Parameters	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Power MOS Output						
On-state Resistance	$R_{DS(ON)}$	-	80	104	m Ω	$V_{DD} = 5\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $T_j = 25\text{ °C}$
		-	150	180	m Ω	$V_{DD} = 5\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $T_j = 150\text{ °C}$
Leak Current	$I_{OUT(L)}$	-	0.0	0.5	μA	$V_{STBY} = 0\text{ V}$, $V_{OUT} = 18\text{ V}$, $T_j = 25\text{ °C}$
		-	1	20	μA	$V_{STBY} = 0\text{ V}$, $V_{OUT} = 18\text{ V}$, $T_j = 150\text{ °C}$
Output Clamp Voltage	$V_{OUT(CL)}$	42	48	52	V	$V_{IN} = 0\text{ V}$, $I_{OUT} = 1\text{ mA}$
Turn-ON Delay Time 1	t_{ONDLY1}	-	38	60	μs	$V_{DD} = 5\text{ V}$, $R_L = 10\ \Omega$, $R_{SR} = 24\text{ k}\Omega$, $V_{BAT} = 12\text{ V}$
Turn-OFF Delay Time 1	$t_{OFFDLY1}$	-	95	145	μs	
Fall Time 1	t_{F1}	28	40	52	μs	
Rise Time 1	t_{R1}	28	40	52	μs	
Slew Rate ON 1	SR_{ON1}	0.138	0.180	0.257	V/ μs	
Slew Rate OFF 1	SR_{OFF1}	0.138	0.180	0.257	V/ μs	
Turn-ON Delay Time 2	t_{ONDLY2}	-	105	155	μs	
Turn-OFF Delay Time 2	$t_{OFFDLY2}$	-	266	410	μs	
Fall Time 2	t_{F2}	78	113	147	μs	
Rise Time 2	t_{R2}	78	113	147	μs	
Slew Rate ON 2	SR_{ON2}	0.049	0.064	0.092	V/ μs	
Slew Rate OFF 2	SR_{OFF2}	0.049	0.064	0.092	V/ μs	
Turn-ON Delay Time 3	t_{ONDLY3}	-	230	335	μs	$V_{DD} = 5\text{ V}$, $R_L = 10\ \Omega$, $R_{SR} = 150\text{ k}\Omega$, $V_{BAT} = 12\text{ V}$
Turn-OFF Delay Time 3	$t_{OFFDLY3}$	-	585	904	μs	
Fall Time 3	t_{F3}	174	249	324	μs	
Rise Time 3	t_{R3}	174	249	324	μs	
Slew Rate ON 3	SR_{ON3}	0.022	0.029	0.041	V/ μs	
Slew Rate OFF 3	SR_{OFF3}	0.022	0.029	0.041	V/ μs	

Electrical Characteristics – Continued
(Unless otherwise specified, $-40\text{ °C} \leq T_j \leq +150\text{ °C}$, $V_{DD} = 5\text{ V}$)

Parameters	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
SR Pin						
SR Output Voltage	V_{SR}	0.95	1.00	1.05	V	$V_{DD} = V_{STBY} = 5\text{ V}$, $R_{SR} = 68\text{ k}\Omega$
Diagnostic Output						
ST Low Voltage ^(Note 1)	$V_{ST(L)}$	-	-	0.5	V	$I_{ST} = 1\text{ mA}$
ST Leak Current	$I_{ST(L)}$	-	-	1	μA	$V_{ST} = 5\text{ V}$
ST Detection Delay Time ^(Note 1)	t_{STDET}	-	-	65	μs	
ST Release Delay Time ^(Note 1)	t_{STREL}	-	-	10	μs	
Protection Function						
Over Current Limitation Level	$I_{OUT(LIM)}$	5.0	7.5	10.0	A	$T_j = 25\text{ °C}$
Thermal Shutdown Detected Temperature ^(Note 1)	T_{TSDD}	150	175	-	$^{\circ}\text{C}$	
Thermal Shutdown Released Temperature ^(Note 1)	T_{TSDR}	135	160	-	$^{\circ}\text{C}$	
Thermal Shutdown Hysteresis Temperature ^(Note 1)	T_{TSDHYS}	-	15	-	$^{\circ}\text{C}$	
ΔT_j Protection Detected Temperature ^(Note 1)	T_{DTJD}	-	93	-	$^{\circ}\text{C}$	
ΔT_j Protection Released Temperature ^(Note 1)	T_{DTJR}	-	43	-	$^{\circ}\text{C}$	
ΔT_j Protection Hysteresis Temperature ^(Note 1)	T_{DTJHYS}	-	50	-	$^{\circ}\text{C}$	

(Note 1): Not 100 % tested.

Typical Performance Curves
 (Unless otherwise specified, $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V}$)

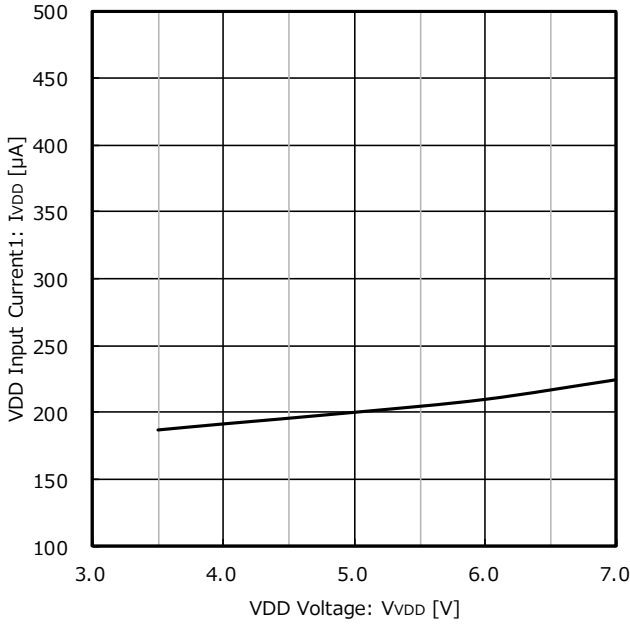


Figure 1. Operating Current vs VDD Input Voltage

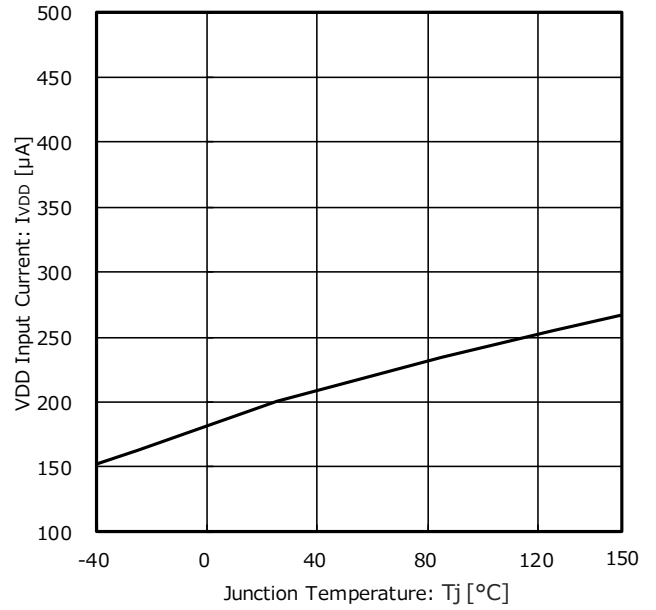


Figure 2. Operating Current vs Junction Temperature

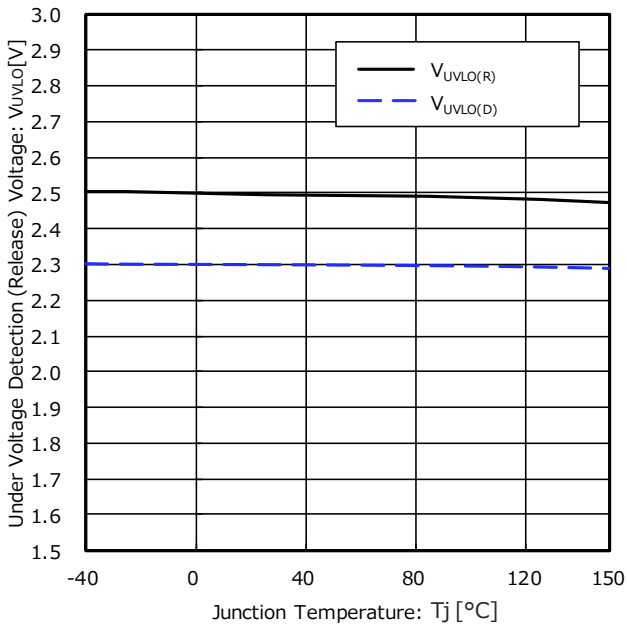


Figure 3. Under Voltage Detection (Release) Voltage vs Junction Temperature

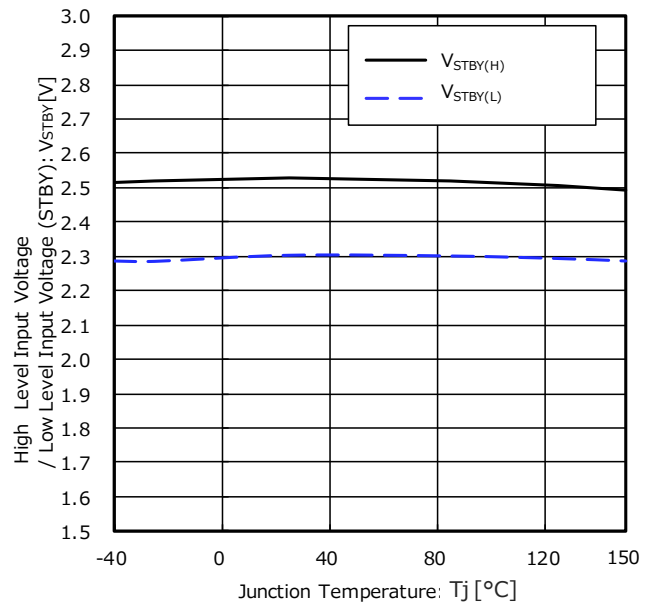


Figure 4. High Level Input Voltage / Low Level Input Voltage (STBY) vs Junction Temperature

Typical Performance Curves - Continued
 (Unless otherwise specified, $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V}$)

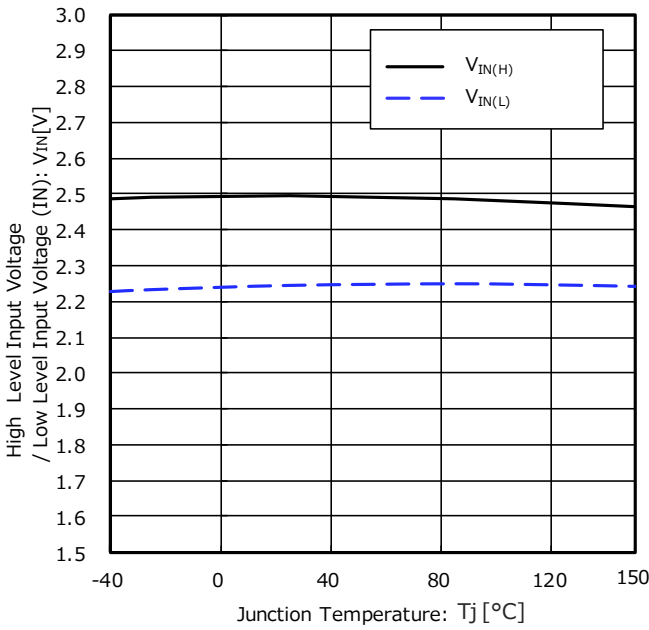


Figure 5. High Level Input Voltage / Low Level Input Voltage (IN) vs Junction Temperature

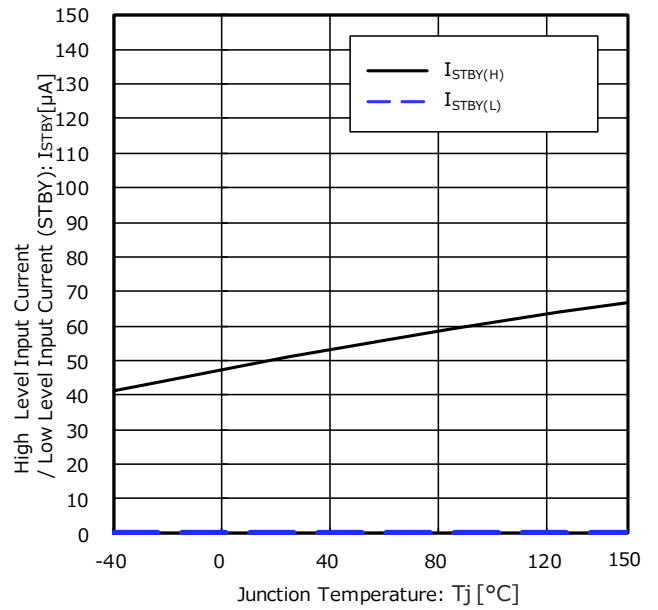


Figure 6. High Level Input Current / Low Level Input Current (STBY) vs Junction Temperature

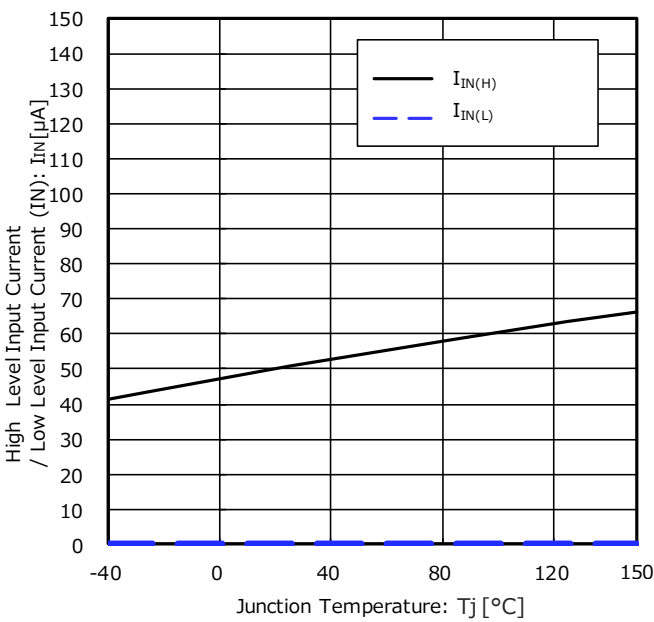


Figure 7. High Level Input Current / Low Level Input Current (IN) vs Junction Temperature

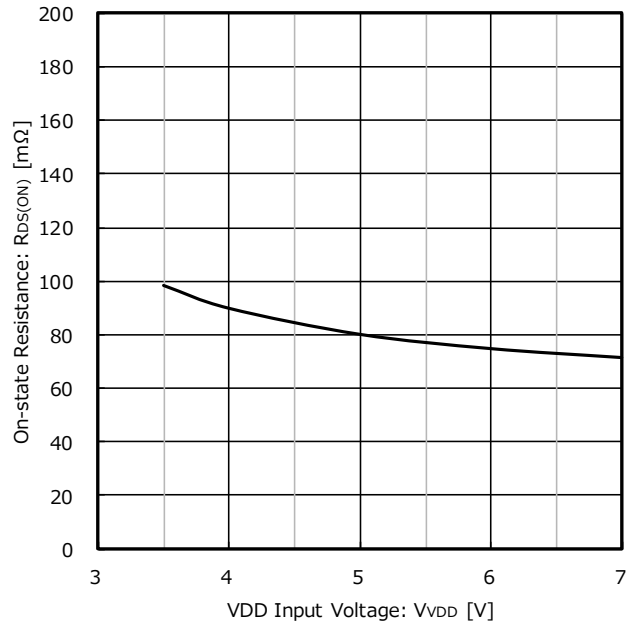


Figure 8. On-state Resistance vs Input Voltage

Typical Performance Curves - Continued
 (Unless otherwise specified, $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V}$)

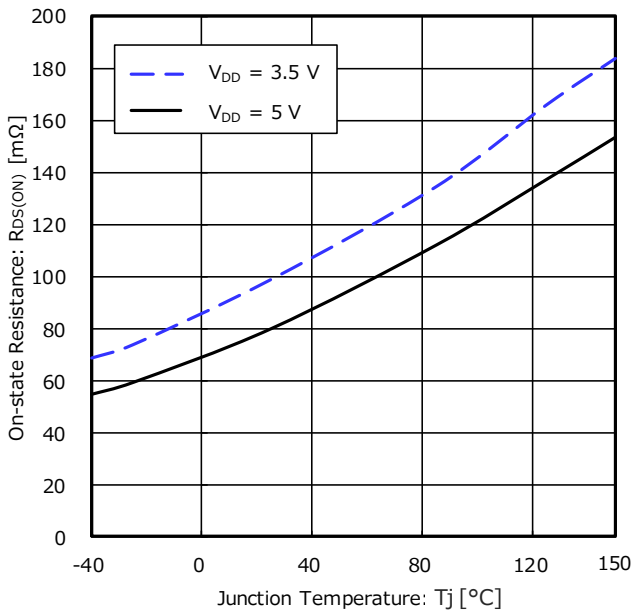


Figure 9. On-state Resistance vs Junction Temperature

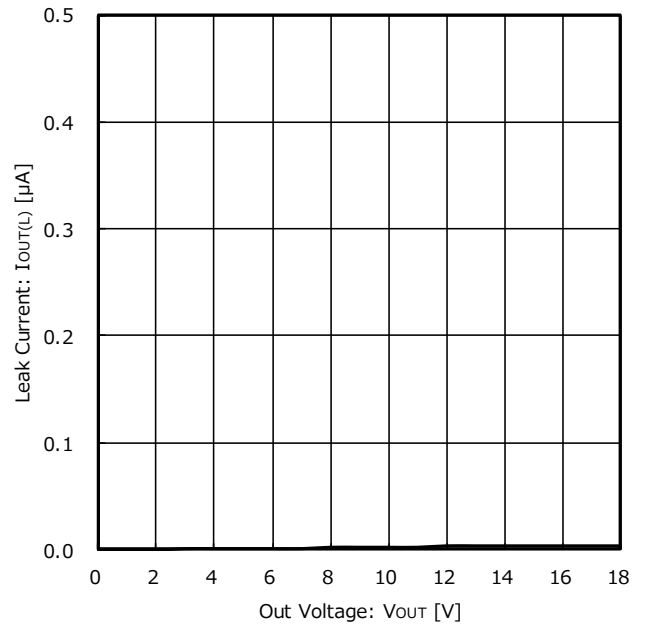


Figure 10. Leak Current vs OUT Voltage

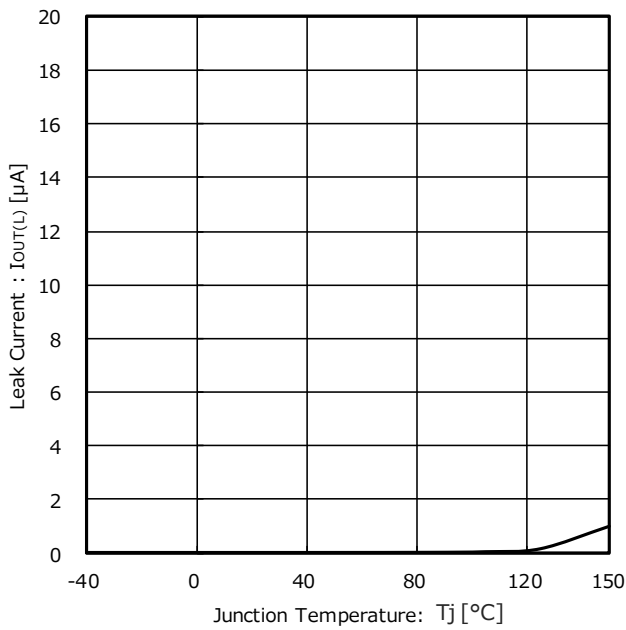


Figure 11. Leak Current vs Junction Temperature

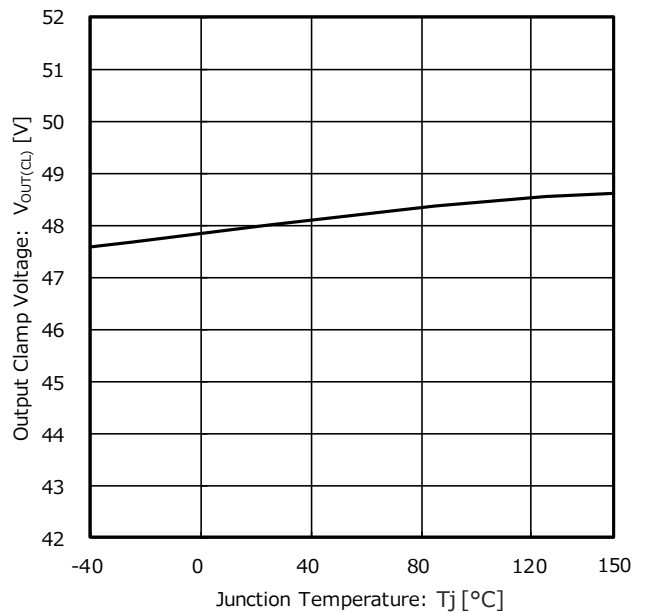


Figure 12. Output Clamp Voltage vs Junction Temperature

Typical Performance Curves - Continued
 (Unless otherwise specified, $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V}$)

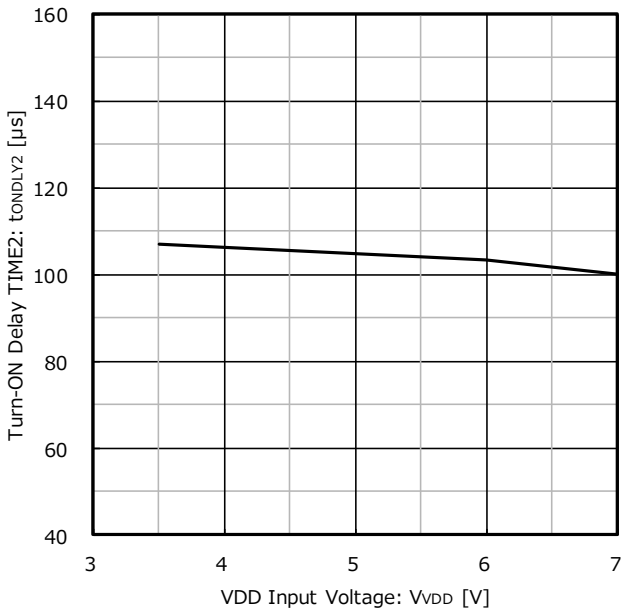


Figure 13. Turn-ON Delay Time2 vs VDD Input Voltage ($R_{SR} = 68\text{ k}\Omega$)

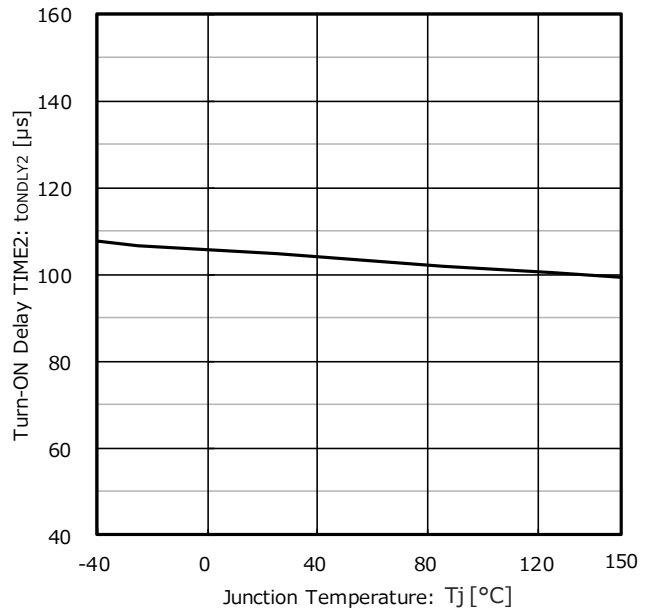


Figure 14. Turn-ON Delay Time2 vs Junction Temperature ($R_{SR} = 68\text{ k}\Omega$)

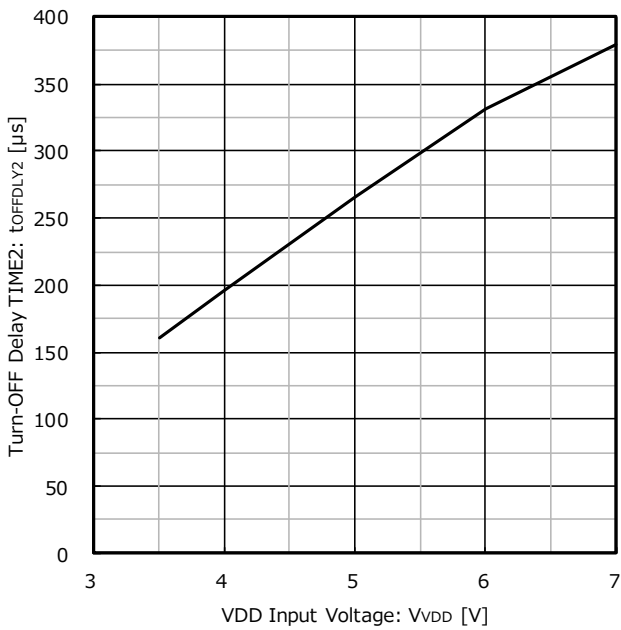


Figure 15. Turn-OFF Delay Time2 vs VDD Input Voltage ($R_{SR} = 68\text{ k}\Omega$)

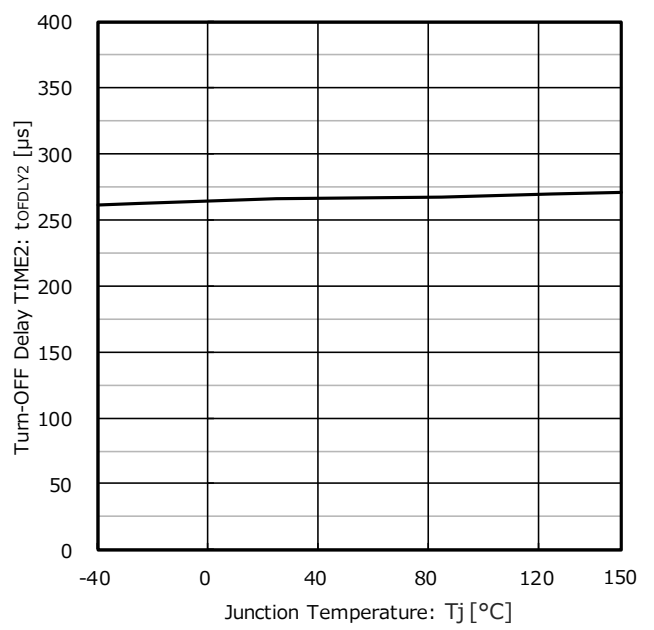


Figure 16. Turn-OFF Delay Time2 vs Junction Temperature ($R_{SR} = 68\text{ k}\Omega$)

Typical Performance Curves - Continued
 (Unless otherwise specified, $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V}$)

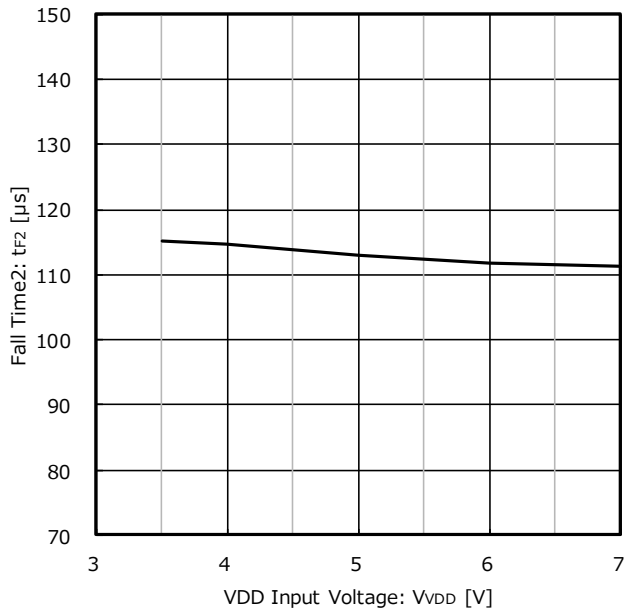


Figure 17. Output Fall Time2 vs VDD Input Voltage
 ($R_{SR} = 68\text{ k}\Omega$)

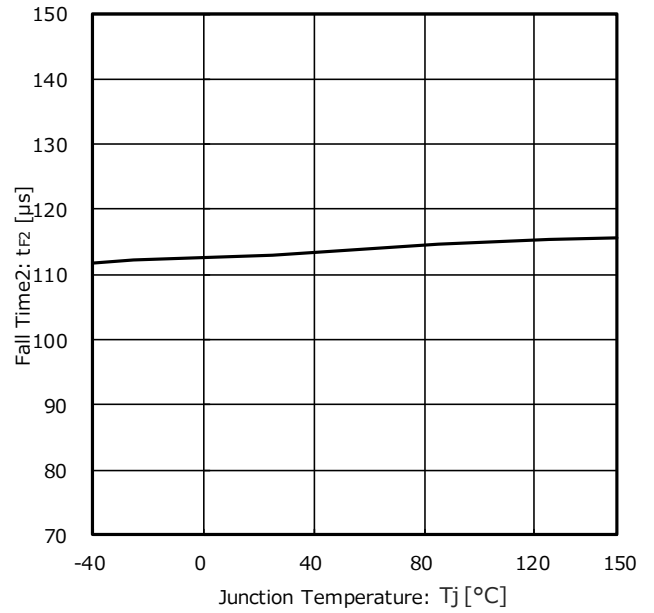


Figure 18. Output Fall Time2 vs Junction Temperature
 ($R_{SR} = 68\text{ k}\Omega$)

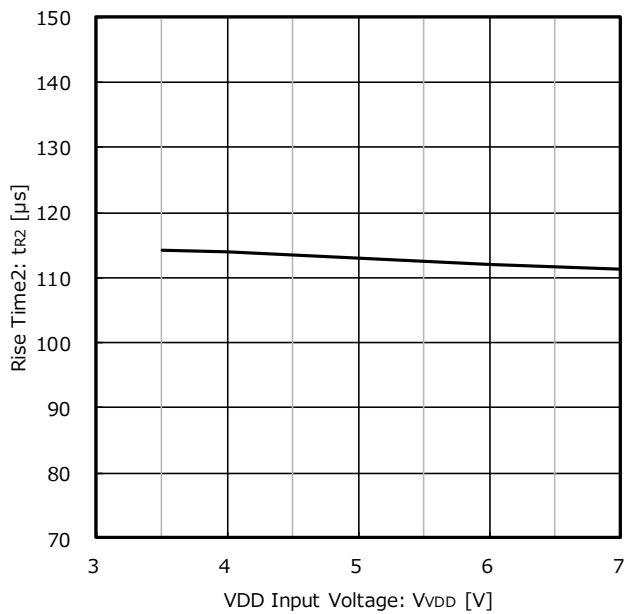


Figure 19. Rise Time2 vs VDD Input Voltage
 ($R_{SR} = 68\text{ k}\Omega$)

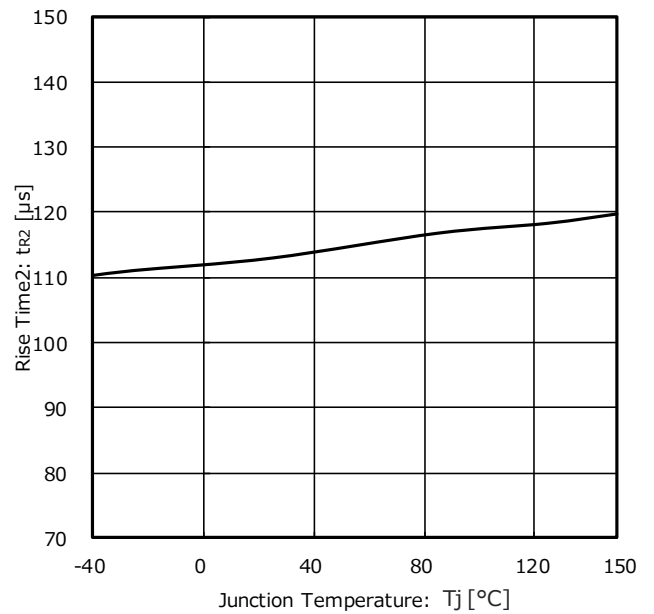


Figure 20. Rise Time2 vs Junction Temperature
 ($R_{SR} = 68\text{ k}\Omega$)

Typical Performance Curves - Continued
 (Unless otherwise specified, $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V}$)

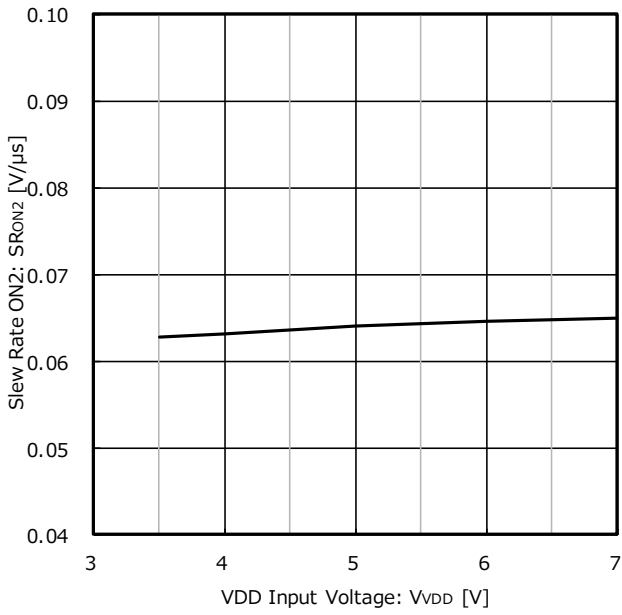


Figure 21. Slew Rate ON2 vs VDD Input Voltage
 ($R_{SR} = 68\text{ k}\Omega$)

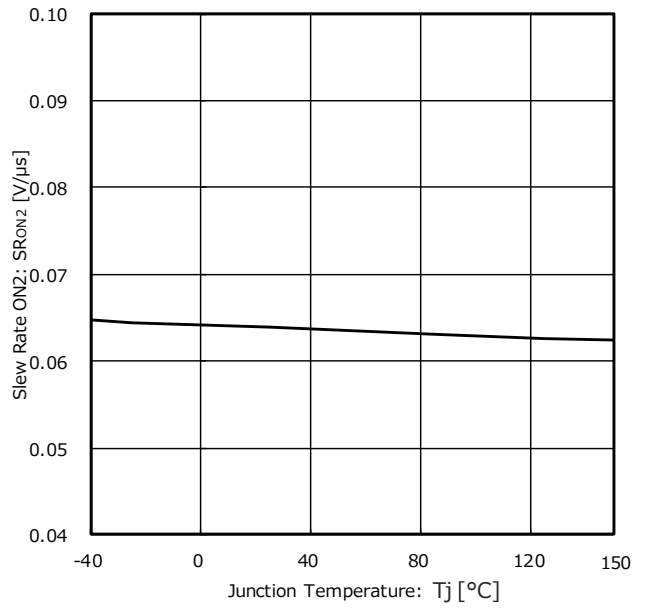


Figure 22. Slew Rate ON2 vs Junction Temperature
 ($R_{SR} = 68\text{ k}\Omega$)

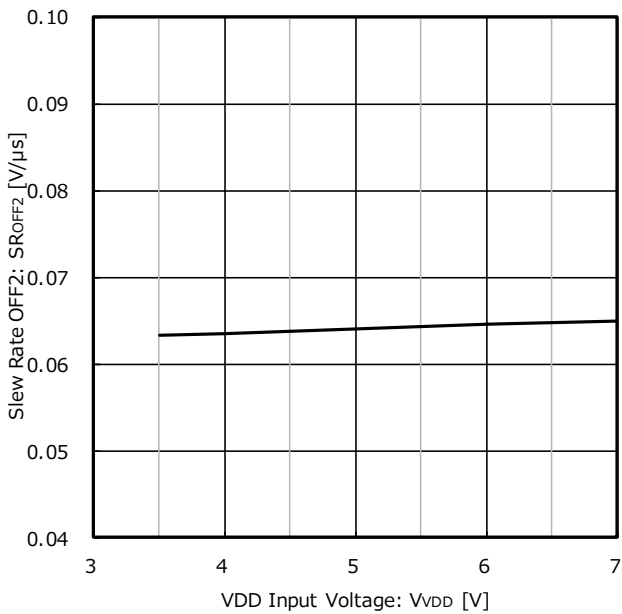


Figure 23. Slew Rate OFF2 vs VDD Input Voltage
 ($R_{SR} = 68\text{ k}\Omega$)

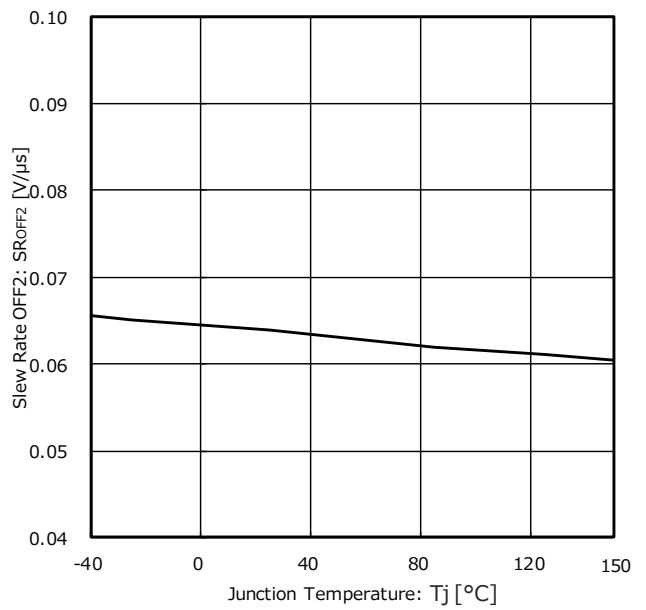


Figure 24. Slew Rate OFF2 vs Junction Temperature
 ($R_{SR} = 68\text{ k}\Omega$)

Typical Performance Curves - Continued
 (Unless otherwise specified, $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V}$)

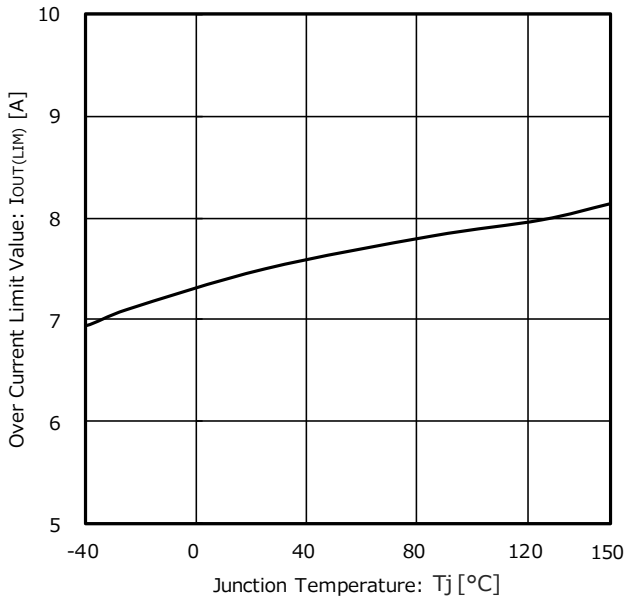


Figure 25. Over Current Limit Value vs Junction Temperature

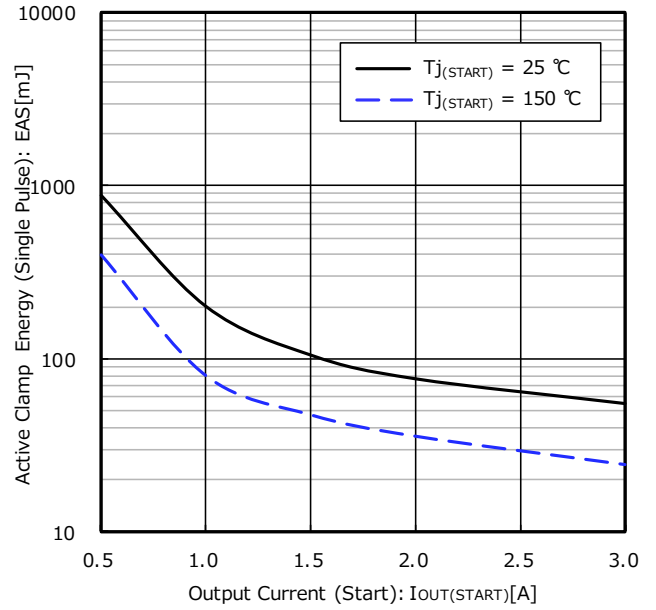
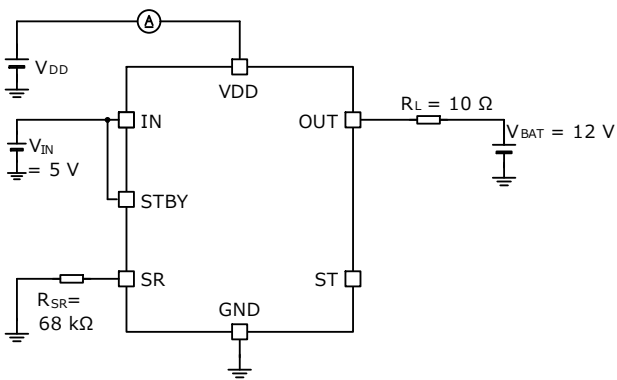
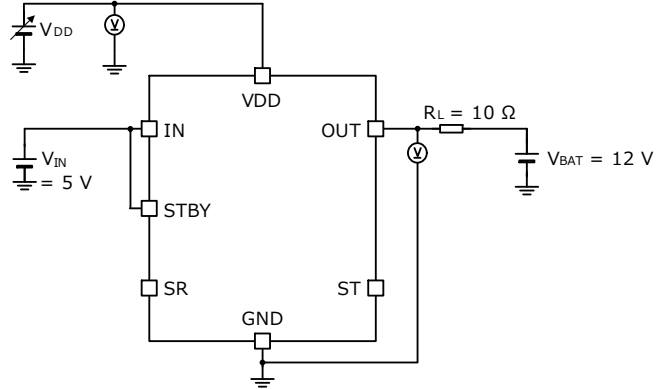


Figure 26. Active Clamp Energy (Single Pulse) vs Output Current (Start)

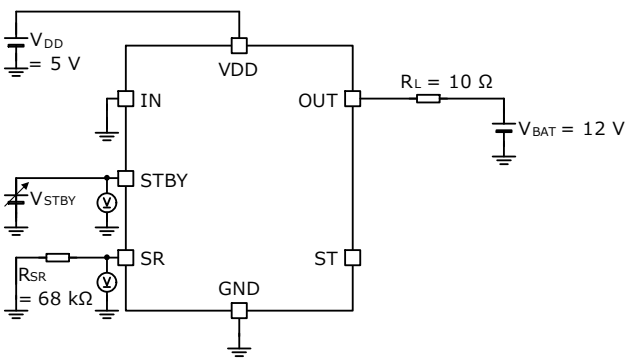
Measurement Circuit



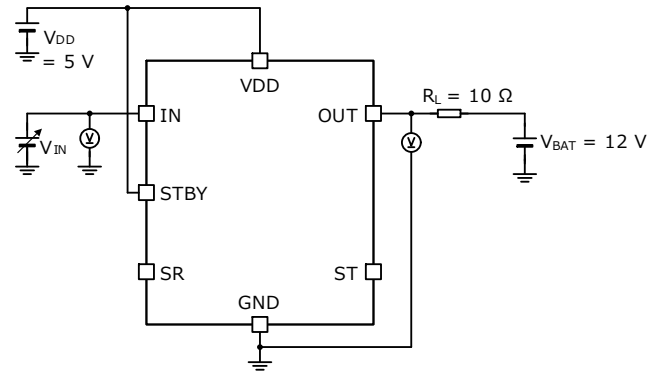
Measurement Circuit for Figure 1 and Figure 2



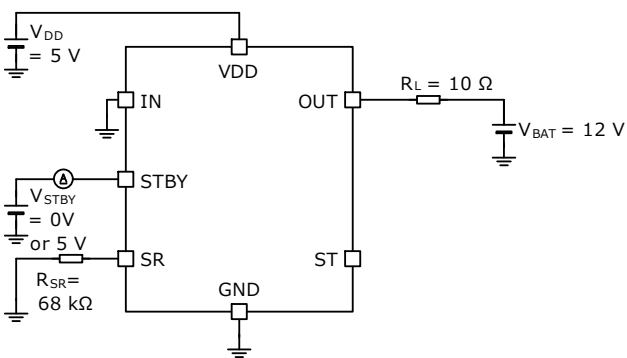
Measurement Circuit for Figure 3



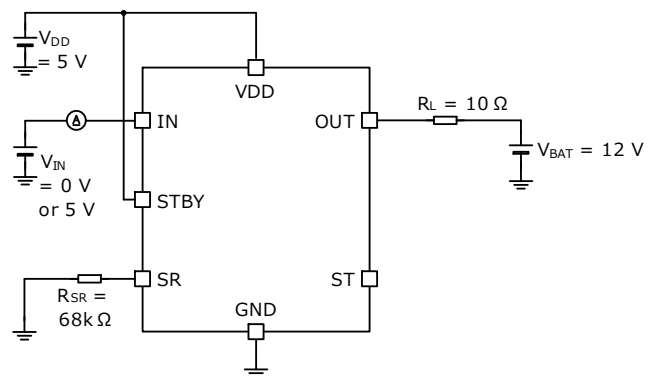
Measurement Circuit for Figure 4



Measurement Circuit for Figure 5

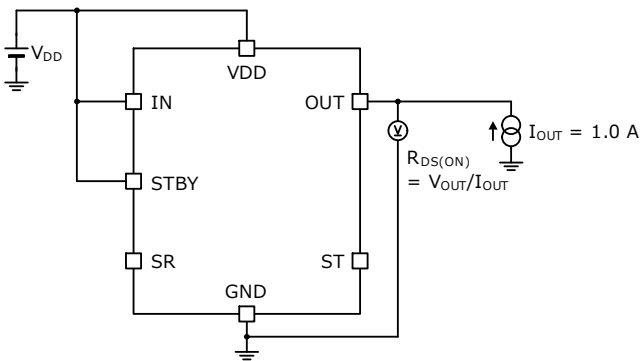


Measurement Circuit for Figure 6

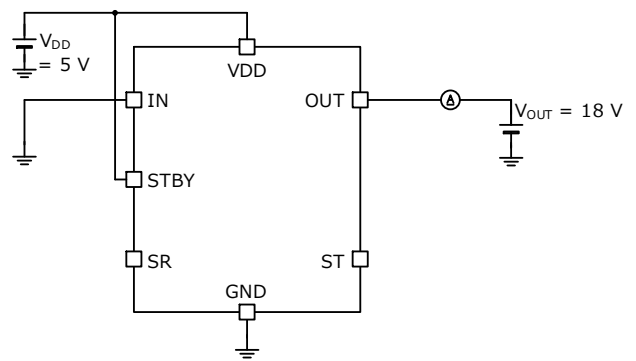


Measurement Circuit for Figure 7

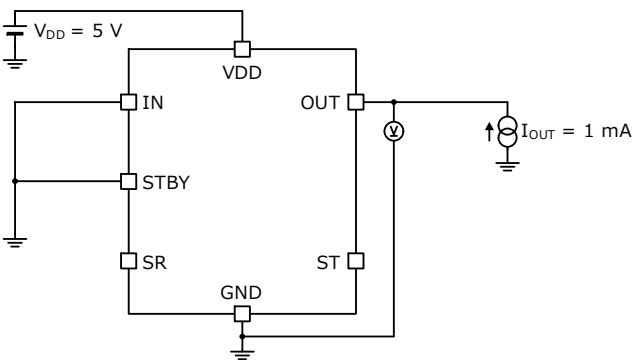
Measurement Circuit – Continued



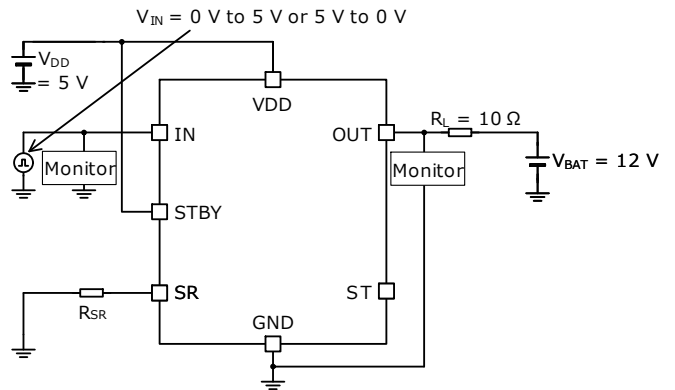
Measurement Circuit for Figure 8 and Figure 9



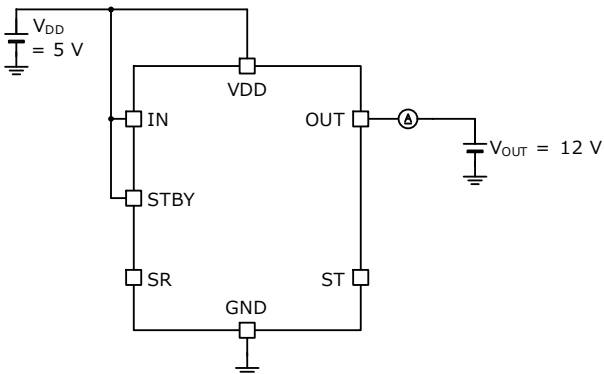
Measurement Circuit for Figure 10 and Figure 11



Measurement Circuit for Figure 12



Measurement Circuit for Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, Figure 19, Figure 20, Figure 21, Figure 22, Figure 23 and Figure 24



Measurement Circuit for Figure 25

Truth Table

■ **OUT Output and Diagnostic Output Function**

Performs diagnostic test to check for any abnormal conditions and output to the ST pin. Once Thermal Shutdown is detected, the ST pin is latched Low. ST pin Low latch is released by setting the STBY pin to Low or set VDD voltage to "Low Voltage Detection ($V_{UVLO} - V_{UVLOHYS}$)"

STBY Pin Voltage	Power Supply (VDD) Under Voltage Detection	IN Pin Voltage	TSD	ΔT_j	OCP	Output State	
						OUT Pin	ST Pin
Low	*	*	*	*	*	OFF	High
High	Detected	*	*	*	*	OFF	High
High	Undetected	Low	*	*	*	OFF	High
High	Undetected	High	Detected	*	*	OFF	Low
High	Undetected	High	Undetected	Detected	*	OFF	High
High	Undetected	High	Undetected	Undetected	No Limit	ON	High
High	Undetected	High	Undetected	Undetected	Limited	Current Limitation	High

Timing Chart

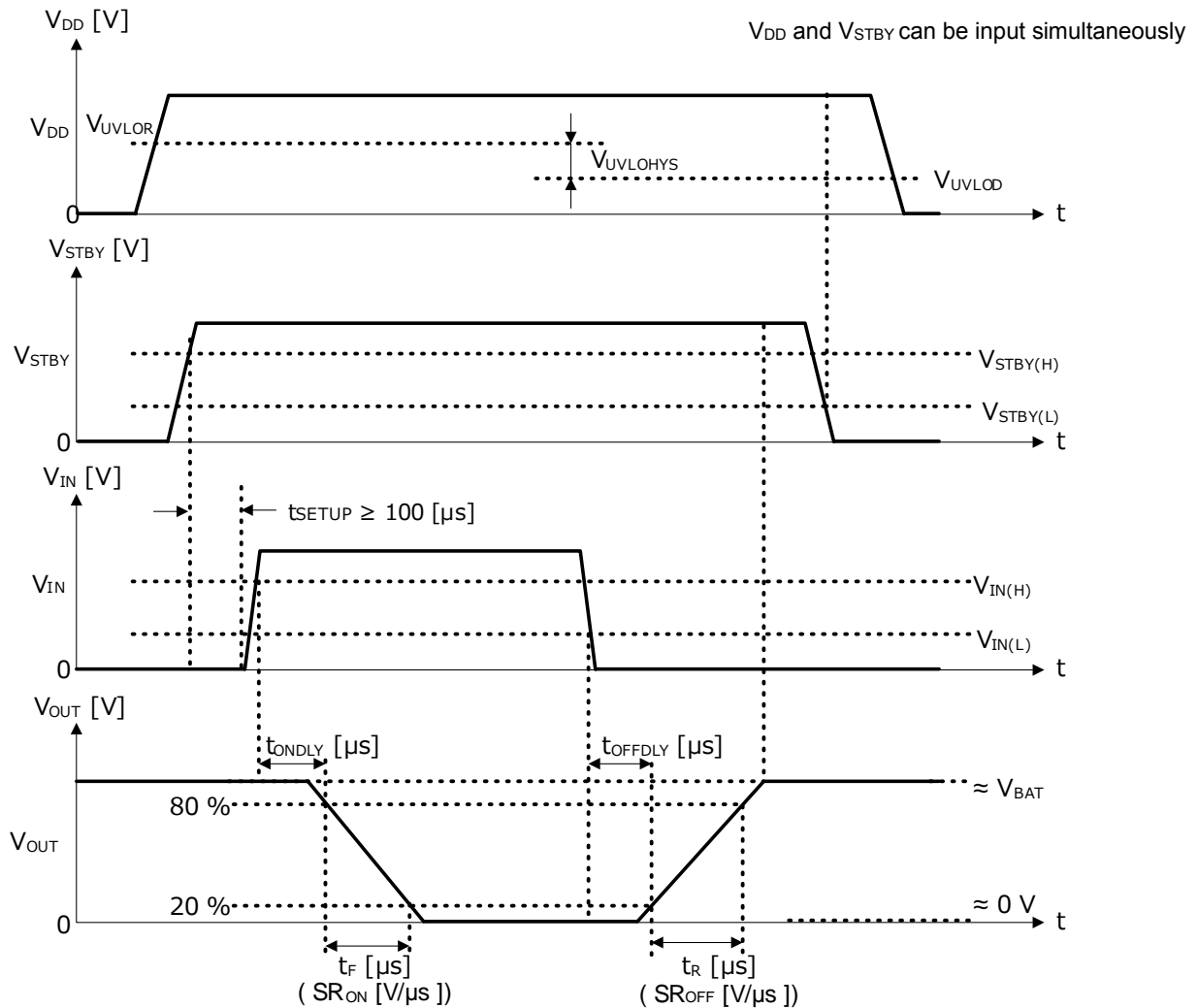


Figure 27. Definition of Turn-ON TIME, Turn-OFF TIME, Fall TIME (Slew Rate ON), and Rise TIME (Slew Rate OFF)

Timing Chart — Continued

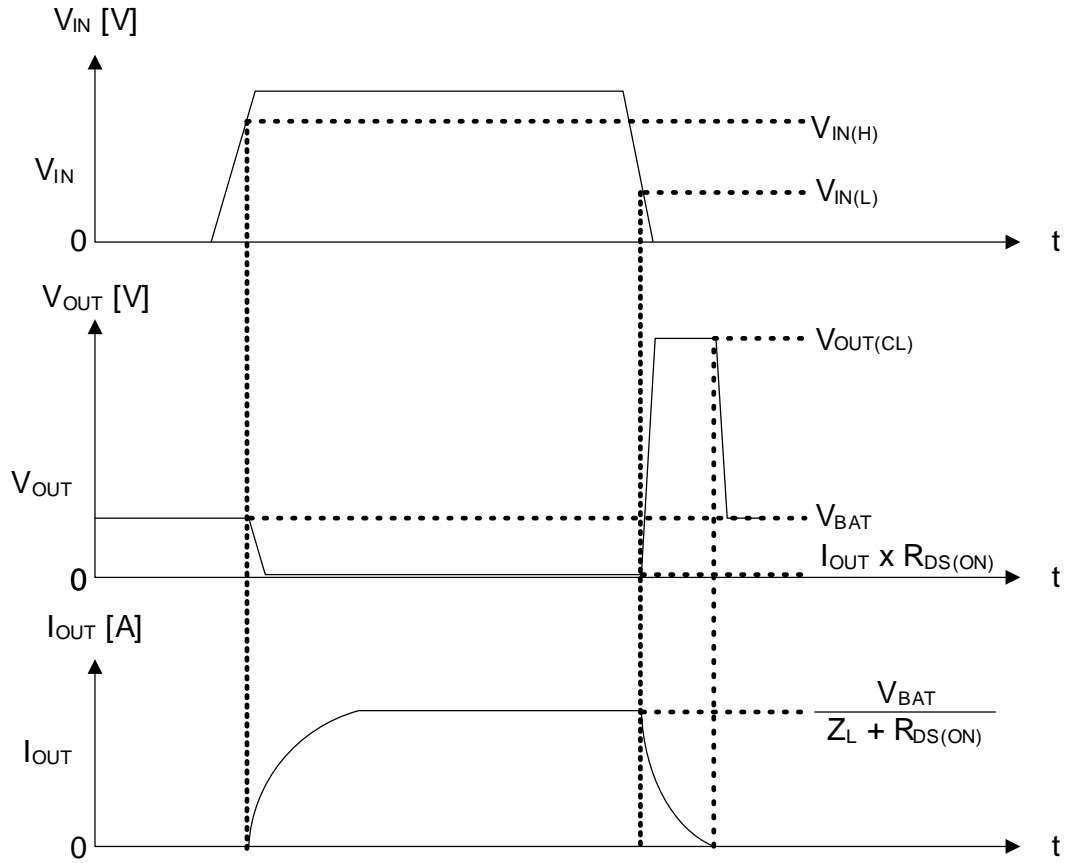


Figure 28. Inductive Load Operation

Function Description

Over Current Protection Function

This IC built-in over current protection function. Following is shown that the timing chart of over current protection function.

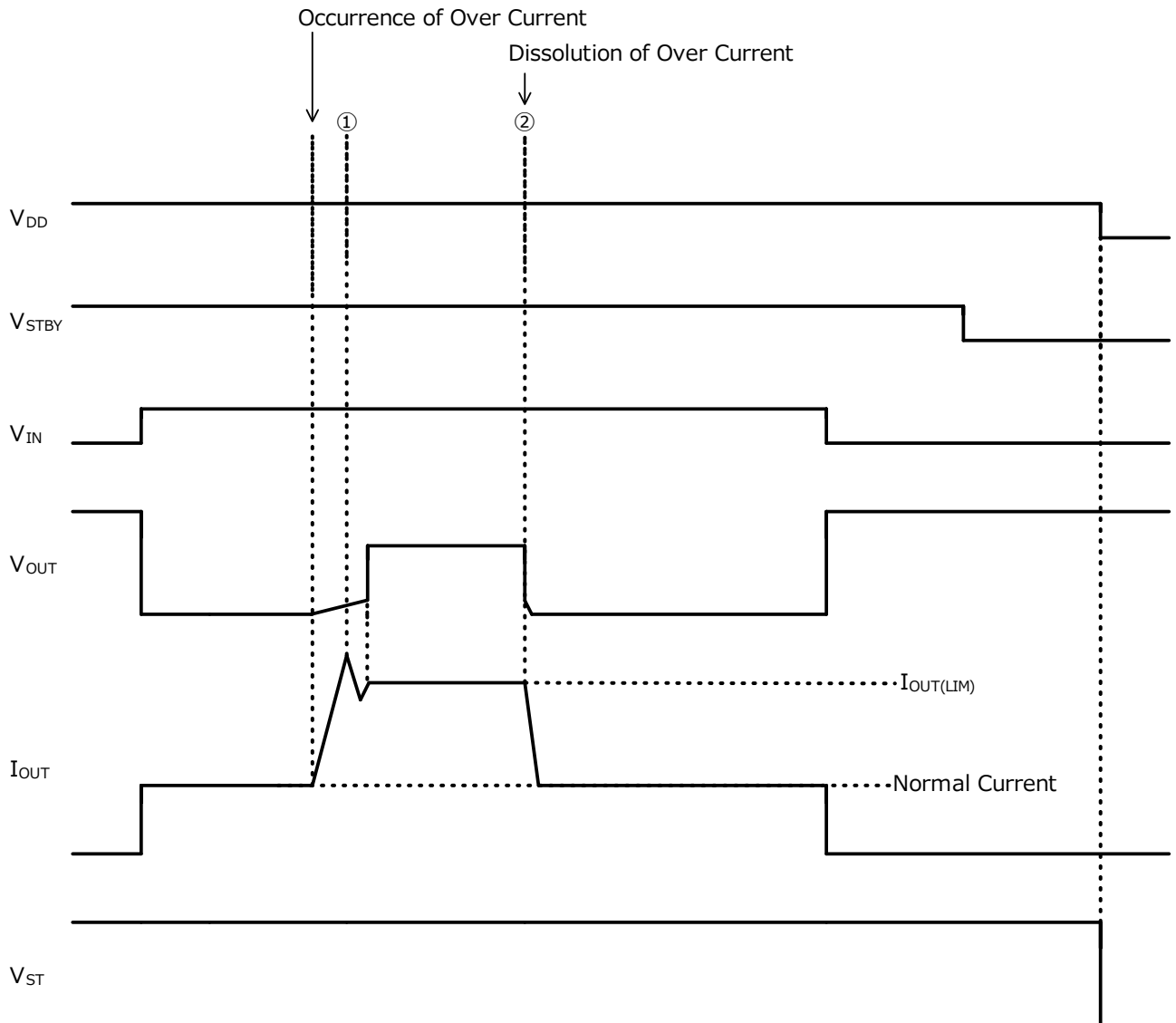


Figure 29. Timing Chart of OCP Function

- ① When an overcurrent occurs, I_{OUT} is controlled by the overcurrent limit level ($I_{OUT(LIM)}$) and V_{OUT} rises. $I_{OUT(LIM)}$ is 7.5 A (Typ). The V_{ST} does not change at this time.
- ② When the overcurrent disappears, the over current limit is released.

Function Description – Continued

■ Dual TSD Function

This IC has a built-in TSD function and ΔT_j protection function. Following is shown that the timing chart of Dual TSD function.

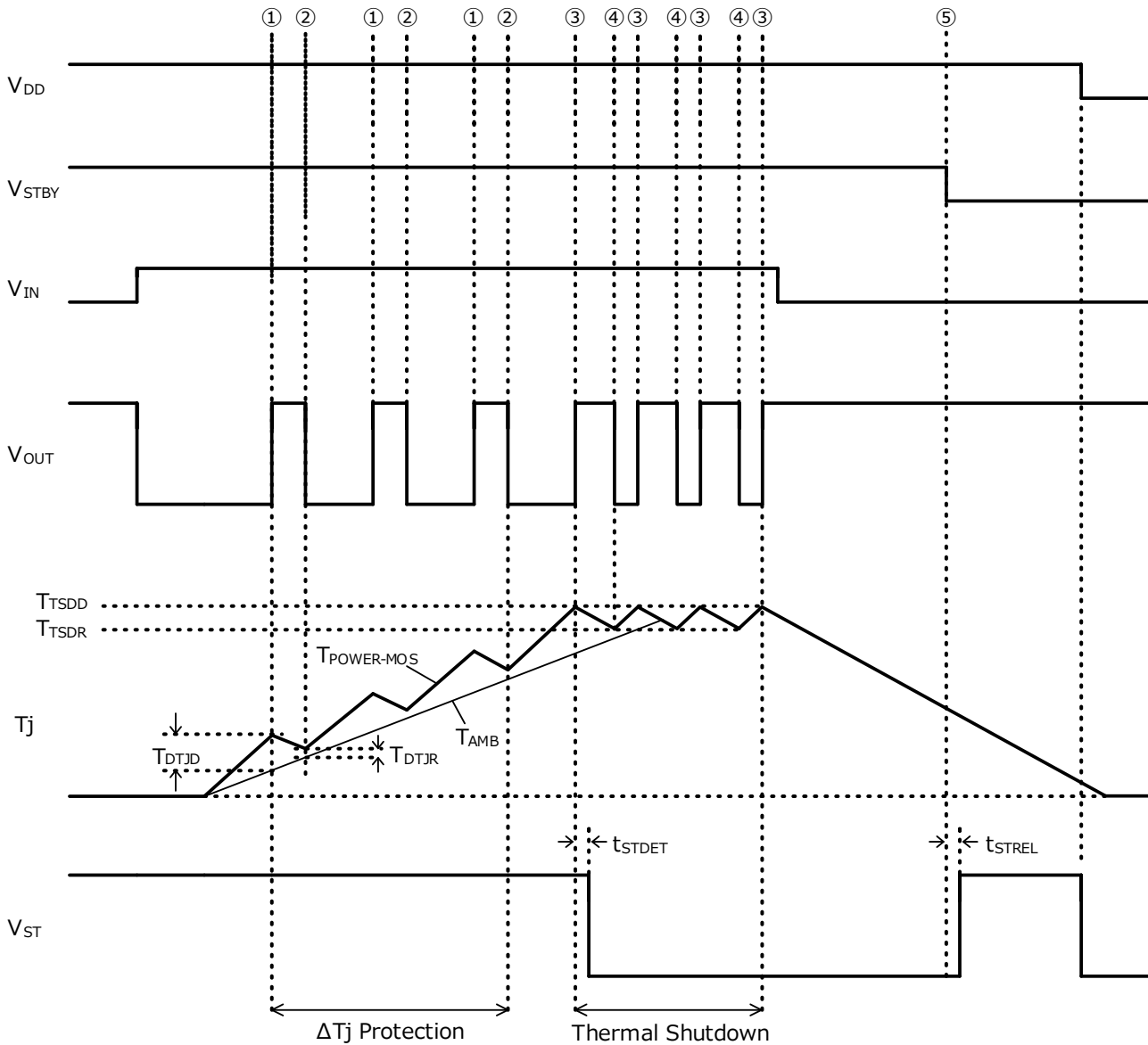


Figure 27. Timing Chart of Dual TSD Function

- ① The temperature of Power MOS FET part and the control part in his IC is each $T_{POWER-MOS}$, T_{AMB} . When the temperature difference becomes 93 °C (Typ) or more, the output turns OFF. This temperature defines as ΔT_j Protection Detected Temperature (T_{DTJD}). At This time, the V_{ST} does not change.
- ② When the temperature difference of $T_{POWER-MOS}$ and T_{AMB} becomes 43 °C (Typ) or less, the output turns automatically ON. This temperature defines as ΔT_j Protection Released Temperature (T_{DTJR}).
- ③ The output is turned off when the temperature of the IC reaches Thermal Shutdown Detected Temperature (T_{SDSD}) = 175 °C (Typ) or more. At this time, the V_{ST} latches Low.
- ④ The output returns to its normal state when the temperature of the IC becomes Thermal Shutdown Released Temperature (T_{SDSR}) = 160 °C (Typ) or less. V_{ST} keeps latching Low.
- ⑤ the V_{ST} become High after t_{STREL} when the V_{STBY} become Low.

Function Description — Continued

■ Slew rate control function

This IC can variably adjust the rise time (Slew Rate ON) and fall time (Slew Rate OFF) of OUT output voltage by setting the SR pin external resistor (R_{SR}).

Rise (fall) time: $t_R(t_F) = (1.636 \times R_{SR}) / 1000 + 3.73$ [μs]

Slew Rate ON (OFF): $SR_{ON}(SR_{OFF}) = 1/t_F(1/t_R)$ [$\text{V} / \mu\text{s}$]

R_{SR} recommended range: 24 k Ω to 150 k Ω

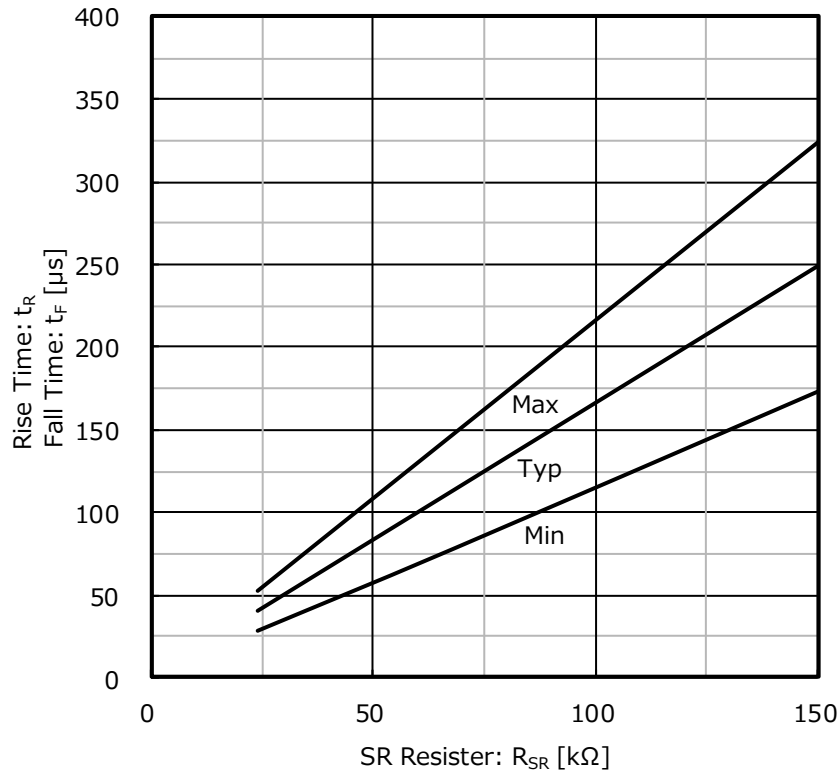
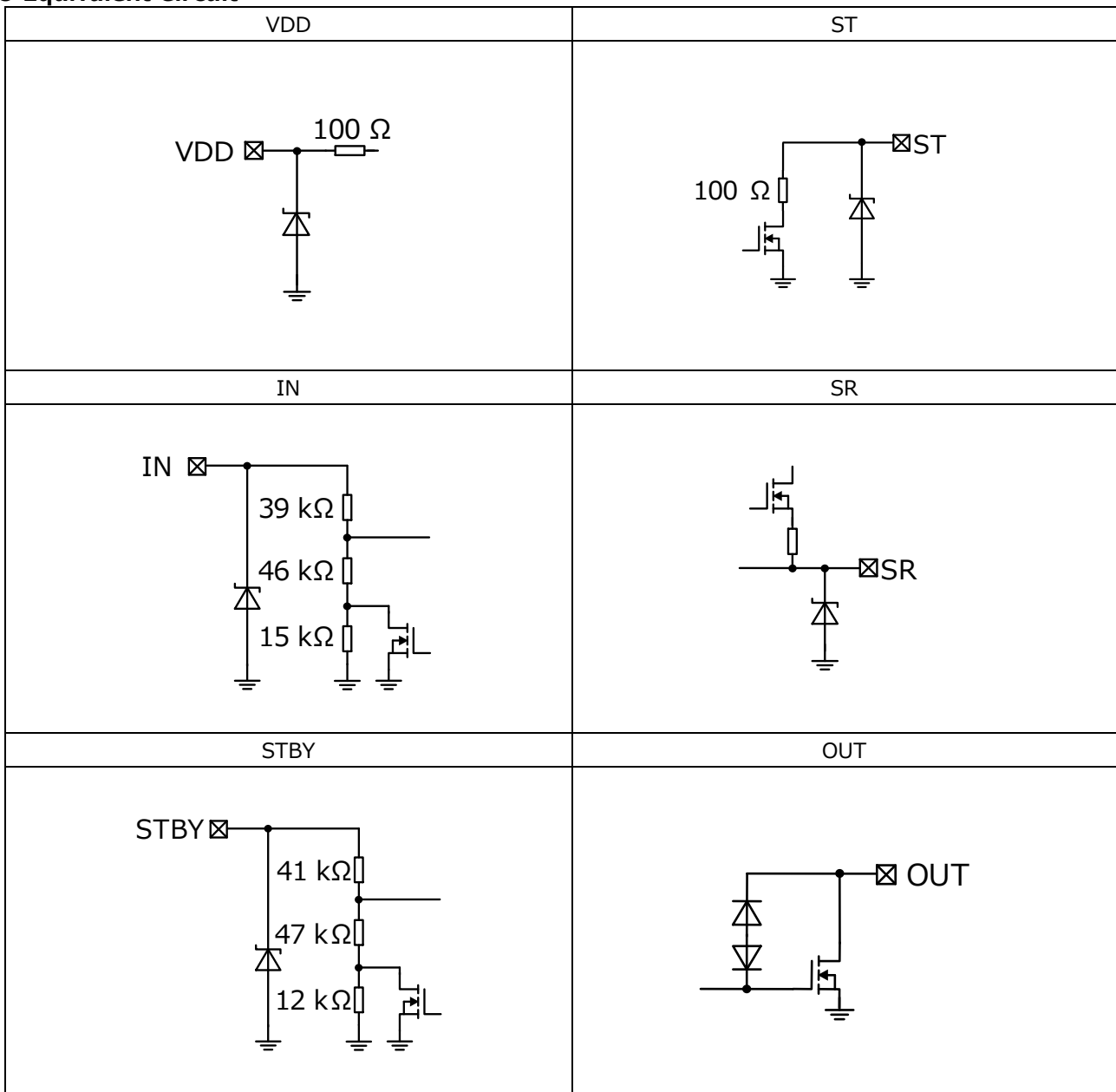


Figure 31. Output rise (fall) time vs The SR pin resistance

I/O Equivalent Circuit



Resistor values in the figure are typical values.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes — Continued**9. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

10. Thermal Shutdown Function (TSD)

This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD function that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

11. Over Current Protection Function (OCP)

This IC incorporates an integrated overcurrent protection function that is activated when the load is shorted. This protection function is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection function.

12. Active Clamp Operation

The IC integrates the active clamp function to internally absorb the reverse energy which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy is active clamp tolerance (refer to Figure CC. graph title) or under when inductive load is used.

13. Negative Current of Output

When the OUT pin (DRAIN) becomes lower than the GND pin (SOURCE) voltage, a current flow from power supply pin (VDD) and the input pins (the STBY pin and the IN pin) to the OUT pin through a parasitic transistor. When the power supply pin is high, as shown in Figure 31, when the input pins are high, as shown in Figure 32, a current flow from the power supply pin and the input pins of connected parts (LDO, MCU, etc.) to the OUT pin. When the power supply pin is low, as shown in Figure 33, and when the input pins are low, as shown in Figure 34, a current flow from the power supply pin and the GND of parts (LDO, MCU, etc.) that connected to the input pins to the OUT pin.

Therefore, set the OUT pin (DRAIN) is -0.3 V or higher. When the OUT pin becomes lower than -0.3 V, add a restriction resistance $82\ \Omega$ or higher to the VDD pin, a restriction resistance $1\text{k}\ \Omega$ or higher to the STBY pin and a restriction resistance $1\text{k}\ \Omega$ or higher to the IN pin. However, set the value of restriction resistance in consideration of the voltage descent caused by power supply pin and input pins currents.

13. Negative Current of Output — Continued

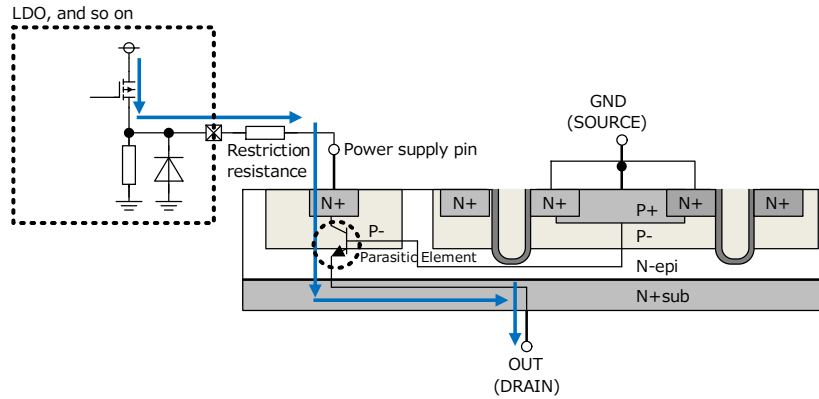


Figure 31. Negative Current Path (when the power supply pin is High)

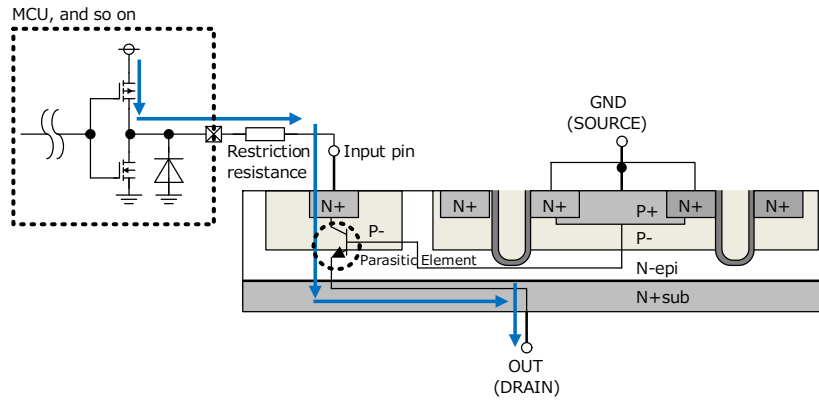


Figure 32. Negative Current Path (when the input pins are High)

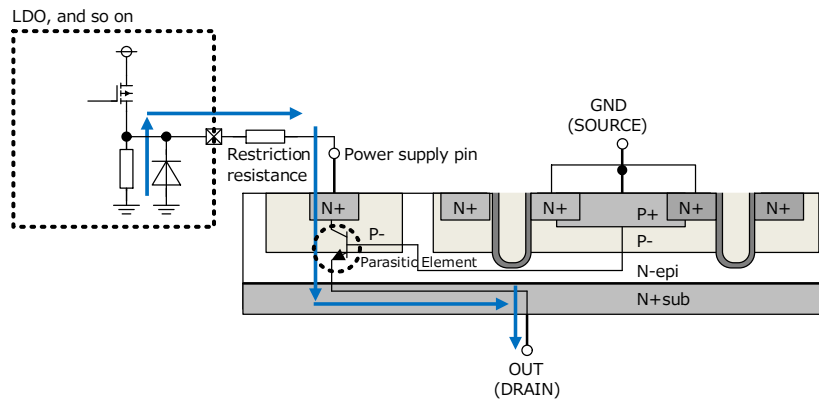


Figure 33. Negative Current Path (when the power supply pin is Low)

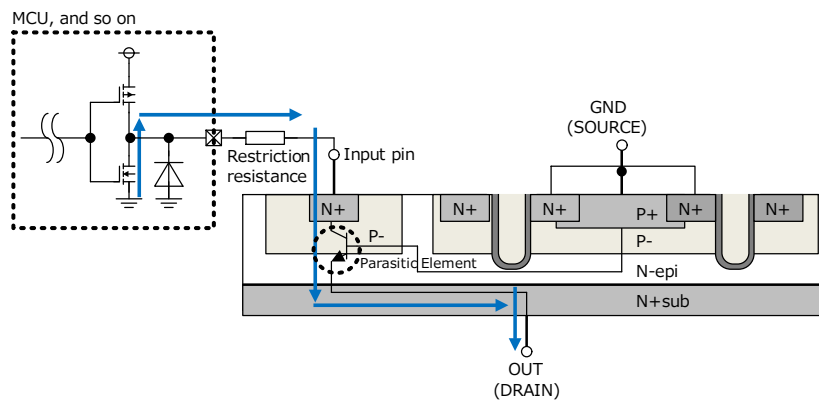


Figure 34. Negative Current Path (when the input pins are Low)

Operational Notes — Continued

14. Power Supply Steep Fluctuation

If the voltage of the power supply pin (VDD) falls sharply, the output pin (OUT) may temporarily turn off as shown in Figure 35. If the power supply pin is expected to fall sharply, take measures such as inserting a capacitor between the power supply pin and the ground pin so that it falls within the recommended usage range shown in Figure 36.

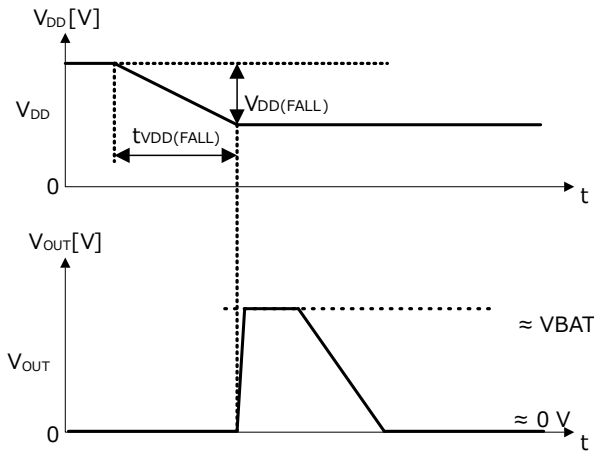


Figure 35. Output OFF Operation when Power Supply Fluctuates Sharply

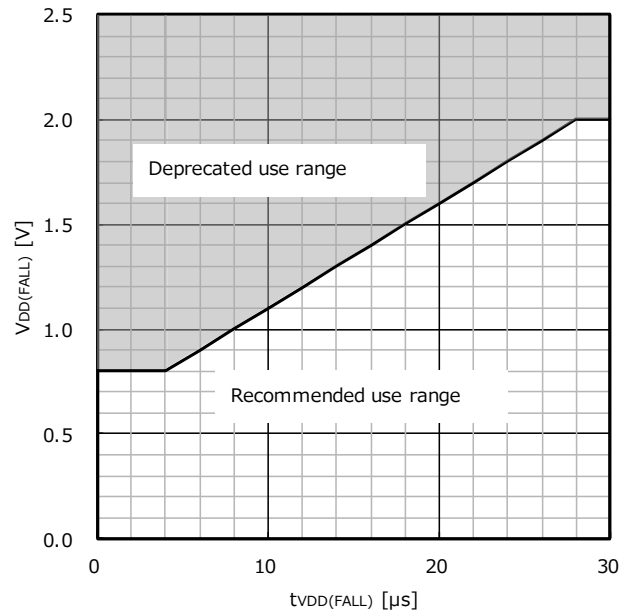
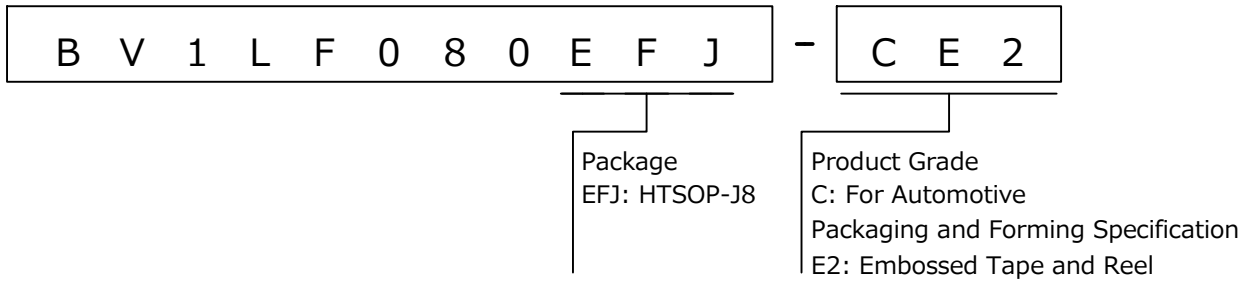
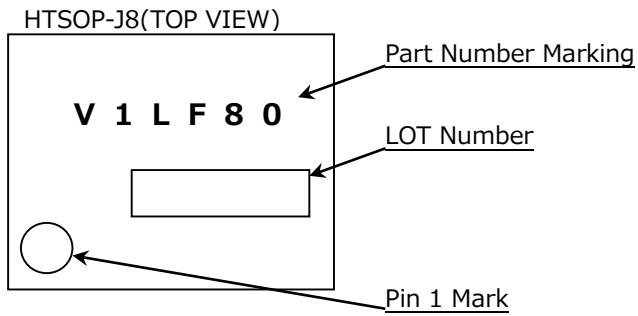


Figure 36. Recommended Use Range

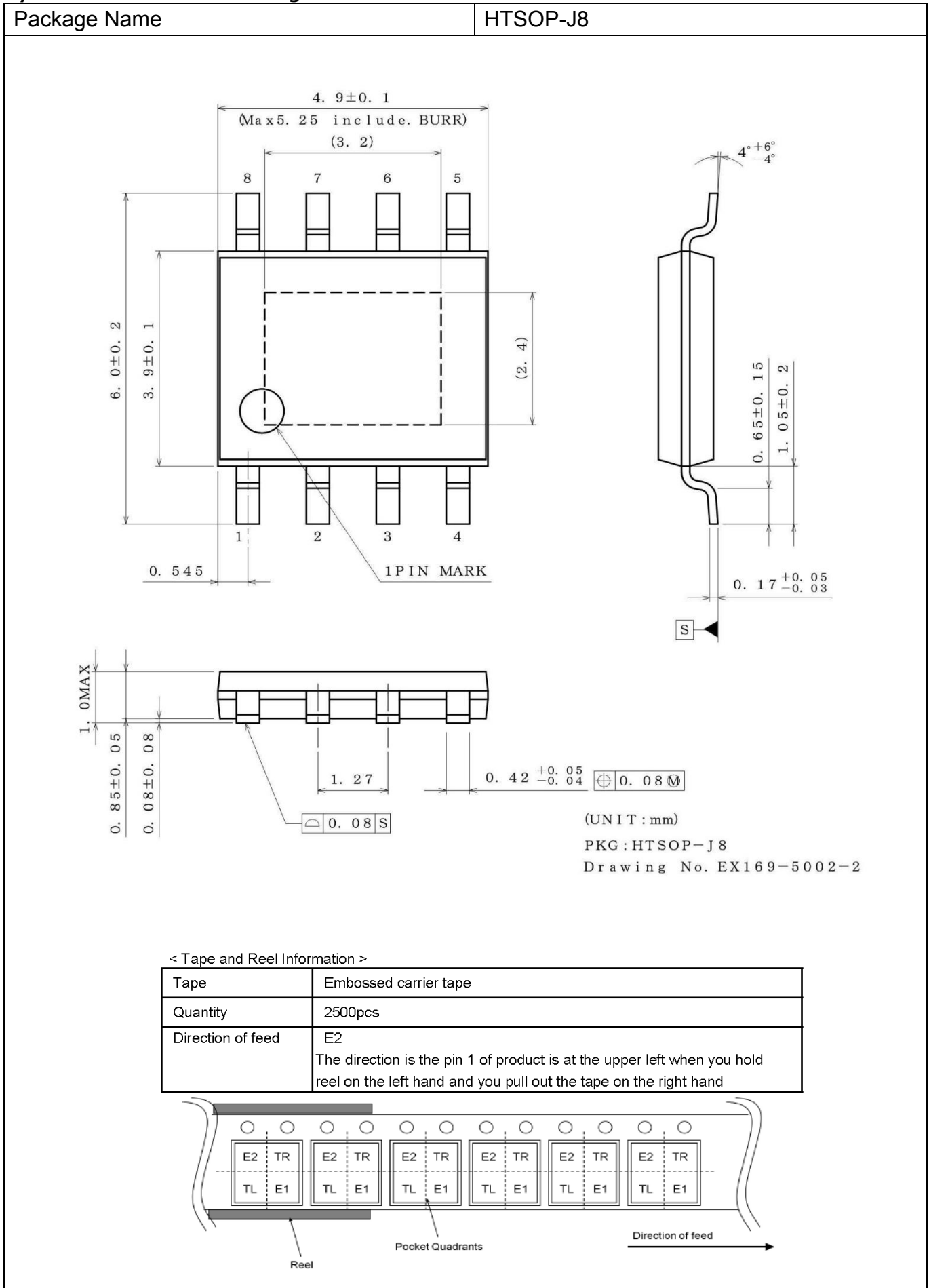
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
24.Jun.2020	001	New release

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CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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