BVA2140

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Device Features

- Small 24-Pin 4 x 4 mm QFN Package
- Integrate Amp1 to DSA and DSA to Amp2 Functionality
- Wide Power supply range of +2.7~5.5V(DSA)
- Single Fixed +5.0V supply(Amp)
- 700-4000MHz Broadband Performance
- 30.2dB Gain at 2.14GHz (Matching Circuit)
- 2.9dB Noise Figure at max gain setting at 2.14GHz(Matching Circuit)
- 25.1dBm P1dB at 2.14GHz (Matching Circuit)
- 40dBm OIP3 at 2.14GHz(10dBm per tone, Matching Circuit)
- 15.2dBm LTE 20MHz ACLR at 1.9GHz (FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. , –50dBc)
- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy(DSA to Amp)
  ±(0.3dB + 5% x Atten) @ 0.7~4GHz
- 1.8V control logic compatible
- Programming modes
  - Serial
- Unique power-up state selection
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package

24-lead 4mm x 4mm x 0.9mm QFN

Figure 1. Package Type

Product Description

The BVA2140 is a digitally controlled variable gain amplifier (DVGA) in a small 4x4mm QFN package, with a broadband frequency range of 700 to 4000 MHz and an operating VDD of 5.0V at 150mA.

BVA2140 is high performance and high dynamic range makes it ideally suited for use in WCDMA/LTE wireless infrastructure point-to-point and other demanding wireless applications.

The BVA2140 is an integration of a high performance digital 6-step attenuator (DSA) that provides a 31.5 dB attenuation range in 0.5 dB steps, and high linearity broadband gain block amplifiers featuring high ACLR and P1.

The BVA2140 digital control interface supports serial programming of the attenuator, and includes the ability to define the initial attenuation state at power-up.

Implementation requires only a few external components, such as DC blocking capacitors on the Input and Output pins, plus a bypass capacitor and a RF choke for the Output port.

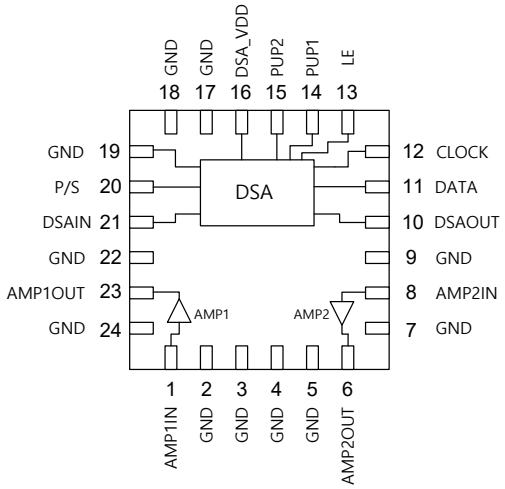


Figure 2. Functional Block Diagram

Application

- Base station/Repeater Infrastructure
- LTE/WCDMA/CDMA Wireless infrastructure and other high performance RF application
- Commercial/Industrial/Military Wireless system
- General purpose Wireless

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			700		4000	MHz
Gain		Attenuation = 0dB, at 2140MHz		30.2		dB
Attenuation Control range		0.5dB step				dB
Attenuation Step				31.5		dB
Attenuation Accuracy	>0.7GHz-4GHz	Any bit or bit combination	±(0.3 + 5% of atten setting)			dB
Return loss (input or output port)	Input Return Loss	Attenuation = 0dB		17		dB
	Output Return Loss			13		
Output Power for 1dB Compression		Attenuation = 0dB , at 2140MHz		25.1		dBm
Output Third Order Intercept Point		Attenuation = 0dB, at 2140MHz		40		dBm
		Pout= +10dBm/tone △f = 1 MHz.				
Noise Figure		Attenuation = 0dB, at 2140MHz		2.9		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		5		V
Supply Current		MCM(AMP1+DSA+AMP2)		150		mA
Control Interface		Serial mode		6		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V, measure on Evaluation Board (AMP1 to DSA and AMP2)

Table 2. Typical RF Performance[1]

Parameter	Frequency							Unit
	700[3]	900[3]	1900	2140	2650	3500	3700	MHz
Gain	41	38.6	31.3	30.2	28.3	24.4	23.5	dB
S11	-24.1	-18.9	-19.1	-20.6	-16.5	-18.8	-18.6	dB
S22	-8.9	-10.5	-14.7	-18.5	-10.9	-28.2	-23.4	dB
OIP3[2]	45	45	39	40	37	36.5	37	dBm
P1dB	25.7	25.9	25.4	25.1	25.6	24.1	23.9	dBm
WCDMA ACLR[3]	14.7	15.1	14.6	14.2	13.9	13.4	13.1	dBm
LTE 20M ACLR[4]	15.4	16	15.5	15.2	15.4	14.8	14.5	dBm
N.F	2.6	2.6	2.7	2.9	3.0	3.4	3.5	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+5.0V,50 Ω system. measure on Evaluation Board (DSA to AMP)
2. OIP3 measured with two tones at an output of +10 dBm per tone separated by 1 MHz.
3. OIP3 _ tuned for max OIP3.
4. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob, @ACLR –50dBc
5. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage(VCC)	MCM(AMP1+DSA+AMP2)	-0.3		5.5	V
Supply Current	MCM(AMP1+DSA+AMP2)			440	mA
Digital input voltage	DSA	-0.3		3.6	V
Maximum input power	MCM(AMP1+DSA+AMP2)			+12	dBm
Operating Case Temperature	MCM(AMP1+DSA+AMP2)	-40		85	℃
Storage Temperature	MCM(AMP1+DSA+AMP2)	-55		150	℃
Junction Temperature	MCM(AMP1+DSA+AMP2)			220	℃
MTTF	at 150℃, MCM(AMP1+DSA+AMP2)		TBD		Hours

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Bandwidth	MCM(AMP1+DSA+AMP2)	700		4000	MHz
Supply Voltage(VCC)	MCM(AMP1+DSA+AMP2)	4.75	5	5.25	V
Operating Case Temperature	MCM(AMP1+DSA+AMP2)	-40		85	˚C
R_{TH}	MCM(AMP1+DSA+AMP2)		38.5		˚C/W

Programming mode

Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by *Figure 3* (Serial Interface Timing Diagram) and *Table 6* (Serial Interface AC Characteristics).

Power-up Control Settings

The BVA2140 always assumes a specifiable attenuation setting on power-up. This feature exists for Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in LE=1 or P/S = 1, PUP1 and PUP2 are not active. But When the attenuator powers up in P/S = 0 with LE = 0, the control bits are automatically set to one of four possible values.

These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in *Table 5* (Power-Up Truth Table).

Table 5. PUP Truth Table

P/S	LE	PUP2	PUP1	Attenuation state
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5-C16

Note: If Power up with LE = 1 or P/S=1, PUP1 and PUP2 are not active

Figure 3. Serial Interface Timing Diagram

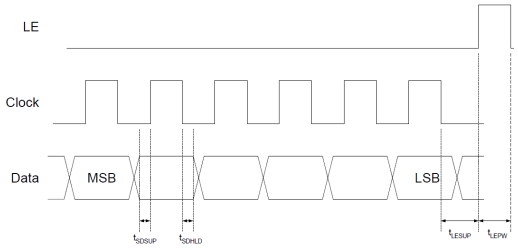


Table 6. Serial Interface AC Characteristics

VDD = 5.0V with DSA only, -40°C < TA < 105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
fClk	Serial data clock frequency		10	MHz
tClkH	Serial clock HIGH time	30		ns
tClkL	Serial clock LOW time	30		ns
tLESUP	LE set-up time after last clock falling edge	10		ns
tLEPW	LE minimum pulse width	30		ns
tSDSUP	Serial data set-up time before clock rising edge	10		ns
tSDHLD	Serial data hold time after clock falling edge	10		ns

Note: fClk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification

Table 7. 6-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B3	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) — LSB (Last in)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Figure 4. Pin Configuration(Top View)

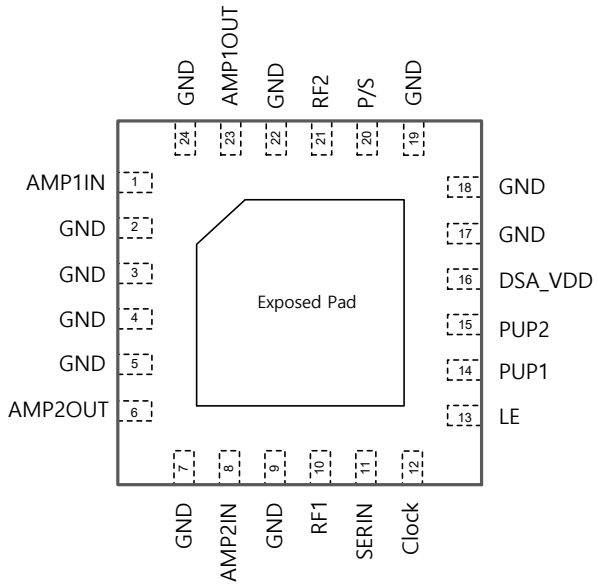


Table 8. Pin Description

Pin	Pin name	Description
2,3,4,5,7,9,17, 18,19,22,24	GND	Ground
1	AMP1IN	RF Amp1 in Port
6	AMP2OUT	RF Amp2 out Port
8	AMP2IN	RF Amp in Port
10	RF1[1]	RF port(DSA output)
11	DATA	Serial interface data input
12	Clock	Serial interface clock input
13	LE[2]	Latch Enable input
14	PUP1[3]	Power-up selection bit 1
15	PUP2	Power-up selection bit 2
16	VDD	DSA Supply voltage (nominal 5.0V)
20	P/S	Parallel/Serial mode select
21	RF2[1]	RF port(DSA input)
23	AMP1OUT	RF Amp1 out Port

Note: 1. RF pins 10 and 21 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met
2. This pin has an internal 2 MΩ resistor to internal positive digital supply
3. This pin has an internal 200 kΩ resistor to GND

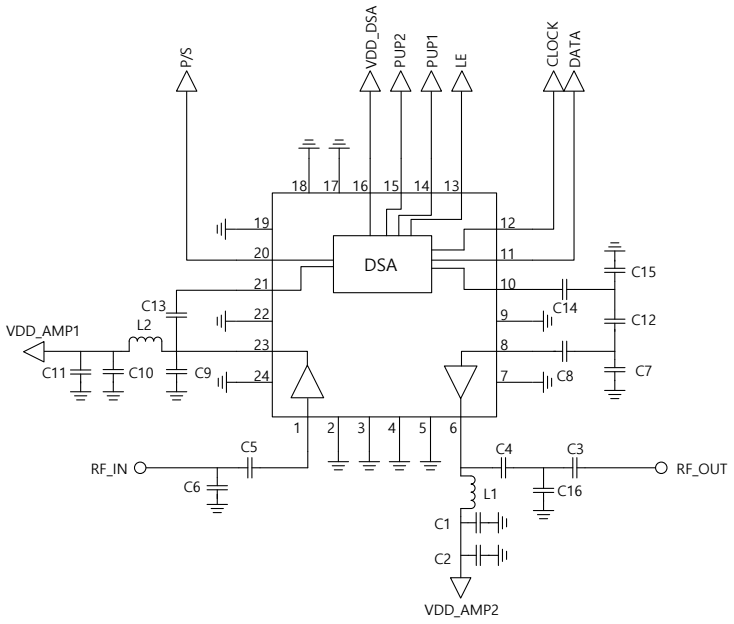
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(700MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

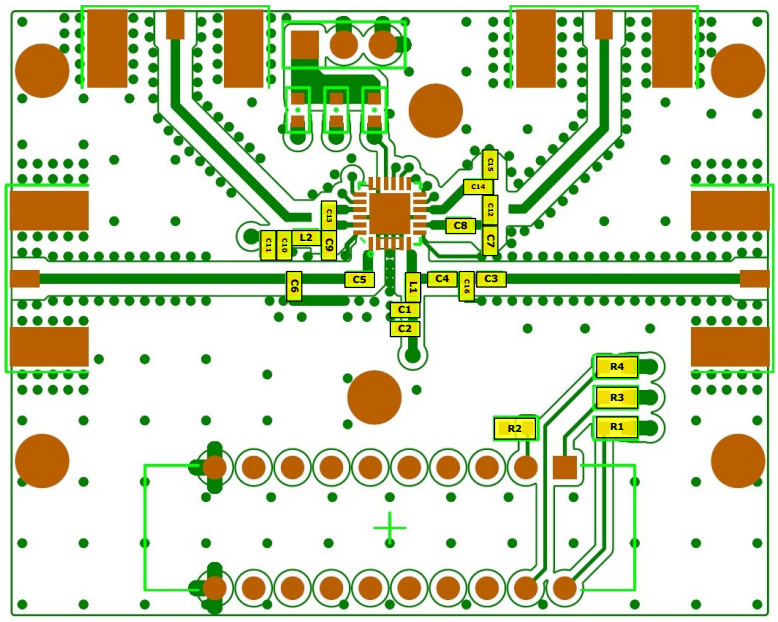
Table 9. Application Circuit : 700MHz

Schematic Diagram



BOM(700MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	22nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	22pF	
C14	0402	0ohm	
C15	0402	NC	
C12	0402	10pF	
C7	0402	9pF	
C8	0402	3.0nH	
L1	0402	33nH	
C1	0402	100pF	
C2	0402	1uF	
C4	0402	4.3nH	
C3	0402	9.0pF	
C16	0402	1.2pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(700MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Table 10. Typical Performance : 700MHz

parameter	Typical Values	Units
Frequency	**700**	**MHz**
Gain	41	dB
S11	-24.1	dB
S22	-8.9	dB
S12	-52.2	dB
OIP3[1]	45	dBm
P1dB	25.7	dBm
Noise Figure	2.6	dB
LTE20MHz ACLR[2]	15.4	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 5. Gain vs Frequency @Max Gain state

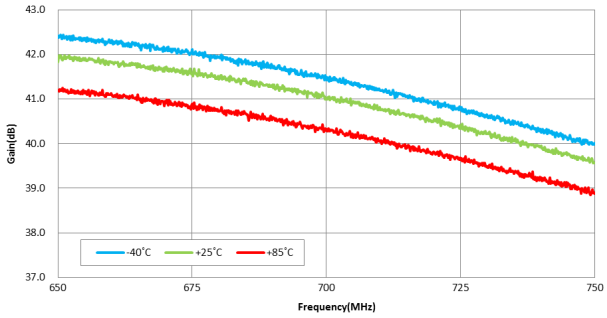


Figure 6. Input Return Loss vs Frequency @Max Gain & Min Gain state

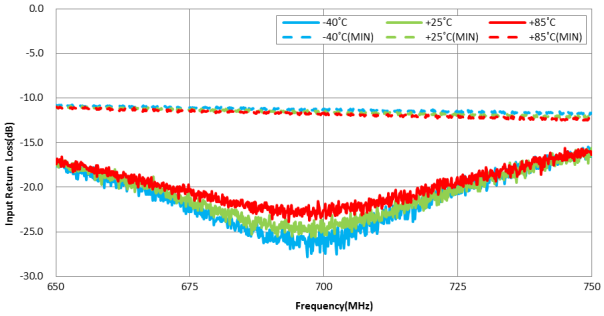


Figure 7. Output Return Loss vs Frequency @Max Gain & Min Gain state

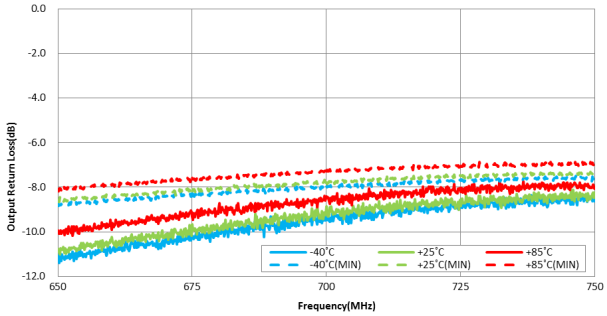


Figure 8. Attenuation Error vs Attenuation Setting @700MHz

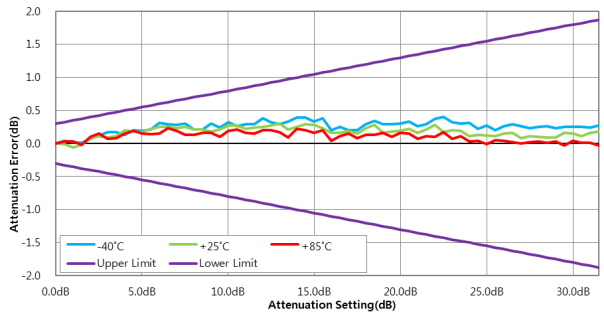
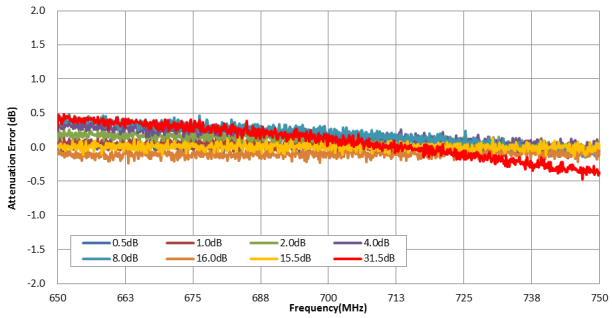


Figure 9. Attenuation Error vs Frequency @Major Attenuation Steps



Note: Upper Limit & Lower Limit is the value converted to a graph 0.3dB+0.5%

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(700MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 10. 0.5dB Step Attenuation vs Attenuation Setting @700MHz

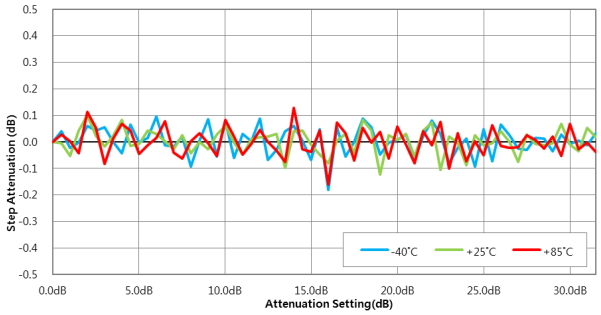


Figure 11. Noise Figure vs Frequency

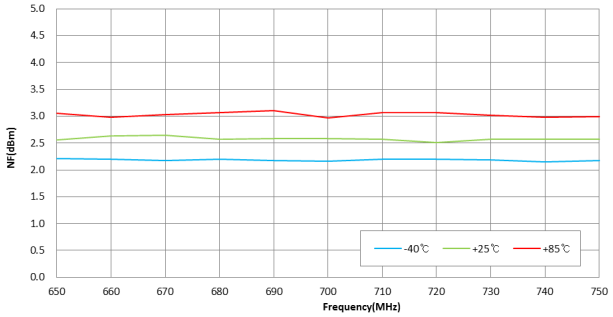


Figure 12. OIP3 vs Output Power @700MHz

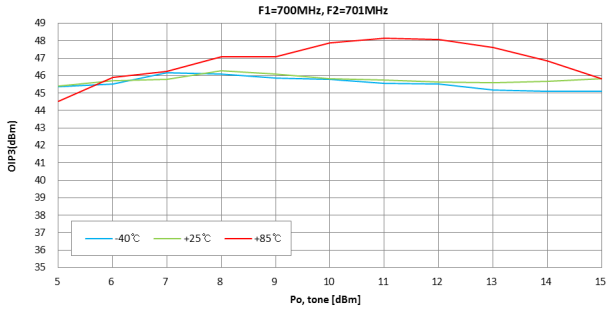


Figure 13. Device performance Pin-Pout-Gain @700MHz

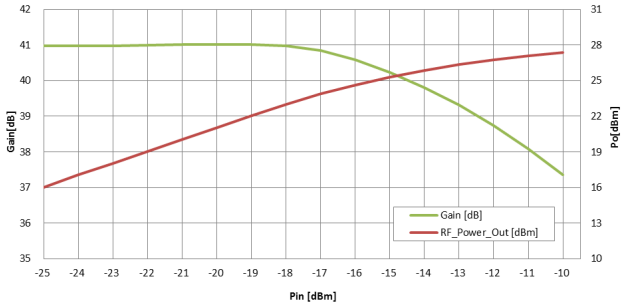
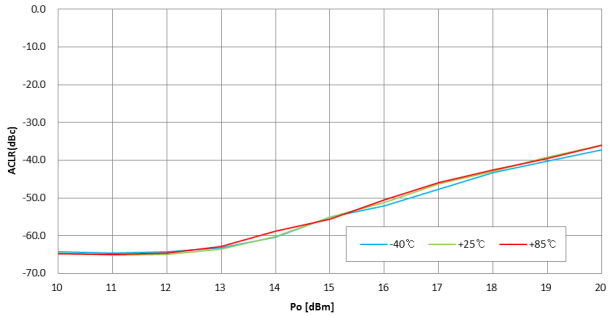


Figure 14. 3GPP WCDMA ACLR vs Output Power
@700MHz, WCDMA 1FA, TM1+64DPCH ±5MHz offset

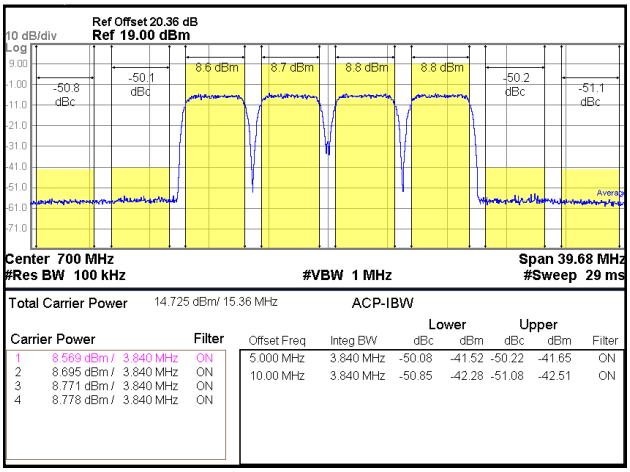


0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(700MHz Application Circuit)

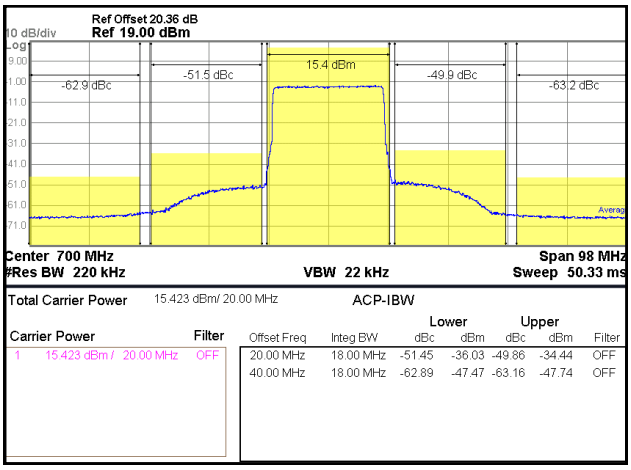
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 15. ACLR @700MHz, WCDMA4FA[1], -50dBc



1. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob

Figure 16. ACLR @700MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob.

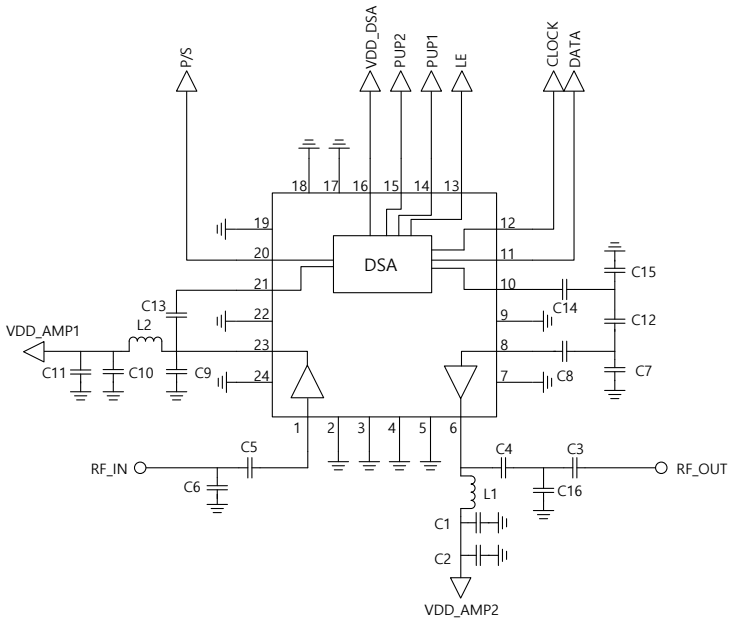
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(900MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

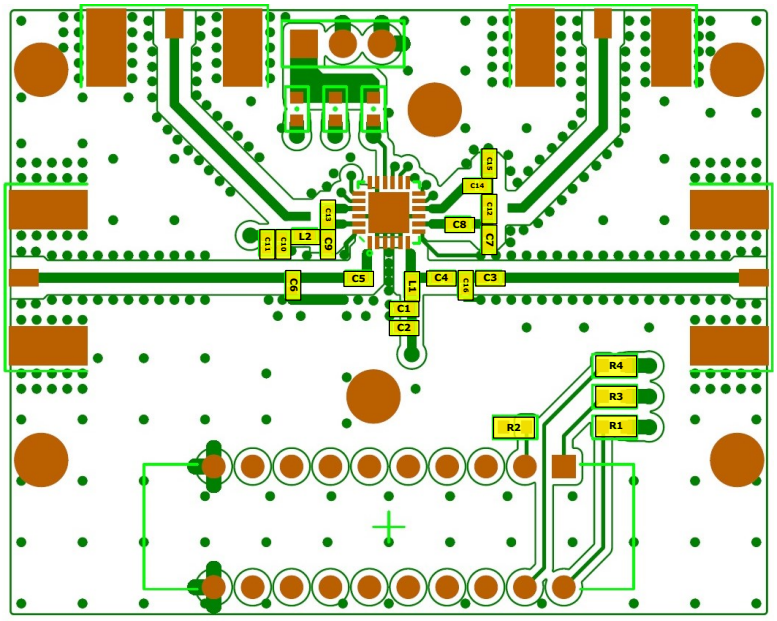
Table 11. Application Circuit : 900MHz

Schematic Diagram



BOM(900MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	22nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	10pF	
C14	0402	0ohm	
C15	0402	NC	
C12	0402	20pF	
C7	0402	7.5pF	
C8	0402	1.0nH	
L1	0402	27nH	
C1	0402	100pF	
C2	0402	1uF	
C4	0402	2.0nH	
C3	0402	100pF	
C16	0402	1.8pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(900MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Table 12. Typical Performance : 900MHz

parameter	Typical Values	Units
Frequency	**900**	**MHz**
Gain	38.6	dB
S11	-18.9	dB
S22	-10.5	dB
S12	-52.0	dB
OIP3[1]	45	dBm
P1dB	25.9	dBm
Noise Figure	2.6	dB
LTE20MHz ACLR[2]	16	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 17. Gain vs Frequency @Max Gain state

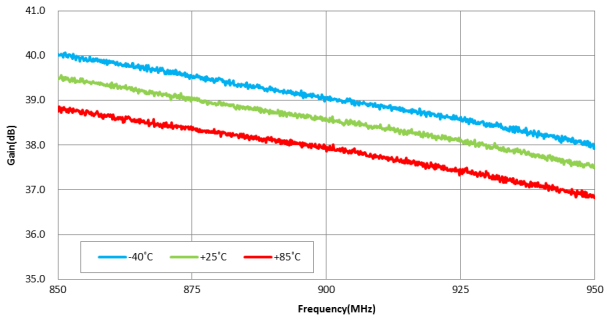


Figure 18. Input Return Loss vs Frequency @Max Gain & Min Gain state

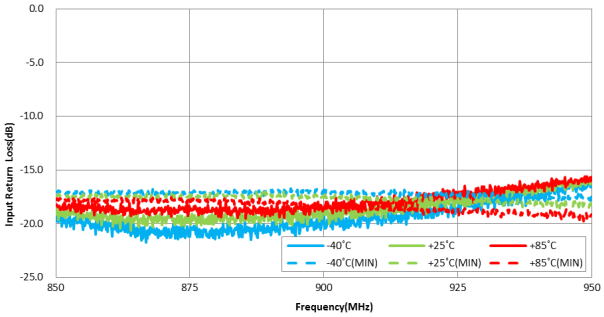


Figure 19. Output Return Loss vs Frequency @Max Gain & Min Gain state

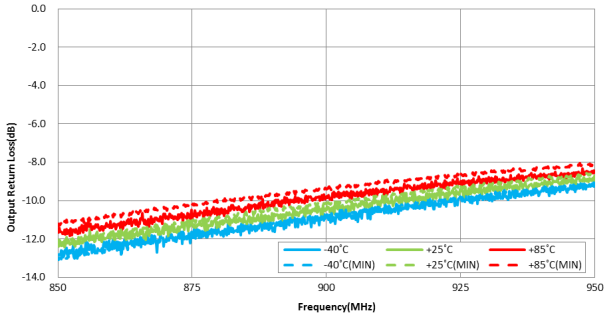


Figure 20. Attenuation Error vs Attenuation Setting @900MHz

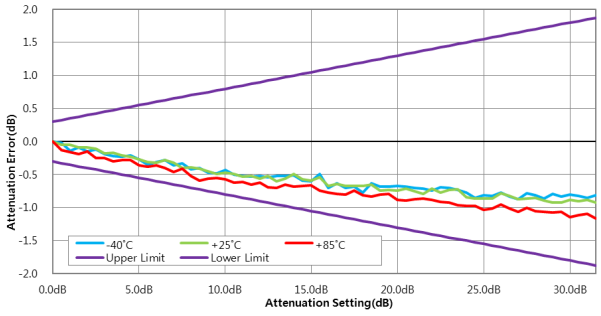
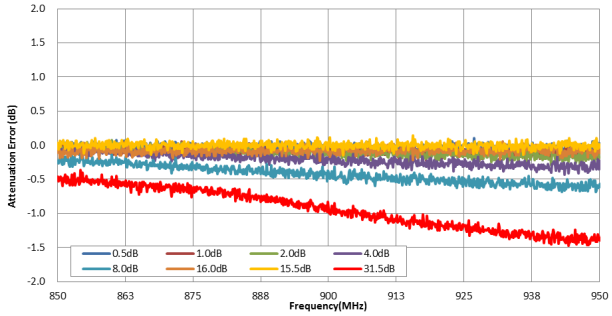


Figure 21. Attenuation Error vs Frequency @Major Attenuation Steps



Note: Upper Limit & Lower Limit is the value converted to a graph 0.3dB+0.5%

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(900MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 22. 0.5dB Step Attenuation vs Attenuation Setting @900MHz

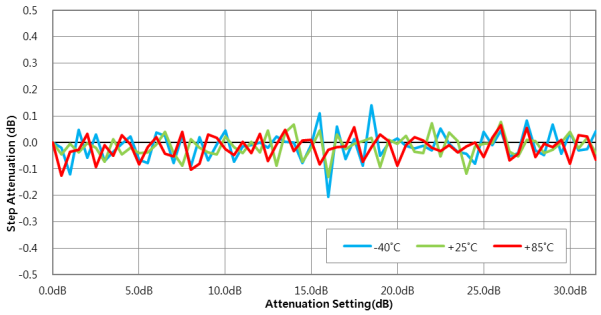


Figure 23. Noise Figure vs Frequency

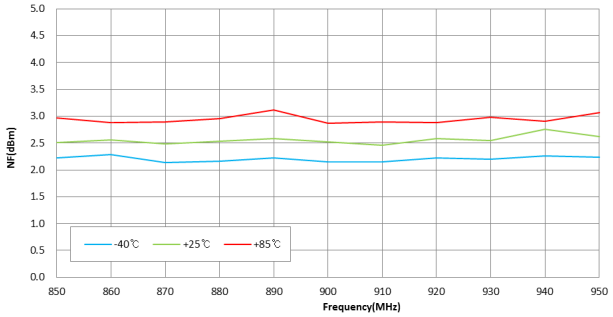


Figure 24. OIP3 vs Output Power @900MHz

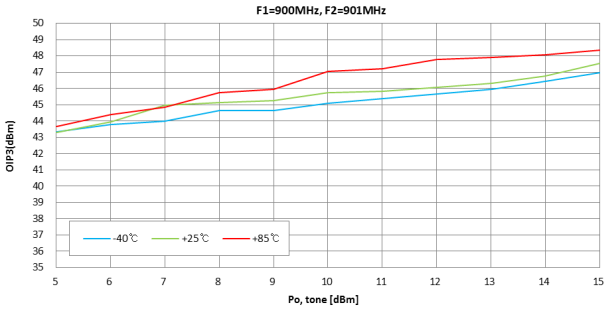


Figure 25. Device performance Pin-Pout-Gain @900MHz

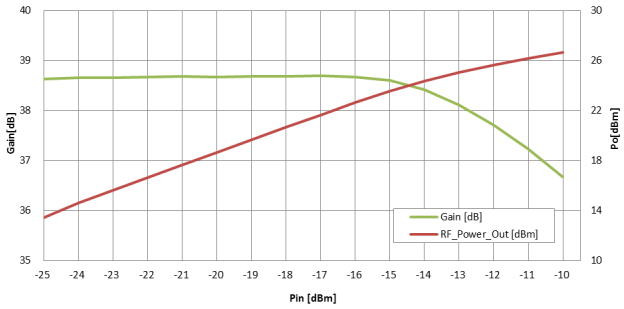
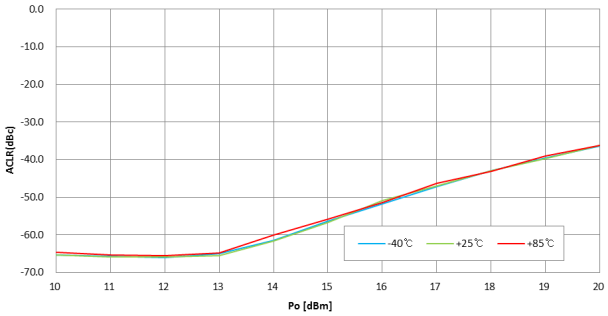


Figure 26. 3GPP WCDMA ACLR vs Output Power
@900MHz, WCDMA 1FA, TM1+64DPCH ±5MHz offset

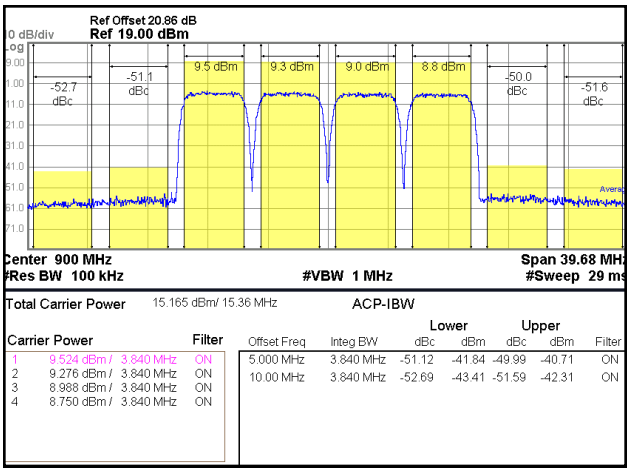


0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(900MHz Application Circuit)

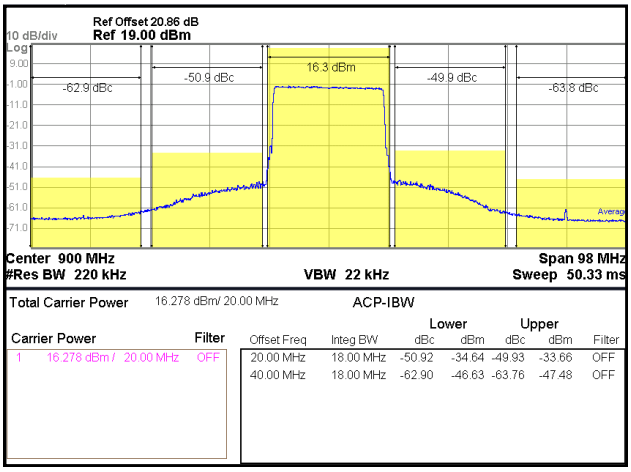
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 27. ACLR @900MHz, WCDMA4FA[1], -50dBc



1. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob

Figure 28. ACLR @900MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob.

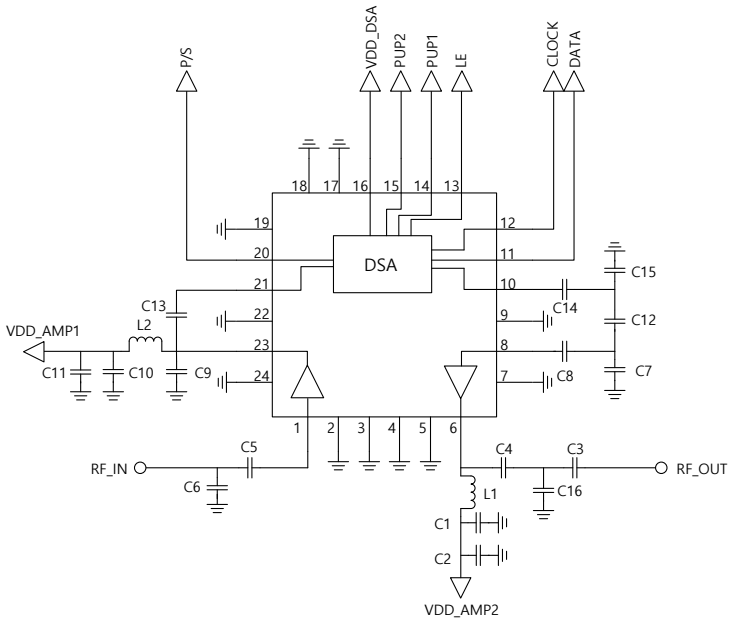
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(1900MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

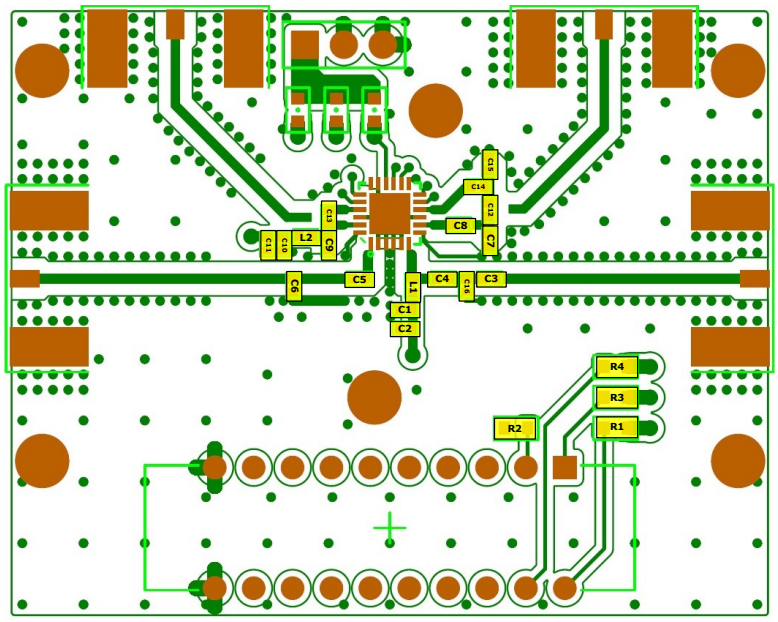
Table 13. Application Circuit : 1900MHz

Schematic Diagram



BOM(1900MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	22nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	22pF	
C14	0402	0ohm	
C15	0402	NC	
C12	0402	1.2pF	
C7	0402	1.3pF	
C8	0402	1.0nH	
L1	0402	15nH	
C1	0402	62pF	
C2	0402	1uF	
C4	0402	1.5nH	
C3	0402	22pF	
C16	0402	1.0pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(1900MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Table 14. Typical Performance : 1900MHz

parameter	Typical Values	Units
Frequency	**1900**	**MHz**
Gain	31.3	dB
S11	-19.1	dB
S22	-14.7	dB
S12	-48.8	dB
OIP3[1]	39	dBm
P1dB	25.4	dBm
Noise Figure	2.7	dB
LTE20MHz ACLR[2]	15.5	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 29. Gain vs Frequency @Max Gain state

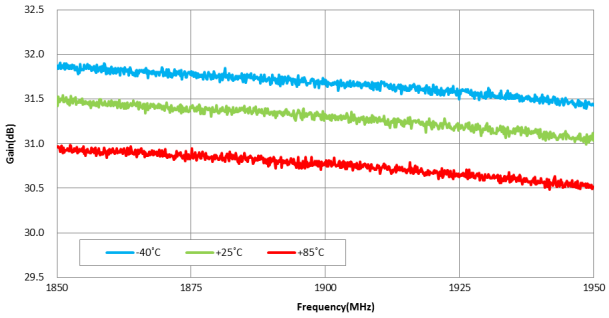


Figure 30. Input Return Loss vs Frequency @Max Gain & Min Gain state

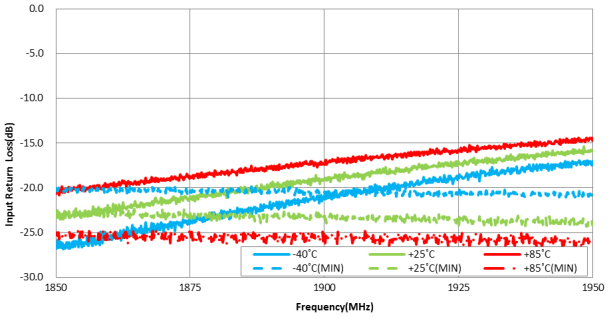


Figure 31. Output Return Loss vs Frequency @Max Gain & Min Gain state

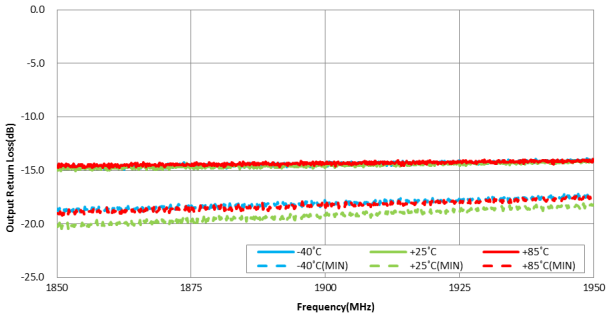


Figure 32. Attenuation Error vs Attenuation Setting @1900MHz

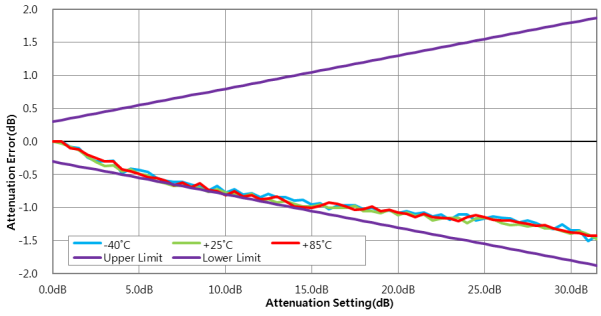
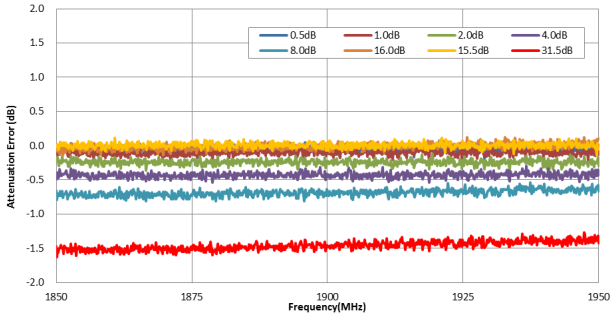


Figure 33. Attenuation Error vs Frequency @Major Attenuation Steps



Note: Upper Limit & Lower Limit is the value converted to a graph 0.3dB+0.5%

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(1900MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 34. 0.5dB Step Attenuation vs Attenuation Setting @1900MHz

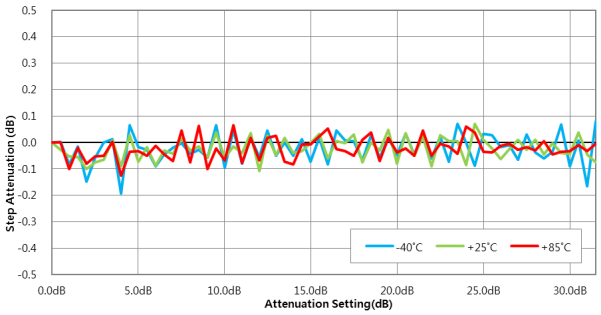


Figure 35. Noise Figure vs Frequency

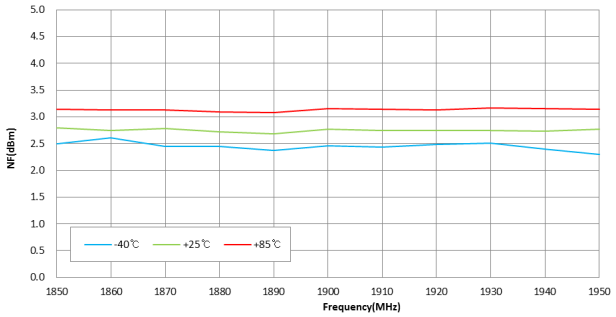


Figure 36. OIP3 vs Output Power @1900MHz

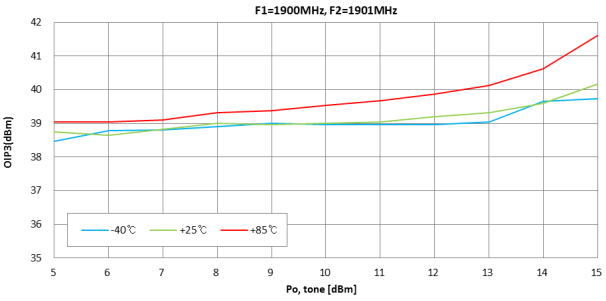


Figure 37. Device performance Pin-Pout-Gain @1900MHz

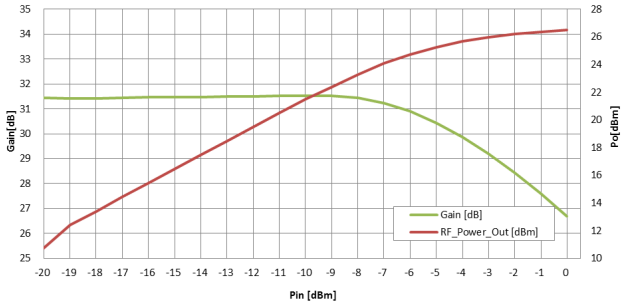
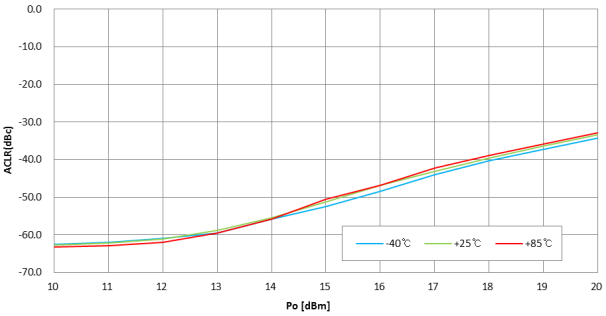


Figure 38. 3GPP WCDMA ACLR vs Output Power
@1900MHz, WCDMA 1FA , TM1+64DPCH ±5MHz offset

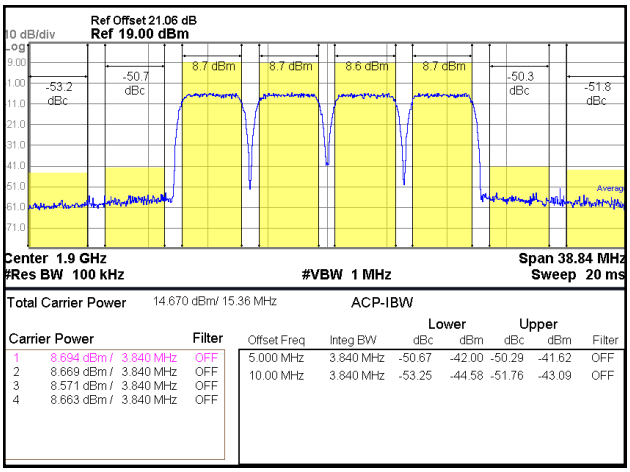


0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(1900MHz Application Circuit)

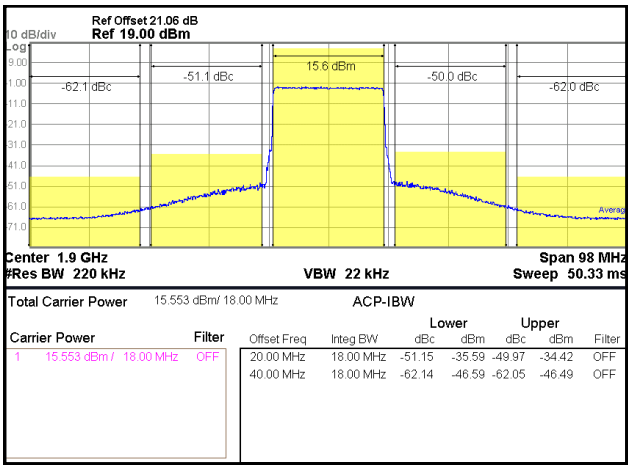
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 39. ACLR @1900MHz, WCDMA4FA[1], -50dBc



1. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob

Figure 40. ACLR @1900MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob.

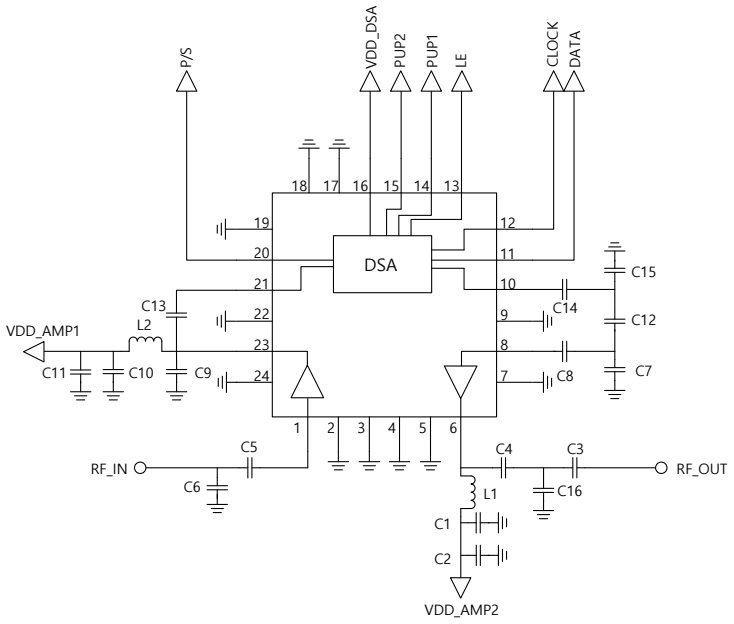
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(2140MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

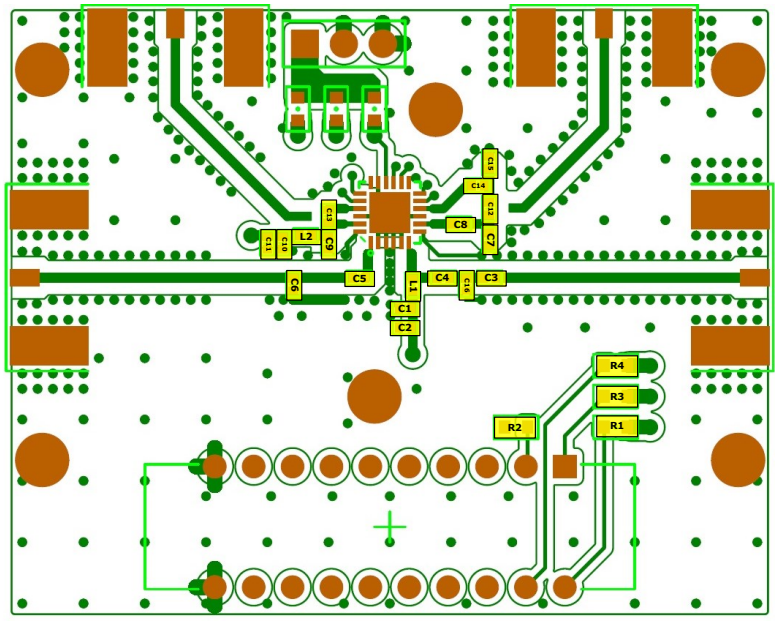
Table 15. Application Circuit : 2140MHz

Schematic Diagram



BOM(2140MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	22nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	22pF	
C14	0402	0ohm	
C15	0402	NC	
C12	0402	0.75pF	
C7	0402	0.5pF	
C8	0402	1.0nH	
L1	0402	5.1nH	
C1	0402	62pF	
C2	0402	1uF	
C4	0402	0ohm	
C3	0402	22pF	
C16	0402	0.5pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(2140MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Table 16. Typical Performance : 2140MHz

parameter	Typical Values	Units
Frequency	**2140**	**MHz**
Gain	30.2	dB
S11	-20.6	dB
S22	-18.5	dB
S12	-49.5	dB
OIP3[1]	40	dBm
P1dB	25.1	dBm
Noise Figure	2.9	dB
LTE20MHz ACLR[2]	15.2	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 41. Gain vs Frequency @Max Gain state

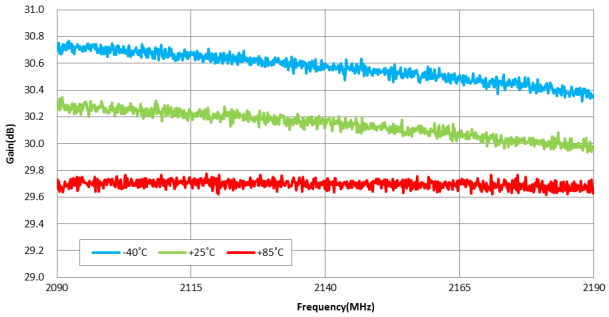


Figure 42. Input Return Loss vs Frequency @Max Gain & Min Gain state

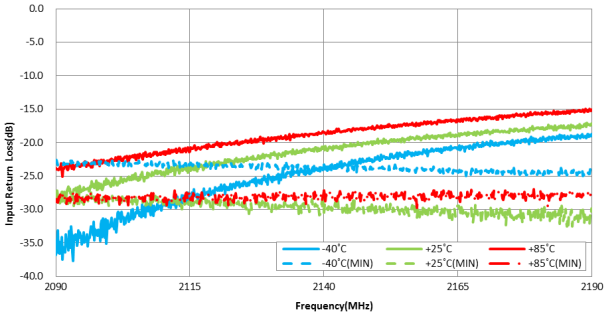


Figure 43. Output Return Loss vs Frequency @Max Gain & Min Gain state

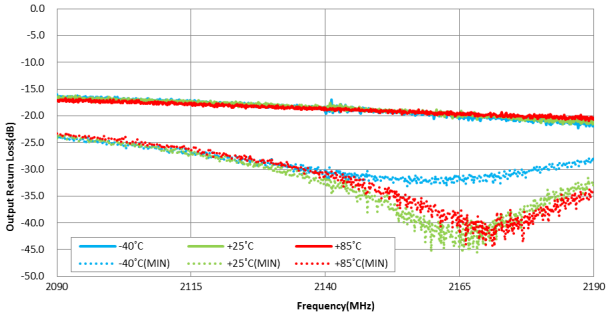


Figure 44. Attenuation Error vs Attenuation Setting @2140MHz

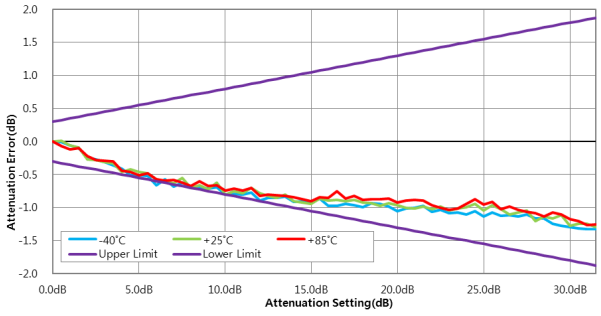
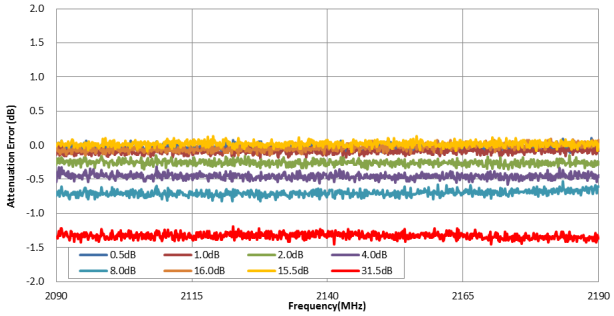


Figure 45. Attenuation Error vs Frequency @Major Attenuation Steps



Note: Upper Limit & Lower Limit is the value converted to a graph 0.3dB+0.5%

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(2140MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 46. 0.5dB Step Attenuation vs Attenuation Setting @2140MHz

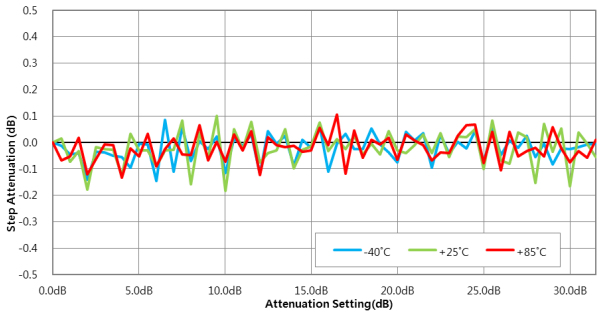


Figure 47. Noise Figure vs Frequency

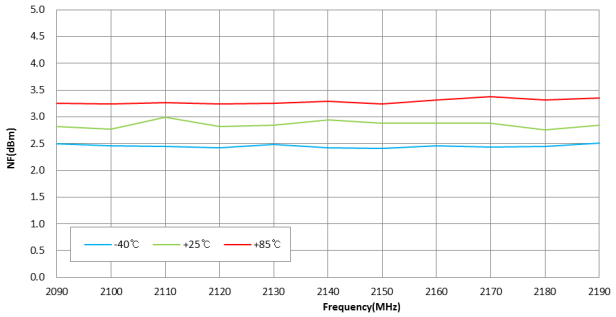


Figure 48. OIP3 vs Output Power @2140MHz

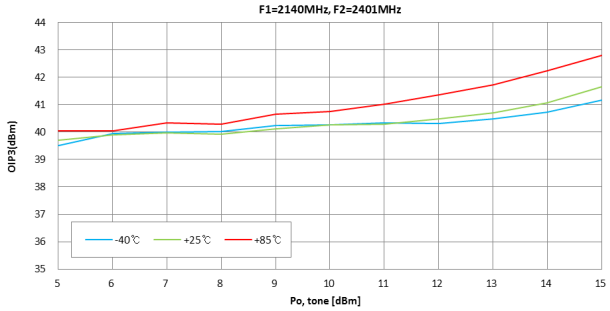


Figure 49. Device performance Pin-Pout-Gain @2140MHz

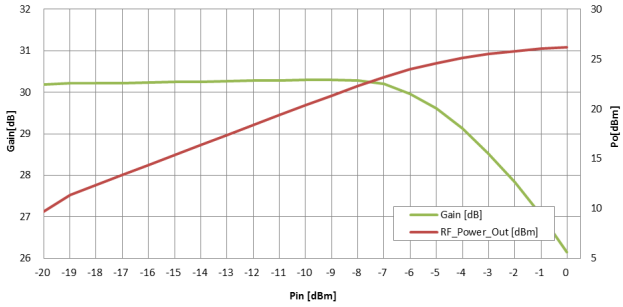
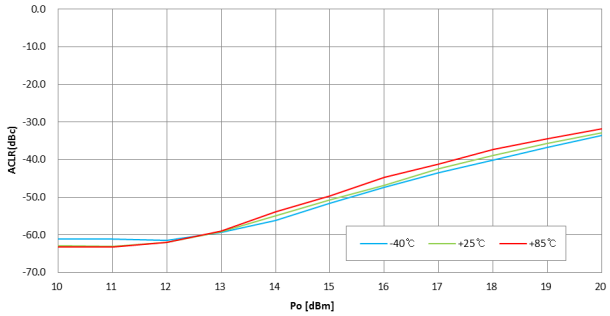


Figure 50. 3GPP WCDMA ACLR vs Output Power
@2140MHz, WCDMA 1FA, TM1+64DPCH ±5MHz offset

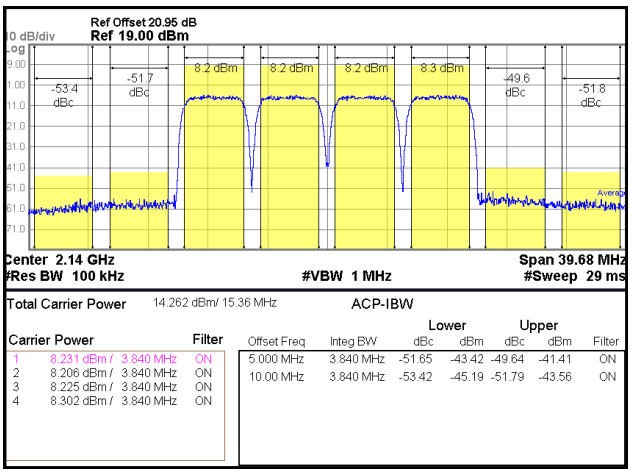


0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(2140MHz Application Circuit)

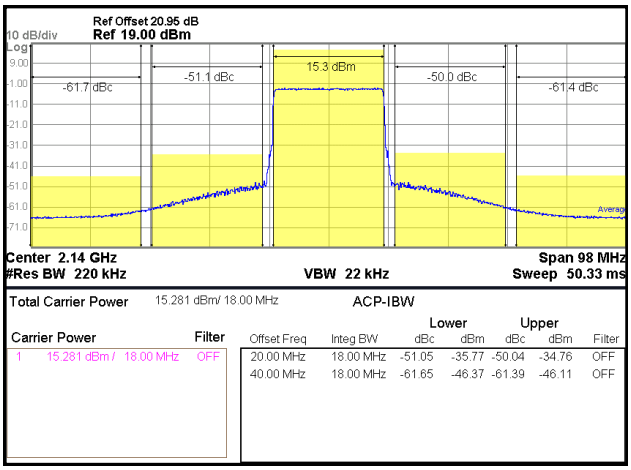
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 51. ACLR @2140MHz, WCDMA4FA[1], -50dBc



1. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob

Figure 52. ACLR @2140MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob.

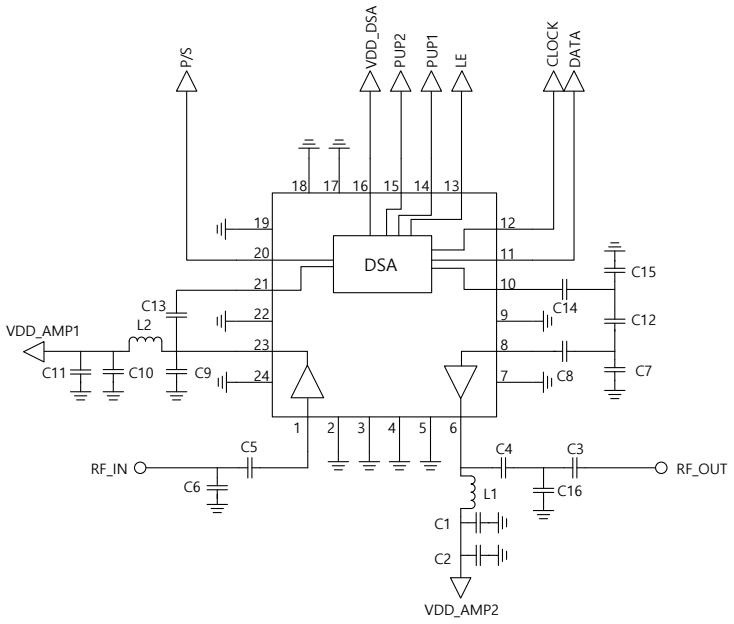
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(2650MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

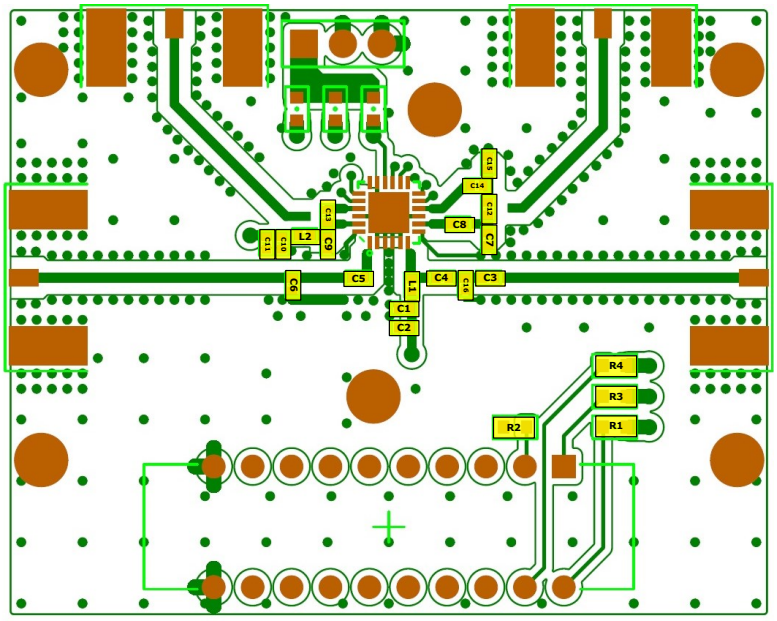
Table 17. Application Circuit : 2650MHz

Schematic Diagram



BOM(2650MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	22nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	22pF	
C14	0402	0ohm	
C15	0402	NC	
C12	0402	0.75pF	
C7	0402	0.75pF	
C8	0402	0ohm	
L1	0402	4.3nH	
C1	0402	22pF	
C2	0402	1uF	
C4	0402	0ohm	
C3	0402	22pF	
C16	0402	1.0pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

Typical RF Performance Plot - BVA2140 EVK - PCB(2650MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Table 53. Typical Performance : 2650MHz

parameter	Typical Values	Units
Frequency	**2650**	**MHz**
Gain	28.3	dB
S11	-16.5	dB
S22	-10.9	dB
S12	-47.3	dB
OIP3[1]	37	dBm
P1dB	25.6	dBm
Noise Figure	3.0	dB
LTE20MHz ACLR[2]	15.4	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 54. Gain vs Frequency @Max Gain state

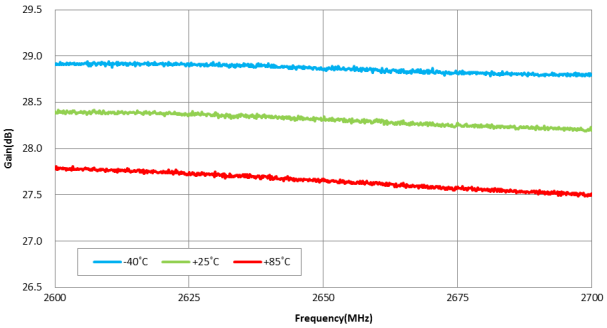


Figure 55. Input Return Loss vs Frequency @Max Gain & Min Gain state

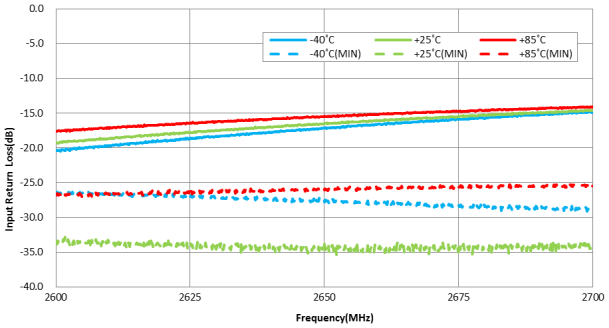


Figure 56. Output Return Loss vs Frequency @Max Gain & Min Gain state

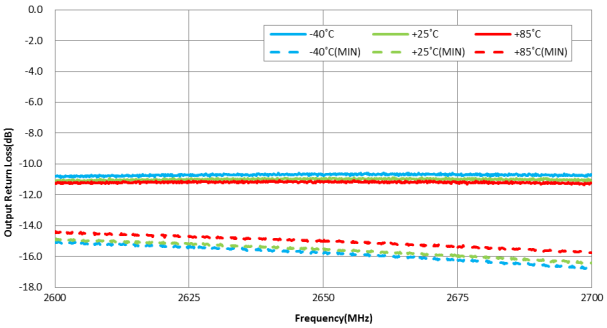


Figure 57. Attenuation Error vs Attenuation Setting @2650MHz

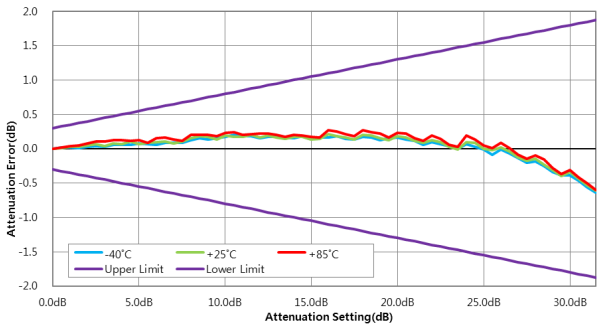
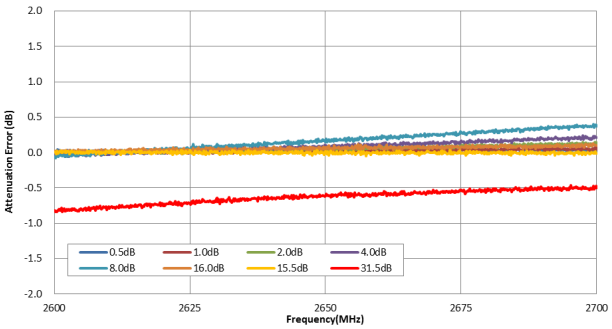


Figure 58. Attenuation Error vs Frequency @Major Attenuation Steps



Note: Upper Limit & Lower Limit is the value converted to a graph 0.3dB+0.5%

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(2650MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 59. 0.5dB Step Attenuation vs Attenuation Setting @2650MHz

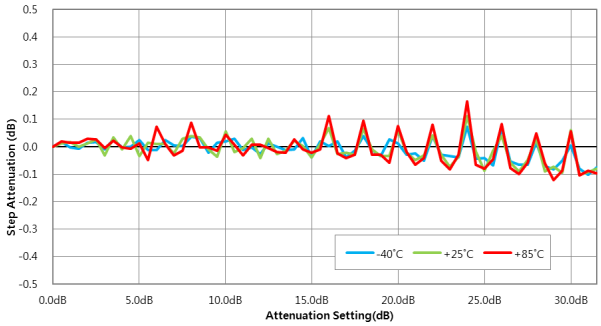


Figure 60. Noise Figure vs Frequency

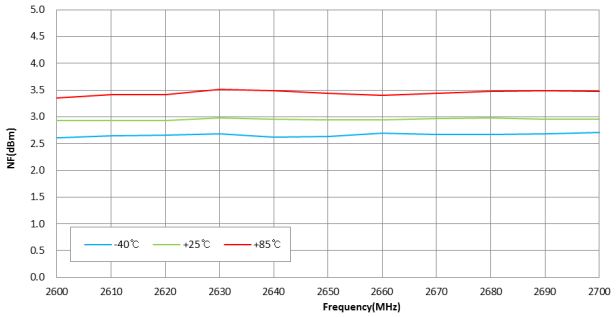


Figure 61. OIP3 vs Output Power @2650MHz

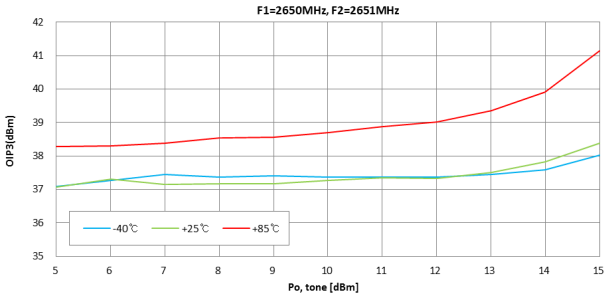


Figure 62. Device performance Pin-Pout-Gain @2650MHz

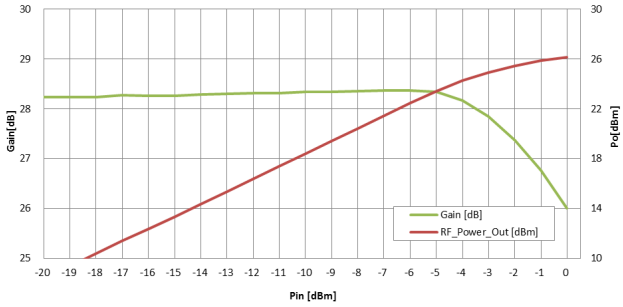
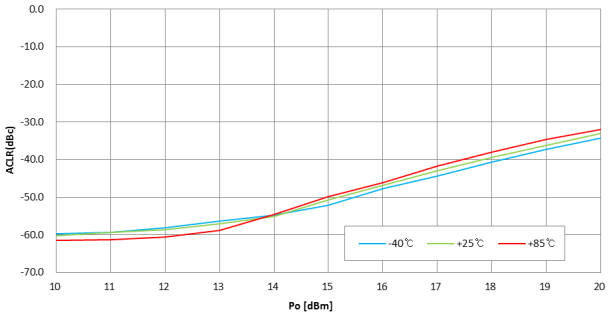


Figure 63. 3GPP WCDMA ACLR vs Output Power
@2650MHz, WCDMA 1FA , TM1+64DPCH ±5MHz offset

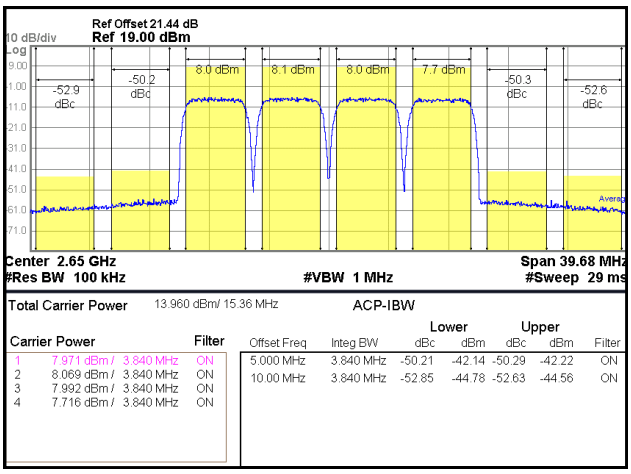


0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(2650MHz Application Circuit)

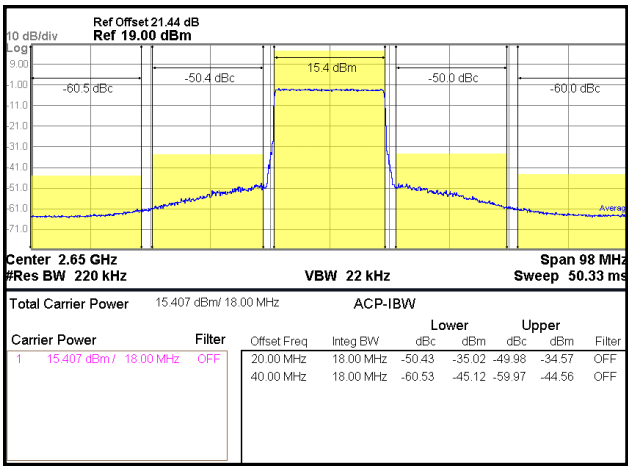
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 64. ACLR @2650MHz, WCDMA4FA[1], -50dBc



1. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob

Figure 65. ACLR @2650MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob.

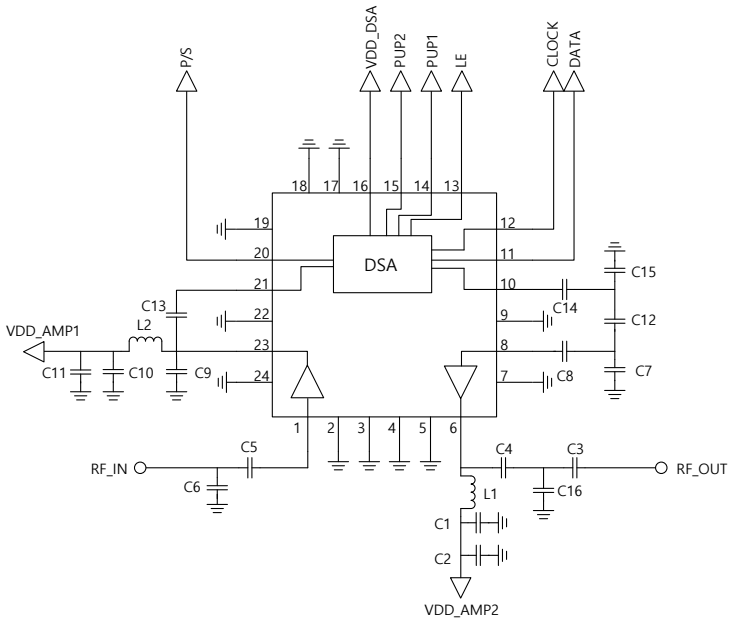
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(3500MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

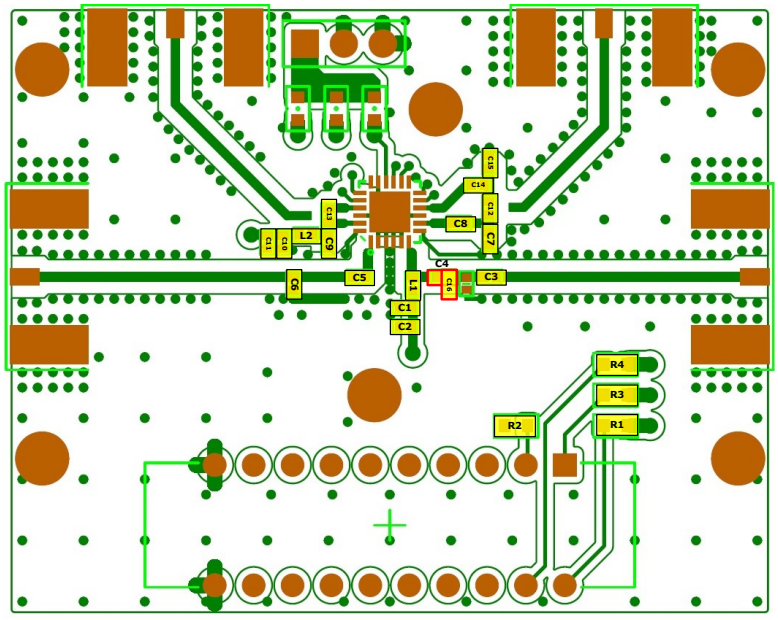
Table 19. Application Circuit : 3500MHz

Schematic Diagram



BOM(3500MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	15nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	22pF	
C14	0402	0ohm	
C15	0402	NC	
C12	0402	0ohm	
C7	0402	1pF	
C8	0402	2pF	
L1	0402	10nH	
C1	0402	22pF	
C2	0402	1uF	
C4	0402	Copper	
C3	0402	22pF	
C16	0402	0.75pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)
2. C4 place piece of trace to cover the gap
3. C16 moves to the left 19.7mil(0.5mm) (refer to the left figure)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(3500MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Table 20. Typical Performance : 3500MHz

parameter	Typical Values	Units
Frequency	**3500**	**MHz**
Gain	24.4	dB
S11	-18.8	dB
S22	-28.2	dB
S12	-37.9	dB
OIP3[1]	36.5	dBm
P1dB	24.1	dBm
Noise Figure	3.4	dB
LTE20MHz ACLR[2]	14.8	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 66. Gain vs Frequency @Max Gain state

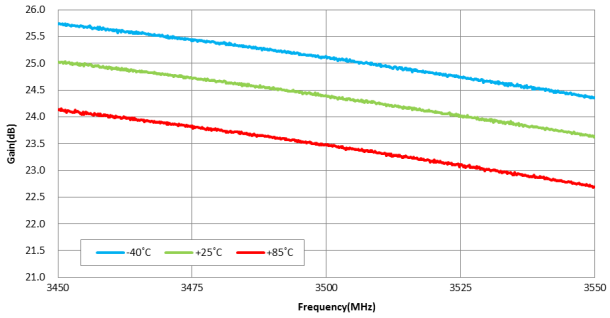


Figure 67. Input Return Loss vs Frequency @Max Gain & Min Gain state

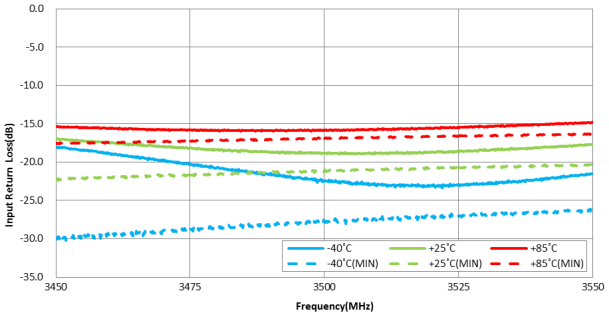


Figure 68. Output Return Loss vs Frequency @Max Gain & Min Gain state

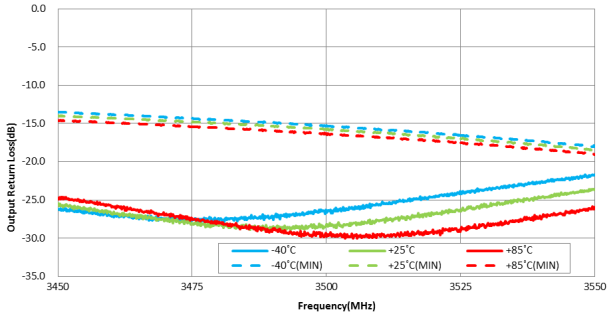


Figure 69. Attenuation Error vs Attenuation Setting @3500MHz

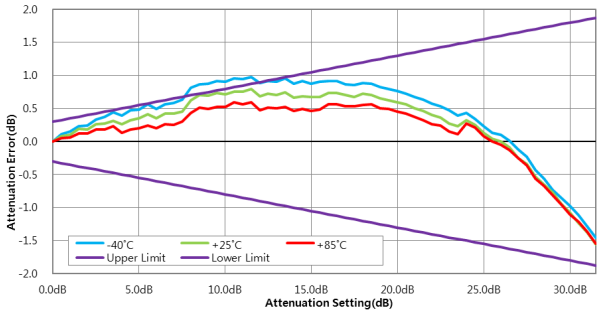
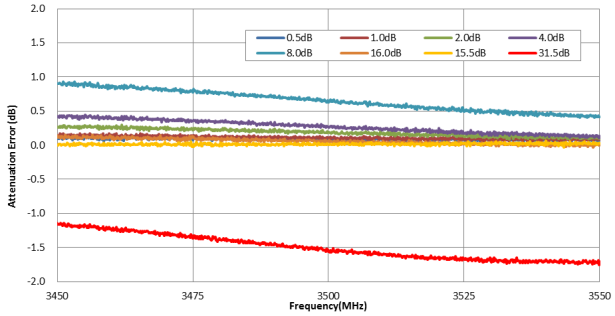


Figure 70. Attenuation Error vs Frequency @Major Attenuation Steps



Note: Upper Limit & Lower Limit is the value converted to a graph 0.3dB+0.5%

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(3500MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 71. 0.5dB Step Attenuation vs Attenuation Setting @3500MHz

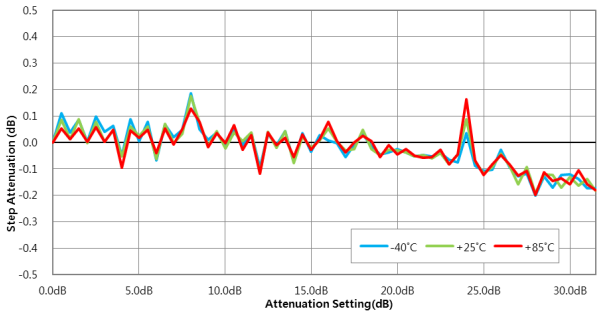


Figure 72. Noise Figure vs Frequency

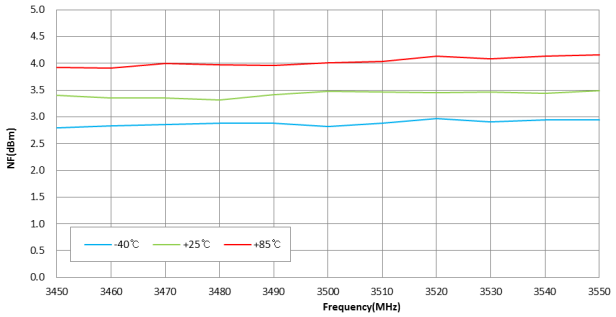


Figure 73. OIP3 vs Output Power @3500MHz

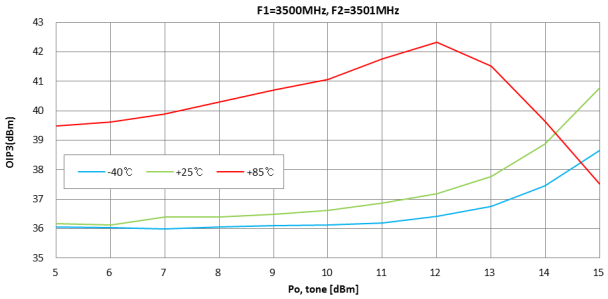


Figure 74. Device performance Pin-Pout-Gain @3500MHz

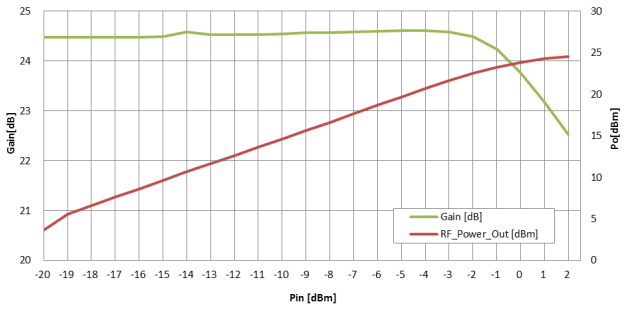
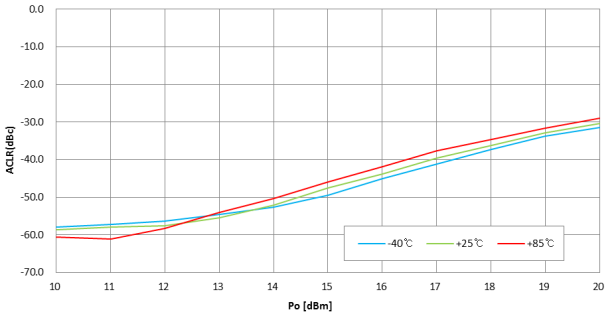


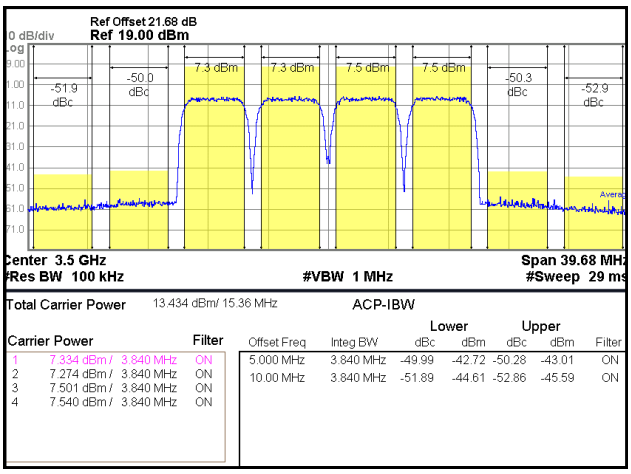
Figure 75. 3GPP WCDMA ACLR vs Output Power
@3500MHz, WCDMA 1FA , TM1+64DPCH ±5MHz offset



Typical RF Performance Plot - BVA2140 EVK - PCB(3500MHz Application Circuit)

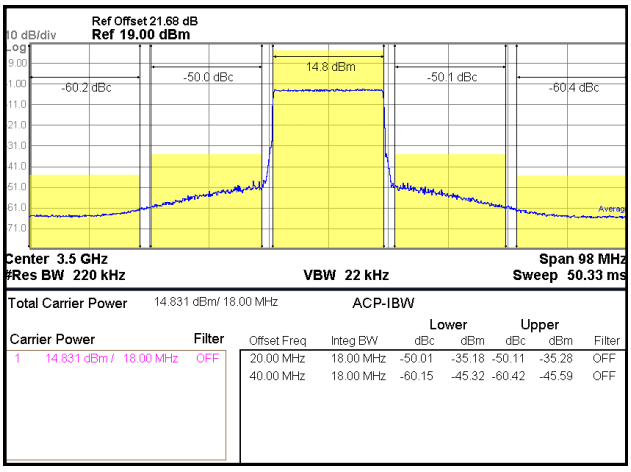
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 76. ACLR @3500MHz, WCDMA4FA[1], -50dBc



1. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob

Figure 77. ACLR @3500MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob.

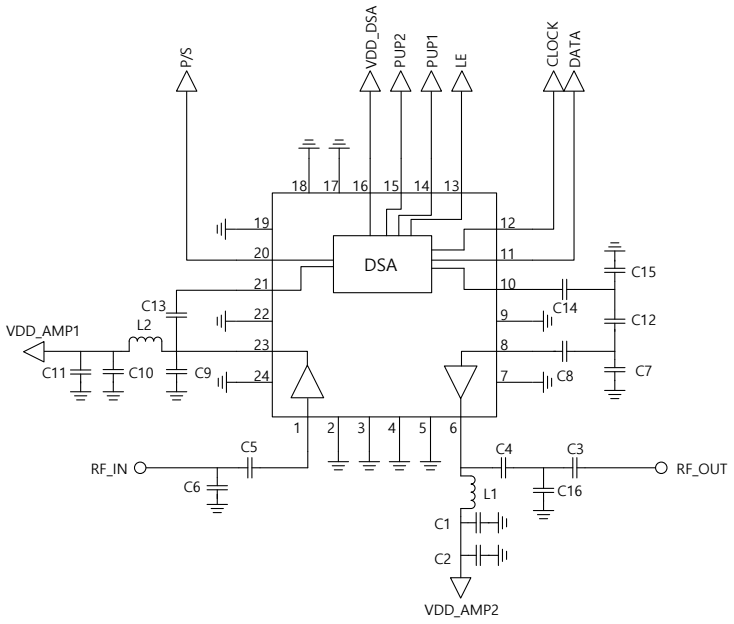
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(3700MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

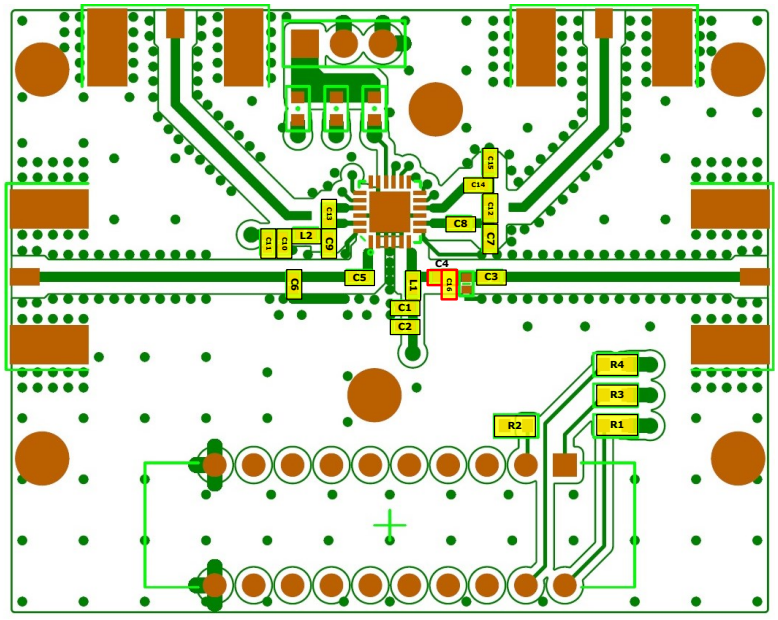
Table 21. Application Circuit : 3700MHz

Schematic Diagram



BOM(3700MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	15nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	22pF	
C14	0402	0ohm	
C15	0402	NC	
C12	0402	0ohm	
C7	0402	0.75pF	
C8	0402	1.8pF	
L1	0402	10nH	
C1	0402	22pF	
C2	0402	1uF	
C4	0402	Copper	
C3	0402	22pF	
C16	0402	0.75pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)
2. C4 place piece of trace to cover the gap
3. C16 moves to the left 19.7mil(0.5mm) (refer to the left figure)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(3700MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Table 22. Typical Performance : 3700MHz

parameter	Typical Values	Units
Frequency	**3700**	**MHz**
Gain	23.5	dB
S11	-18.6	dB
S22	-23.4	dB
S12	-37.1	dB
OIP3[1]	37	dBm
P1dB	23.9	dBm
Noise Figure	3.5	dB
LTE20MHz ACLR[2]	14.5	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 78. Gain vs Frequency @Max Gain state

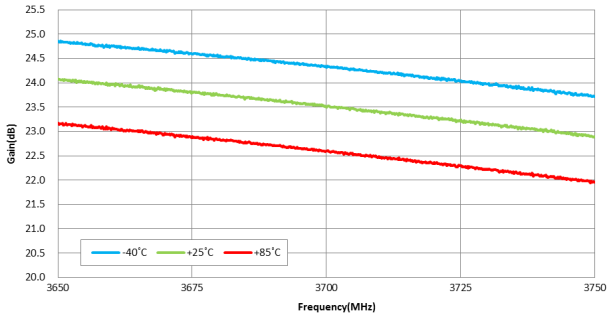


Figure 79. Input Return Loss vs Frequency @Max Gain & Min Gain state

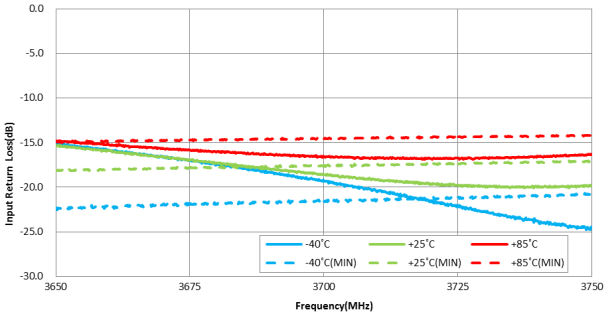


Figure 80. Output Return Loss vs Frequency @Max Gain & Min Gain state

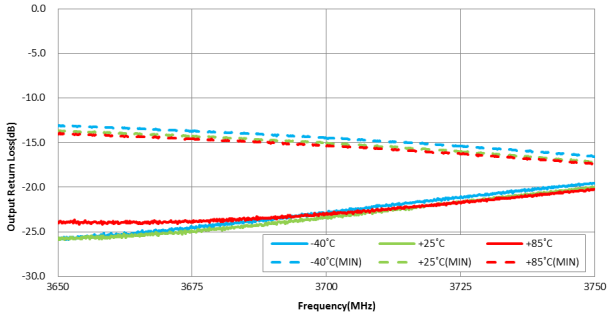


Figure 81. Attenuation Error vs Attenuation Setting @3700MHz

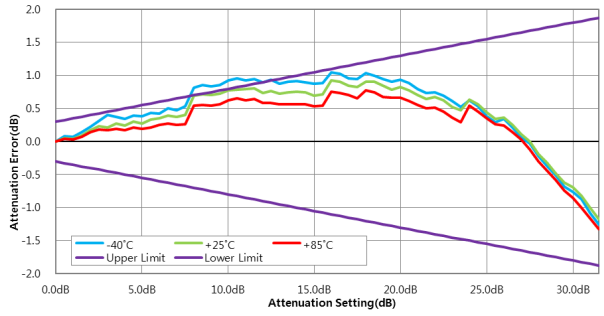
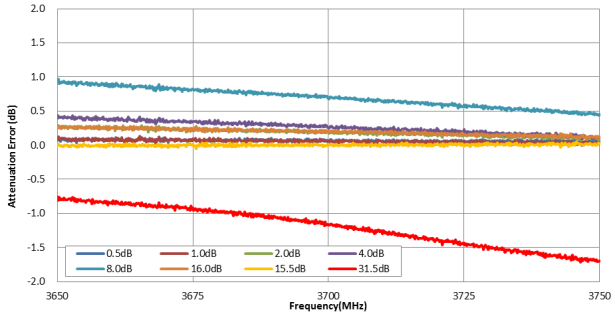


Figure 82. Attenuation Error vs Frequency @Major Attenuation Steps



Note: Upper Limit & Lower Limit is the value converted to a graph 0.3dB+0.5%

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(3700MHz Application Circuit)

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 83. 0.5dB Step Attenuation vs Attenuation Setting @3700MHz

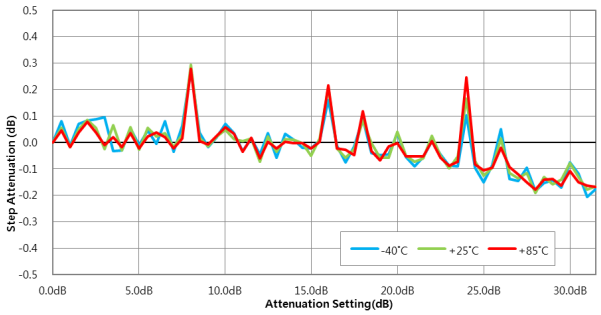


Figure 84. Noise Figure vs Frequency

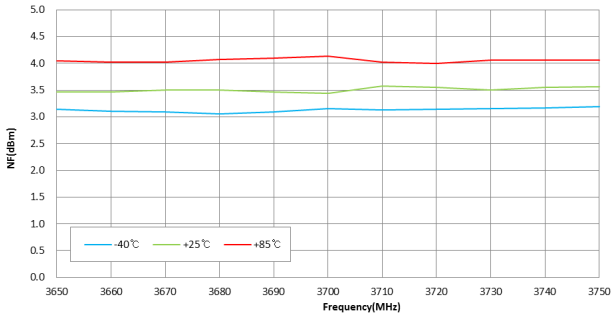


Figure 85. OIP3 vs Output Power @3700MHz

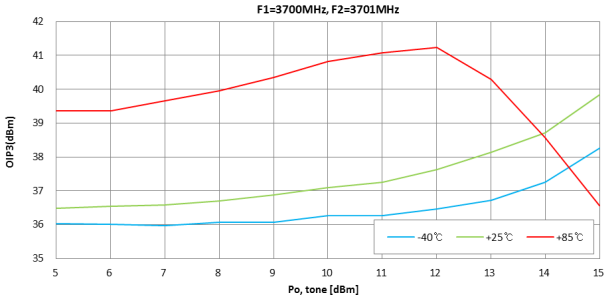


Figure 86. Device performance Pin-Pout-Gain @3700MHz

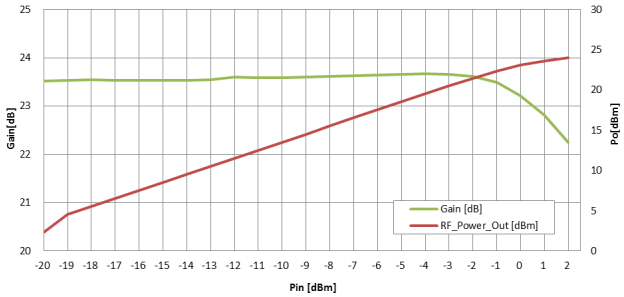
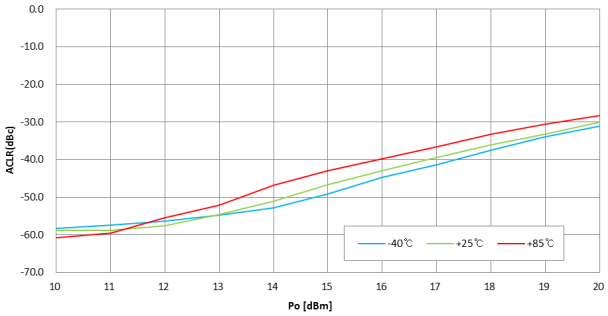


Figure 87. 3GPP WCDMA ACLR vs Output Power
@3700MHz, WCDMA 1FA , TM1+64DPCH ±5MHz offset

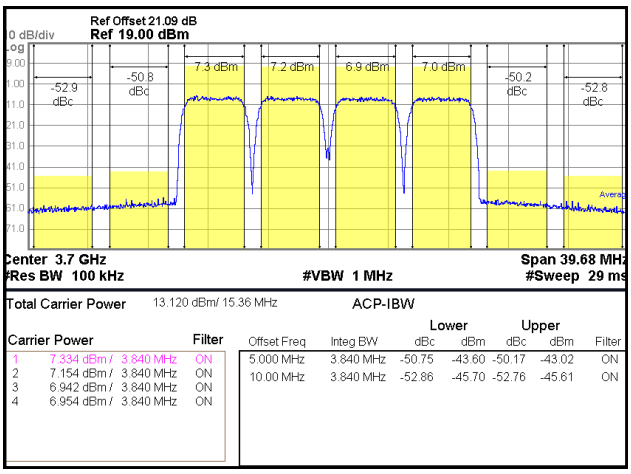


0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140 EVK - PCB(3700MHz Application Circuit)

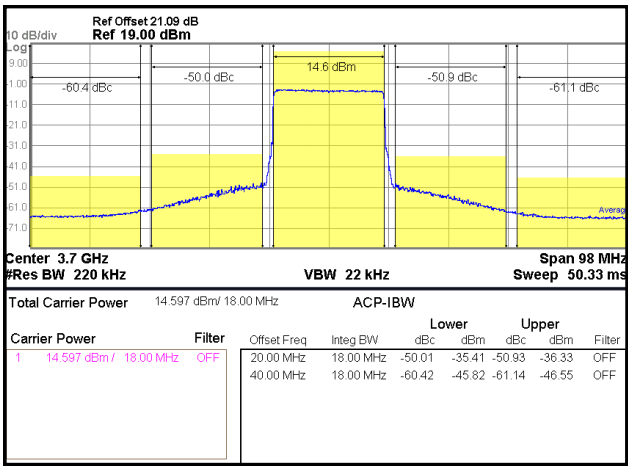
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted and RF Circuit

Figure 88. ACLR @3700MHz, WCDMA4FA[1], -50dBc



1. WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 10.11 at 0.01% Prob

Figure 89. ACLR @3700MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob.

Figure 90. Evaluation Board PCB Layer Information

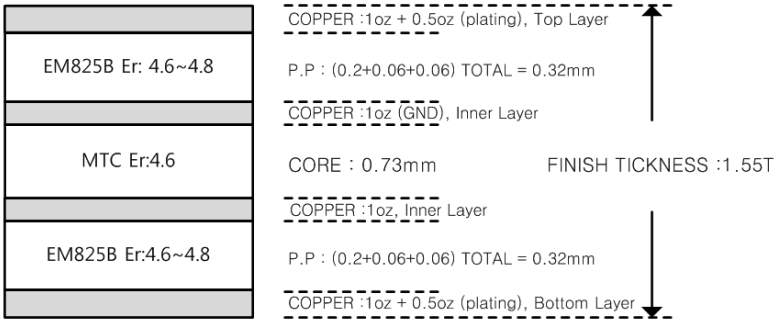
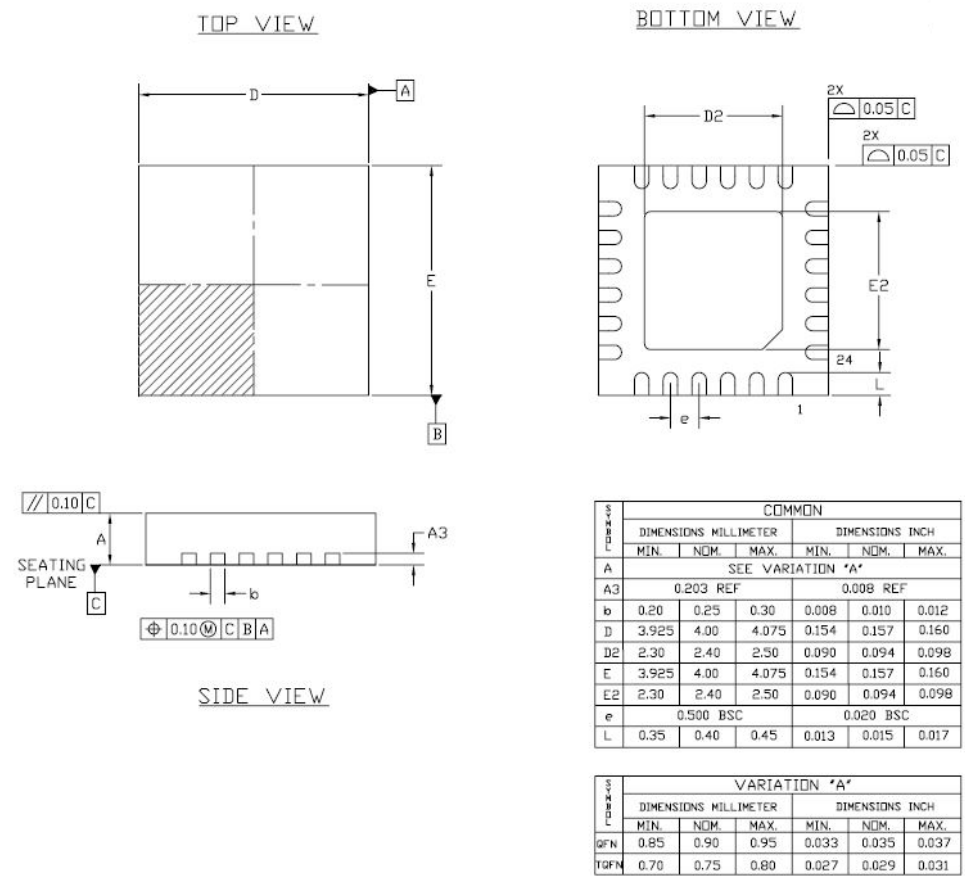


Table 23. Bill of material Information

No.	Value	Description	Manuf.	Part Number
1	1.0nF	IND, 0402, CHIP, 5%	murata	LQG15HS1N0S02D
2	1.2nH	IND, 0402, CHIP, 5%	murata	LQG15HS1N2S02D
3	1.5nH	IND, 0402, CHIP, 5%	murata	LQG15HS1N5S02D
4	2.0nH	IND, 0402, CHIP, 5%	murata	LQG15HS2N0S02D
5	3.0nH	IND, 0402, CHIP, 5%	murata	LQG15HS3N0S02D
6	4.3nH	IND, 0402, CHIP, 5%	murata	LQG15HS4N3S02D
7	4.7nH	IND, 0402, CHIP, 5%	murata	LQG15HS4N7S02D
8	5.1nH	IND, 0402, CHIP, 5%	murata	LQG15HS5N1S02D
9	10nH	IND, 0402, CHIP, 5%	murata	LQG15HS10NJ02D
10	15nH	IND, 0402, CHIP, 5%	murata	LQG15HS15NJ02D
11	22nH	IND, 0402, CHIP, 5%	murata	LQG15HS22NJ02D
12	27nH	IND, 0402, CHIP, 5%	murata	LQG15HS27NJ02D
13	33nH	IND, 0402, CHIP, ±5%	murata	LQG15HS33NJ02D
14	0.5pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C0R5CB5NNNC
15	0.75pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05CR75CB5NNNC
16	1.0pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R0CB5NNNC
17	1.2pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R2CB5NNNC
18	1.3pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R3CB5NNNC
19	1.5pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R5CB5NNNC
20	1.8pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R8CB5NNNC
21	2.0pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C020CB5NNNC
22	7.5pF	CAP, 0402, CHIP Ceramic, ±0.25%	WALSIN tech	0402N7RD500CT
23	9pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C090CB5NNNC
24	10pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C100CB5NNNC
25	20pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C200CB5NNNC
26	22pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C220CB5NNNC
27	62pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C620CB5NNNC
28	100pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C101CB5NNNC
29	1nF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C102CB5NNNC
30	1uF	CAP, 0402, (105Z 10V)	WALSIN tech	0402F105Z100CT
31	0ohm	RES, 0402, CHIP, ±5%	samsung	RC1005J000CS

Figure 91. Packing outline Dimension



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	SEE VARIATION "A"					
A3	0.203 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.925	4.00	4.075	0.154	0.157	0.160
D2	2.30	2.40	2.50	0.090	0.094	0.098
E	3.925	4.00	4.075	0.154	0.157	0.160
E2	2.30	2.40	2.50	0.090	0.094	0.098
e	0.500 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017

SYMBOL	VARIATION "A"					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
QFN	0.85	0.90	0.95	0.033	0.035	0.037
TQFN	0.70	0.75	0.80	0.027	0.029	0.031

NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM. FROM TERMINAL TIP.

Figure 92. Package Marking

YY = Year, WW = Working Week, XX = Wafer No.

Figure 93. Suggested PCB Land Pattern and PAD Layout

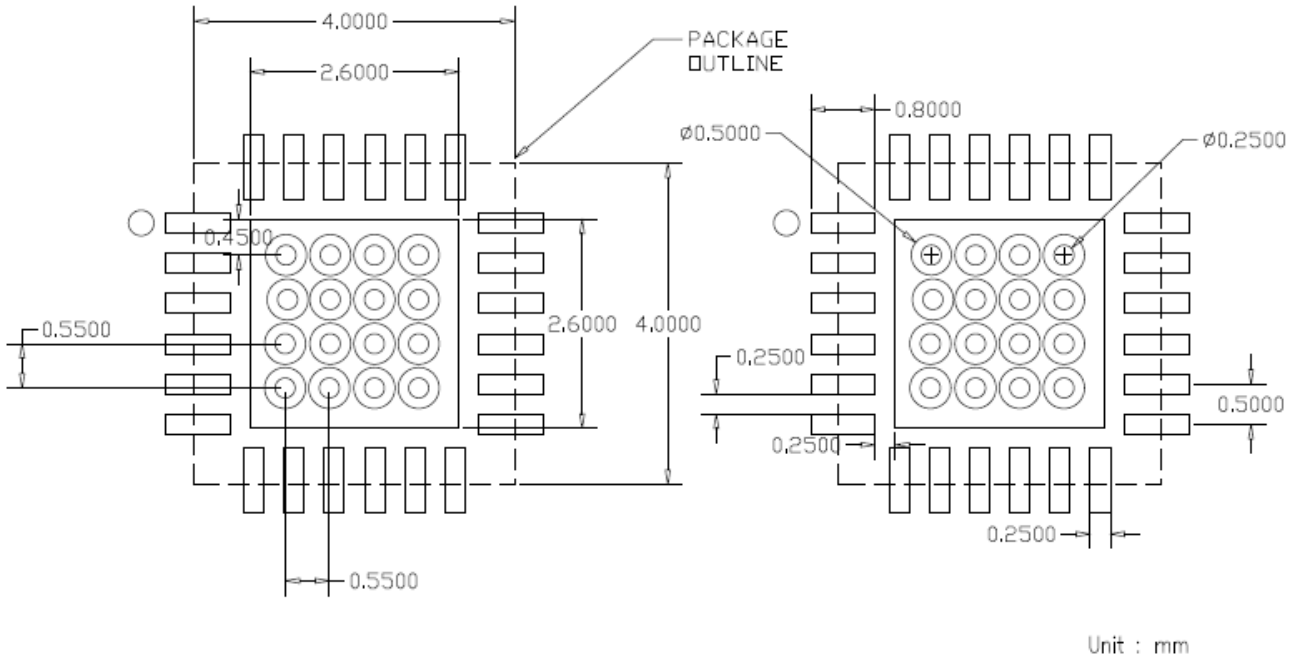
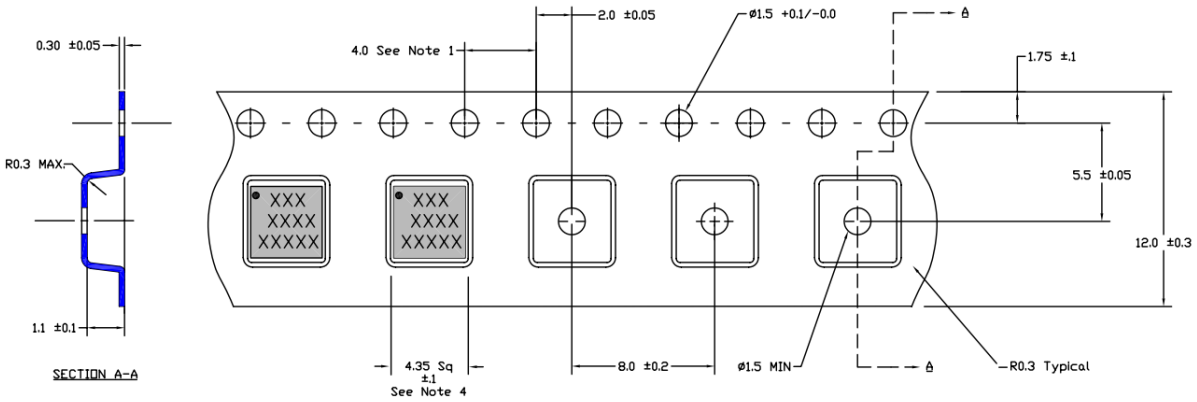


Figure 45. Tape & Reel



Packaging information:
Tape Width (mm): 12 / Reel Size (inches): TBD

Device Cavity Pitch (mm): 8 / Devices Per Reel: TBD

Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	**Passes<2000V**
Test:	Human Body Model(HBM)
Standard:	JEDEC Standard JS-001-2014
MSL Rating:	**Level 1 at +265°C convection reflow**
Standard:	JEDEC Standard J-STD-020

Proper ESD procedures should be followed when handling this device.

NATO CAGE code:

2	N	9	6	F