BVA518C

Wide Band Digital Variable Gain Amplifier

5-4000 MHz

Device Features

- Integrate DSA to Amp Functionality
- Power Supply Range
  AMP : Nominal 5.0V
  DSA : 2.7V to 5.5V
- 5-4000MHz Broadband Performance
- 20.0dB Gain @ 1.9GHz
- 5.3dB Noise Figure at max gain setting @ 1.9GHz
- 19dBm P1dB @ 1.9GHz
- 32.7dBm OIP3 @ 1.9GHz
- No matching circuit needed
- Attenuation: 0.5 dB steps up to 31.5 dB
- Safe attenuation state transitions
- High attenuation accuracy (DSA to Amp)
  ±(0.25 + 3% x ATT) @ 1.9GHz
- 1.8V control logic compatible
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
- Unique power-up state selection
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package

24-lead 4mm x 4mm x 0.9mm QFN

Figure 1. Package Type

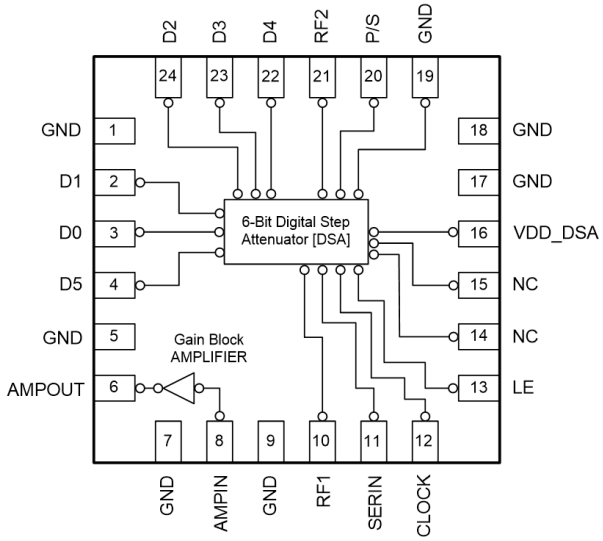


Figure 2. Functional Block Diagram

Product Description

The BVA518C is a digitally controlled variable gain amplifier (DVGA) is featuring high linearity using the voltage 5V supply with a broadband frequency range of 5 to 4000MHz.

The BVA518C integrates a high performance digital step attenuator and high performance InGaP/GaAs HBT MMIC amplifier. Amplifier is internally matched to 50 Ohms and uses a patented **temperature compensation circuit** to provide stable current over the operating temperature range without the need for external components and a patented **over voltage protection circuit** to protect a internal device. The BVA518C is designed for high linearity gain block applications that require excellent gain flatness and designed for use in 3G/4G/5G wireless infrastructure and other high performance RF applications.

Both stages are internally matched to 50 Ohms and It is easy to use with no external matching components required.

The BVA518C always initialize to the maximum attenuation setting on power-up for both Serial and Parallel mode until next programming word is inputted.

The BVA518C is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

Application

- 5G/4G/3G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

Table 1. Electrical Specifications[1] @ VDD = 5V

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			5		4000	MHz
Gain		ATT = 0dB, at 1900MHz		20		dB
Attenuation Control range		0.5dB Step		31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	40MHz — 1GHz	Any bit or bit combination			±(0.25 + 2.5% of ATT setting)	dB
	1GHz — 2GHz				±(0.25 + 3% of ATT setting)	
	2GHz — 3GHz				±(0.25 + 3% of ATT setting)	
	3GHz — 4GHz				±(0.25 + 3.5% of ATT setting)	
Input Return Loss	5MHz — 700MHz	ATT = 0dB	8	15		dB
	700MHz — 2GHz		13	17		
	2GHz — 3GHz		13	17		
	3GHz — 4GHz		10	13		
Output Return Loss	5MHz — 700MHz	ATT = 0dB	8	20		dB
	700MHz — 2GHz		15	20		
	2GHz — 3GHz		15	25		
	3GHz — 4GHz		13	20		
Output Power for 1dB Compression (OP1dB)		ATT = 0dB , at 1900MHz		18.8		dBm
Output Third Order Intercept Point[2] (OIP3)		ATT = 0dB, at 1900MHz		32.8		dBm
Adjacent Channel Leakage Ratio[3] (ACLR)		Output Power @ 50dBc ATT = 0dB, at 1900MHz		9		dBc
Noise Figure		ATT = 0dB, at 1900MHz		5.3		dB
DSA Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Maximum Spurious level		Measured at DSA RF1, RF2 ports		< -145		dBm
Impedance				50		Ω

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. (DSA to AMP)
2. OIP3 measured with two tone at 3dBm output per tone separated by 1MHz.
3. ACLR measured with 5GNR 100MBW PAR=9.6dB.

Table 2. Typical RF Performance[1]

Parameter	Frequency							Unit
	100[2]	500[2]	900[3]	1800[3]	2100[3]	2700[3]	3500[3]	MHz
Gain	22.8	22.1	21.5	20.2	19.6	18.0	15.6	dB
Input Return Loss	-11.5	-20.3	-18.5	-14.8	-14.9	-17.9	-12.2	dB
Output Return Loss	-13.1	-20.0	-16.4	-17.8	-18.2	-25.0	-24.0	dB
OIP3[4]	35.9	36.9	35.5	33.0	32.4	31.3	28.5	dBm
P1dB	19.8	20.3	20.0	19.1	18.5	17.3	15.2	dBm
ACLR 50dBc @ 5GNR 100MBW	-	10.5	10.2	9.1	8.5	7.0	4.7	dBm
Noise Figure	4.6	4.7	4.8	5.3	5.3	5.8	6.2	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. (DSA to AMP)
2. 100MHz and 500MHz measured with application circuits refer to table 11.
3. 900MHz to 3500MHz measured with application circuit refer to table 13.
4. OIP3 measured with two tone at 3dBm output per tone separated by 1MHz.

Table 3. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	AMP + DSA	5		4000	MHz
Supply Voltage, VDD	AMP VDD	4.75	5	5.25	V
	DSA VDD	2.7		5.5	V
Current, IDD	AMP ON @ VDD=5V	67	77	87	mA
	DSA	100	200	300	uA
DSA Control Voltage	Digital Input High	1.17		3.6	V
	Digital Input Low	-0.3		0.6	V
DSA Control pin Current	Digital Input High			20	uA
Operating Temperature	AMP + DSA	-40		105	℃

Specifications are not guaranteed over all recommended operating conditions.

Table 4. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	AMP			6.0	V
	DSA			5.5	V
Supply Current	AMP			160	mA
	DSA			1000	uA
Digital input voltage	DSA Control Pin (LE, SERIN, CLK, P/S, D0, D1, D2, D3, D4, D5)	-0.3		3.6	V
Maximum input power	AMP			23	dBm
	DSA			30	dBm
Storage Temperature		-55		150	℃
Junction Temperature			150		℃

Operation of this device above any of these parameters may result in permanent damage.

Figure 3. Pin Configuration (Top View)

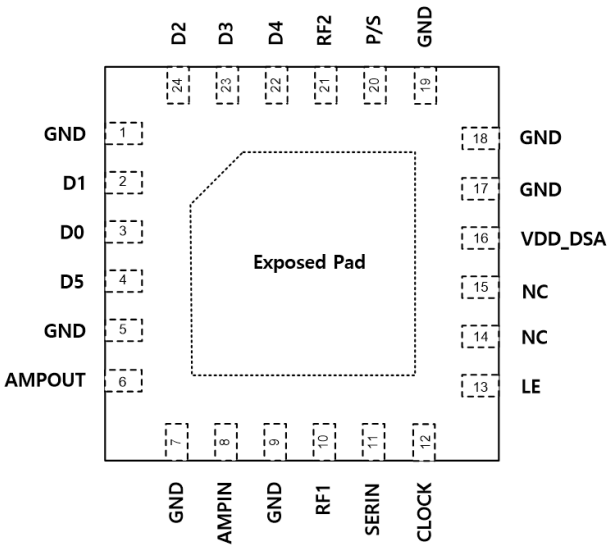


Table 5. Pin Description

Pin	Pin name	Description
2	D1	Parallel Control Voltage Input, Attenuation control bit 1dB.
3	D0	Parallel Control Voltage Input, Attenuation control bit 0.5dB.
4	D5	Parallel Control Voltage Input, Attenuation control bit 16dB.
6	AMPOUT	RF Amplifier Output & Amplifier Power Supply Input.
8	AMPIN	RF Amplifier input. This pin should be connected to RF1 (Pin 10) with DC blocking Capacitor.
10	RF1[1]	RF1 port. (DSA RF Output) This pin should be connected to AMPIN (Pin 8) with DC blocking Capacitor.
11	SERIN	Serial interface data input.
12	Clock	Serial interface clock input.
13	LE	Latch Enable input.
14,15	NC	Not connected, It doesn't matter whether this pin is High or Low. Basically, it is recommended to set to GND.
16	VDD_DSA	DSA Power Supply (nominal 3.3V)
20	P/S	Parallel/Serial Mode Selection input. For parallel mode operation, set this pin to LOW. For serial mode operation, set this pin to HIGH.
21	RF2[1]	RF2 port. (DSA RF Input) This pin is a main RF input port. (DSA + Amplifier structure)
22	D4	Parallel Control Voltage Inputs, Attenuation control bit 8dB
23	D3	Parallel Control Voltage Inputs, Attenuation control bit 4dB
24	D2	Parallel Control Voltage Inputs, Attenuation control bit 2dB
1,5,7,9, 17,18,19	GND	Ground, These pins must be connected to ground.
EXPOSE PAD	GND	Exposed pad : The exposed pad must be connected to ground for proper operation.

1. RF pins 10 and 21 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met.

Programming Options

BVA518C can be programmed using either the parallel or serial interface, which is selectable via P/S pin (Pin20).
Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW.

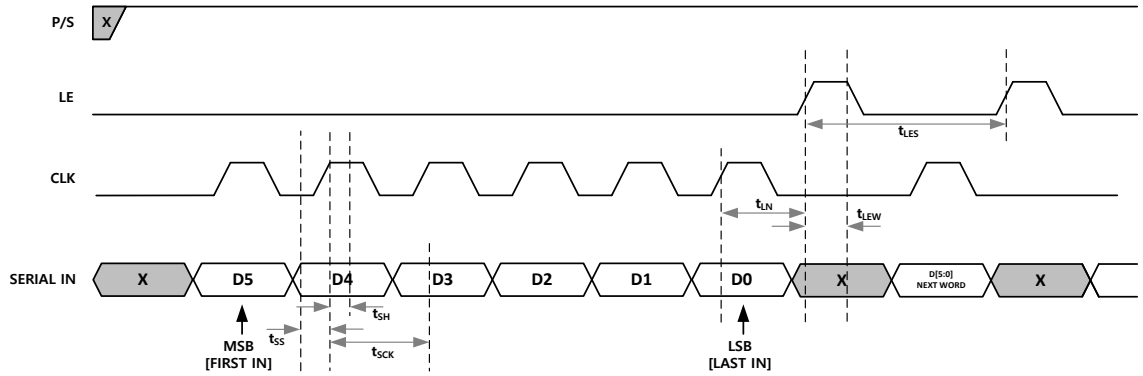
Table 6. Mode Selection

P/S	Control Mode
LOW	Parallel
HIGH	Serial

Serial Control Mode

The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. When serial programming is used, all the parallel control input pins (2,3,4,22,23,24) should be grounded.
It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Figure 4. Serial Mode Resister Timing Diagram



The BVA518C has a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to HIGH.
In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled HIGH to latch the new attenuation state into the device. LE must be set to LOW to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept HIGH (see Figure 4 and Table 8).

Table 7. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{Clk}	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns
t_{LES}	Minimum LE pulse spacing		600		ns

Table 8. Truth Table for Serial Control Word

Serial Control Input						Attenuation State [dB]
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	
LOW	LOW	LOW	LOW	LOW	LOW	0
LOW	LOW	LOW	LOW	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	1
LOW	LOW	LOW	HIGH	LOW	LOW	2
LOW	LOW	HIGH	LOW	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	31.5

Parallel Control Mode

The BVA518C has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 10. The parallel control interface is activated when P/S is set to LOW. There are two modes of parallel operation: direct parallel and latched parallel

Direct Parallel Mode

The LE pin must be kept High. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 2, 3, 4, 22,23, 24]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the desired attenuation state.
LE must be toggled High to Low to latch the desired attenuation state into the device. And then LE should be held Low again until the next attenuation value to be set. (see Figure 5 and Table 10).

Power-UP Interface

The BVA518C basically is set the maximum attenuation state when the initially powered up for all serial and latched parallel mode status until the next programming word is inputted.
If the BVA518C powered up in serial mode, all parallel data pins [2,3,4,22,23,24] do not matter whether they are high or low. Basically, it is recommended to set these pins to Logic low.

Figure 5. Latched Parallel Mode Timing Diagram

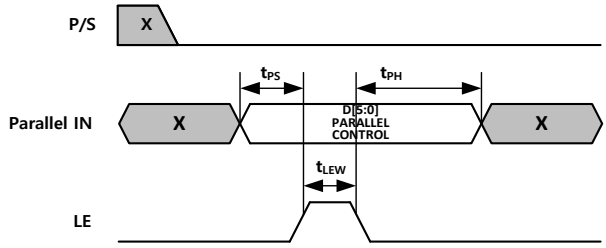


Table 9. Latched Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{LEW}	Minimum LE pulse width	10			ns
t_{PH}	Data hold time from LE	10			ns
t_{PS}	Data setup time to LE	10			ns

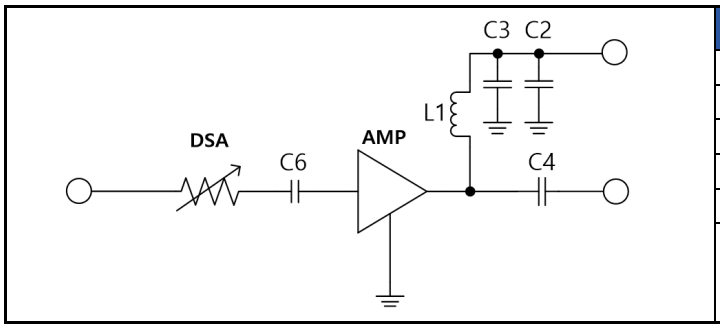
Table 10. Truth Table for Parallel Control Word

Parallel Control Input						Attenuation State [dB]
D5	D4	D3	D2	D1	D0	
LOW	LOW	LOW	LOW	LOW	LOW	0
LOW	LOW	LOW	LOW	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	1
LOW	LOW	LOW	HIGH	LOW	LOW	2
LOW	LOW	HIGH	LOW	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	31.5

Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 100 ~ 700MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Table 11. 100 ~ 700MHz RF Application Circuit



BOM	
L1	270nH
C4	1nF
C6	1nF
C2	100nF
C3	100pF

This value can be changed little by little according to the frequency band and bandwidth.

Table 12. Typical RF Performance @ VDD = 5V

Parameter	Frequency				Unit
	100	300	500	700	MHz
Gain	22.8	22.3	22.1	22	dB
S11	-11.5	-17.9	-20.3	-21.5	dB
S22	-13.1	-19.7	-20	-21.5	dB
OIP3[1]	35.9	36.5	36.9	35.1	dBm
P1dB	19.8	20	20.3	20.1	dBm
ACLR 50dBc	-	10.5	10.5	10.3	dBm
Noise Figure	4.6	4.7	4.7	4.7	dB

1. OIP3 measured with two tones at an output of 3dBm per tone separated by 1MHz.
2. ACLR measured with 5GNR 100MBW PAR=9.6dB .

Figure 6. Gain

: Max Gain (ATT=0dB)

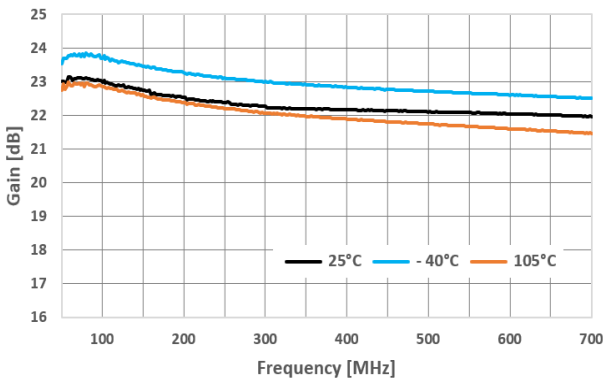
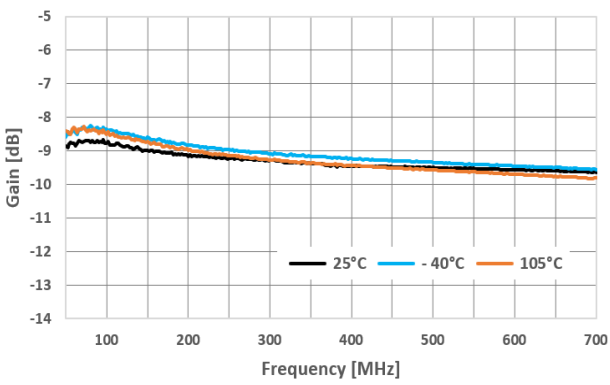


Figure 7. Gain vs. Frequency

: Min Gain (ATT=31.5dB)



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 100 ~ 700MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 8. Gain

: Major Attenuation States

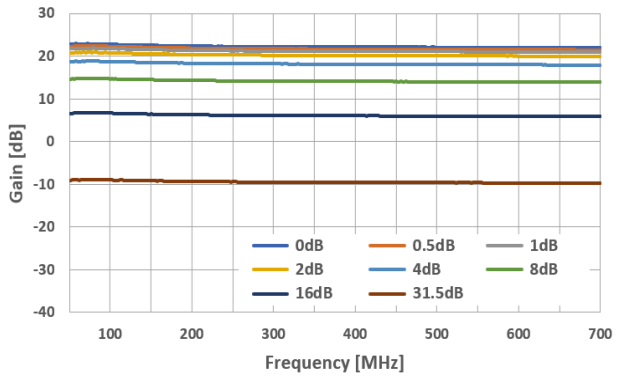


Figure 9. Input Return Loss

: Max Gain

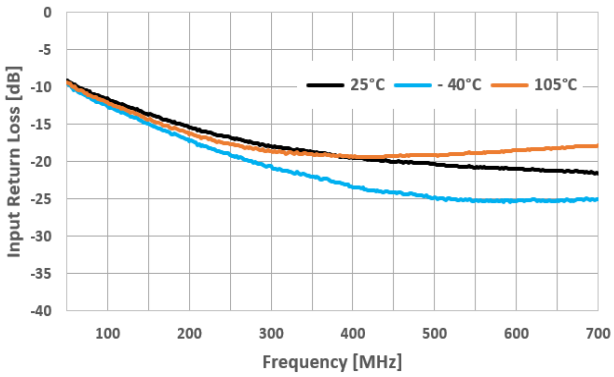


Figure 10. Input Return Loss

: Min Gain

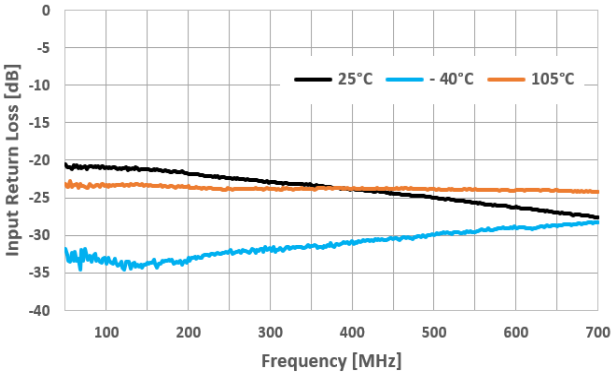


Figure 11. Input Return loss vs. Frequency

: Major Attenuation States

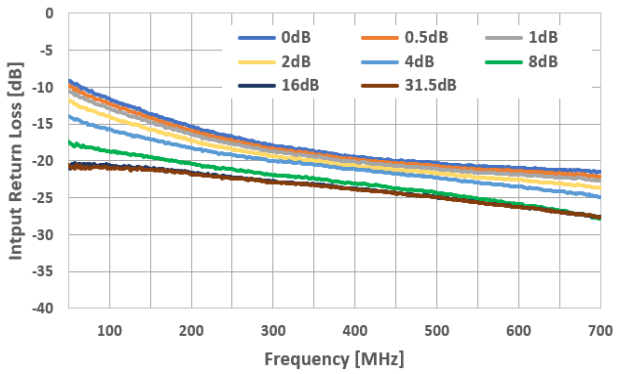


Figure 12. Output Return Loss

: Max Gain

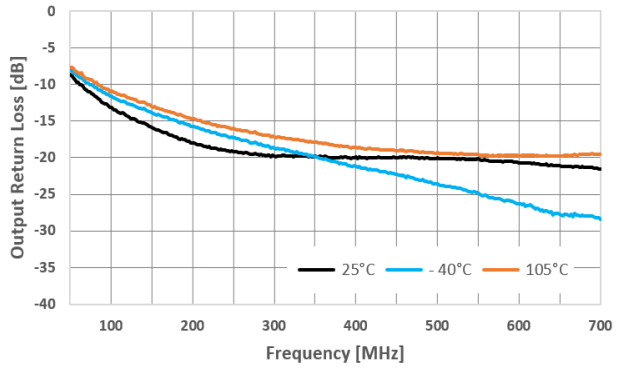
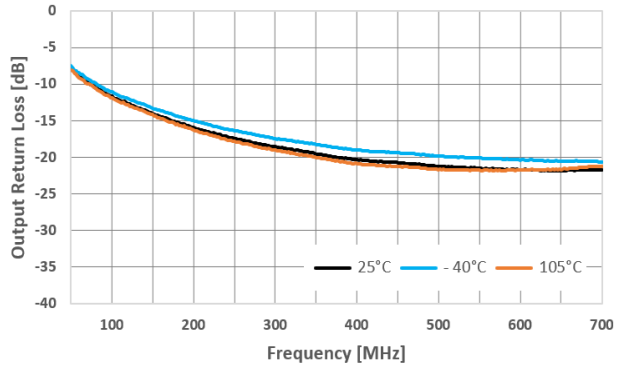


Figure 13. Output Return Loss

: Min Gain



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 100 ~ 700MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 14. Output Return Loss

: Major Attenuation States

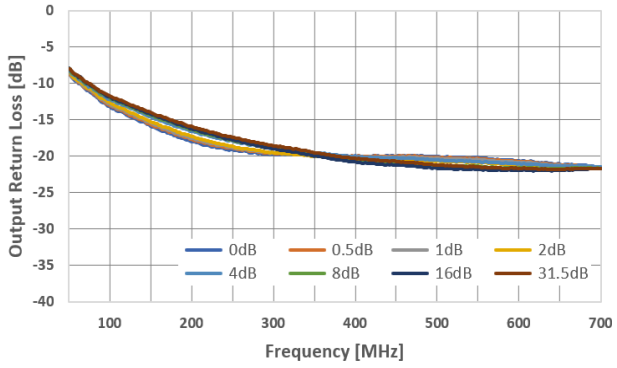


Figure 15. Attenuation Error

: Major Attenuation States

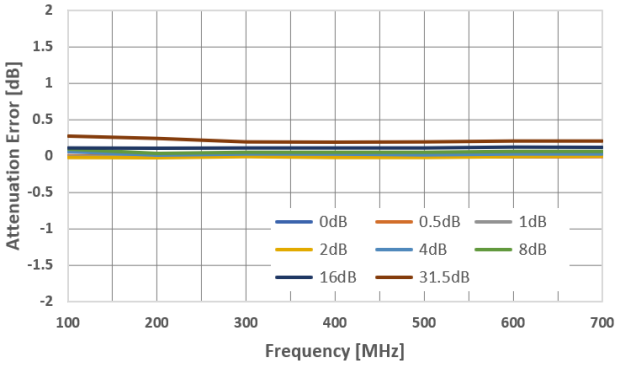


Figure 16. Attenuation Error

: Frequency

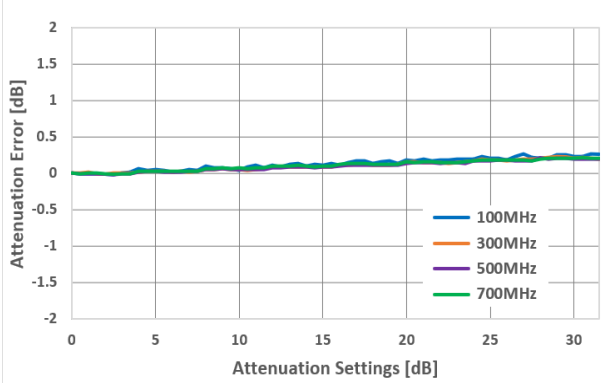


Figure 17. Attenuation Error @ 100MHz

: 100MHz

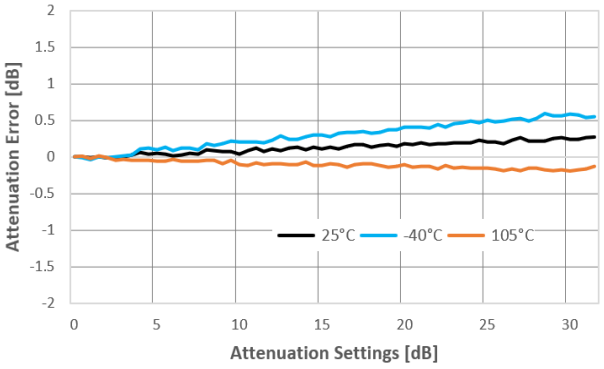


Figure 18. Attenuation Error @ 500MHz

: 500MHz

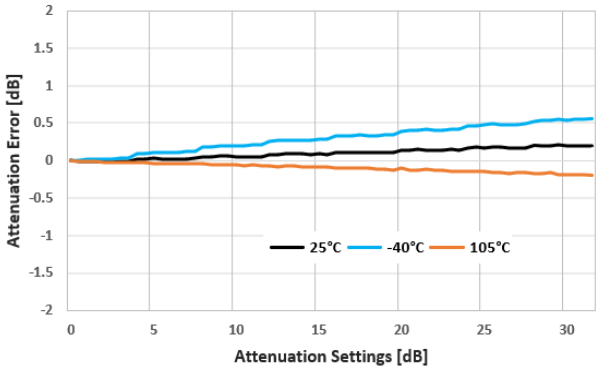
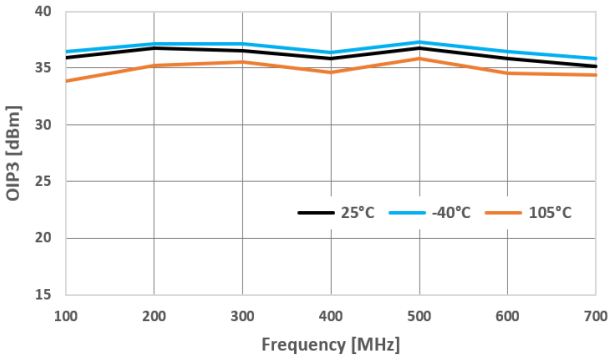


Figure 19. OIP3

: Max Gain



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 100 ~ 700MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 20. OP1dB

: Max Gain

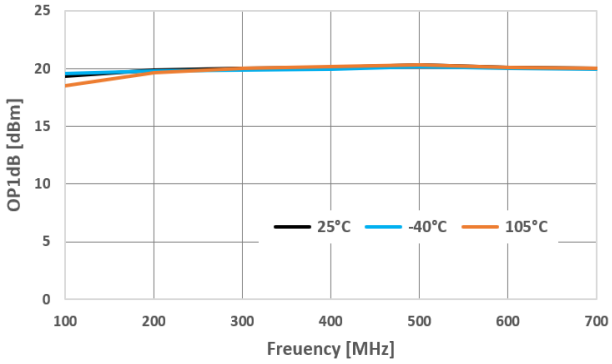


Figure 21. ACLR @ 300MHz

: Max Gain, 5GNR 100MBW PAR=9.6dB

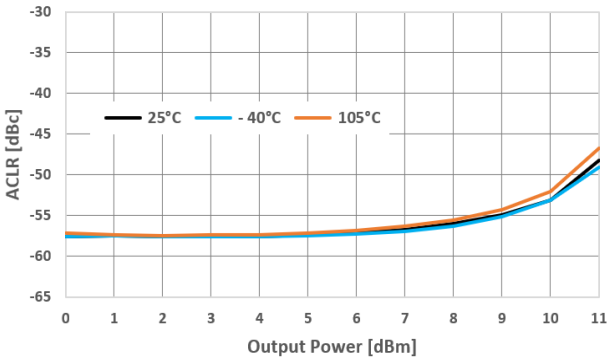


Figure 22. ACLR @ 500MHz

: Max Gain, 5GNR 100MBW PAR=9.6dB

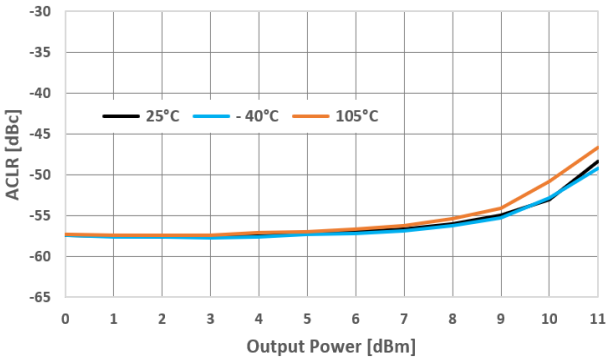


Figure 23. ACLR 50dBc @ 500MHz

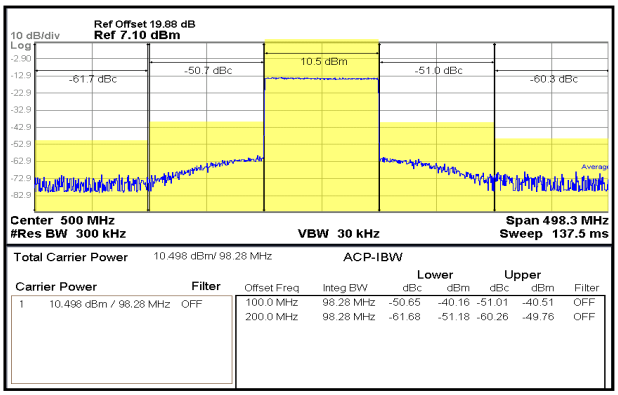
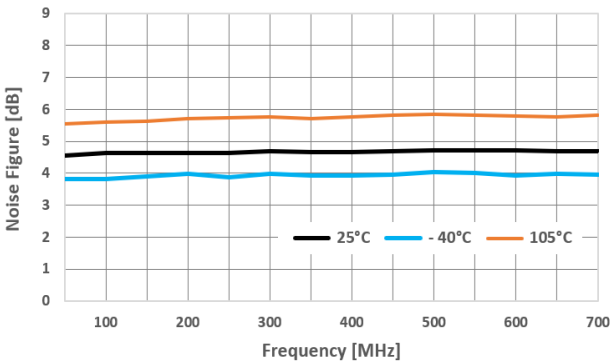


Figure 24. Noise Figure

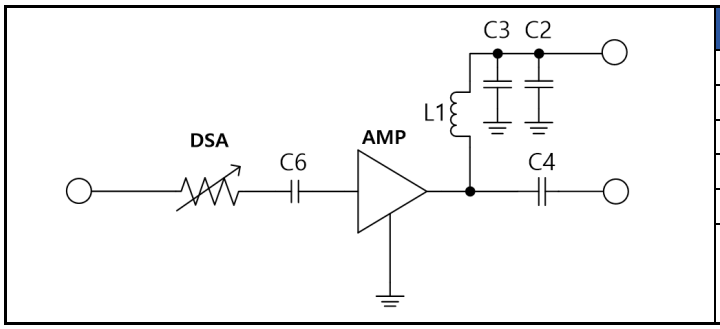
: Max Gain



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 13

Table 13. 800 - 4000MHz RF Application Circuit



BOM	
L1	27nH
C4	100pF
C6	100pF
C2	100nF
C3	100pF

This value can be changed little by little according to the frequency band and bandwidth.

Table 14. Typical RF Performance @ VDD = 5V

Parameter	Frequency					Unit
	900	1800	2100	2700	3500	MHz
Gain	21.5	20.2	19.6	18	15.6	dB
S11	-18.5	-14.8	-14.9	-17.9	-12.2	dB
S22	-16.4	-17.8	-18.2	-25	-24	dB
OIP3[1]	35.5	33	32.4	31.3	28.5	dBm
P1dB	20	19.1	18.5	17.3	15.2	dBm
ACLR[2] **50dBc**	10.2	9.1	8.5	7	4.7	dBm
Noise Figure	4.8	5.3	5.3	5.8	6.2	dB

1. OIP3 measured with two tones at an output of 3dBm per tone separated by 1MHz.
2. ACLR measured with 5GNR 100MBW PAR=9.6dB .

Figure 25. Gain

: Max Gain (ATT=0dB)

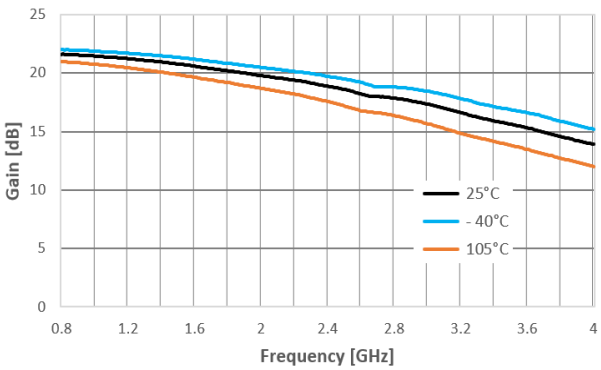
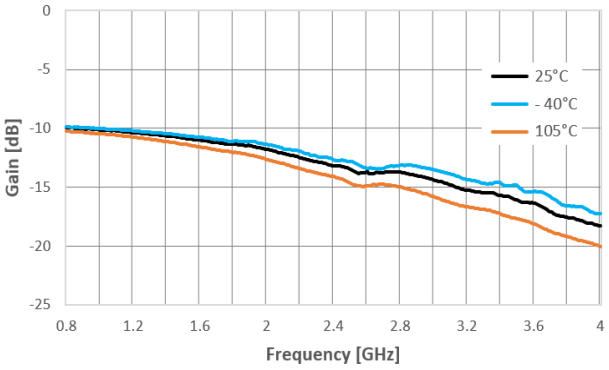


Figure 26. Gain

: Min Gain (ATT=31.5dB)



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 13

Figure 27. Gain vs. Frequency

: Major Attenuation States

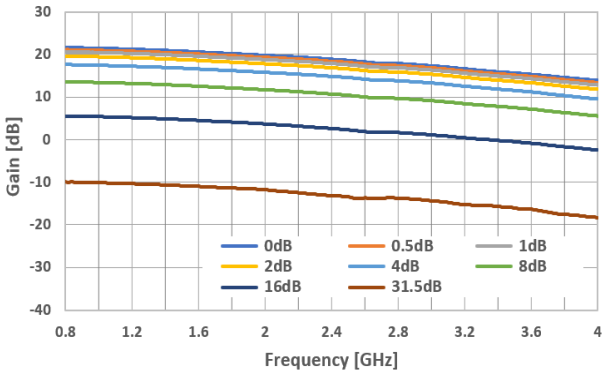


Figure 28. Input Return Loss

: Max Gain

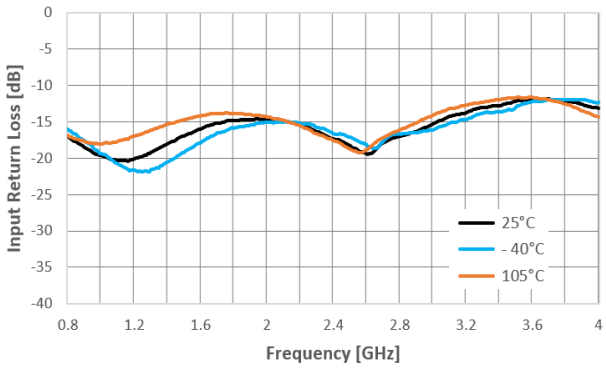


Figure 29. Input Return Loss

: Min Gain

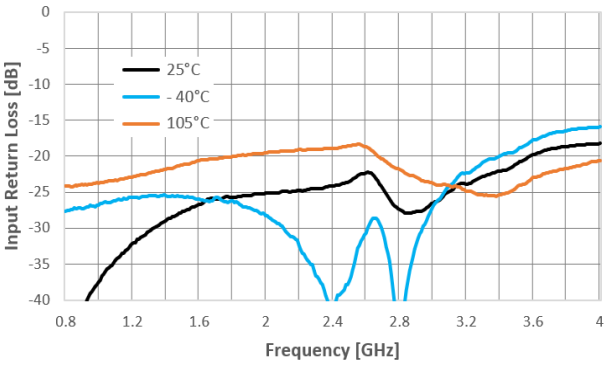


Figure 30. Input Return loss

: Major Attenuation States

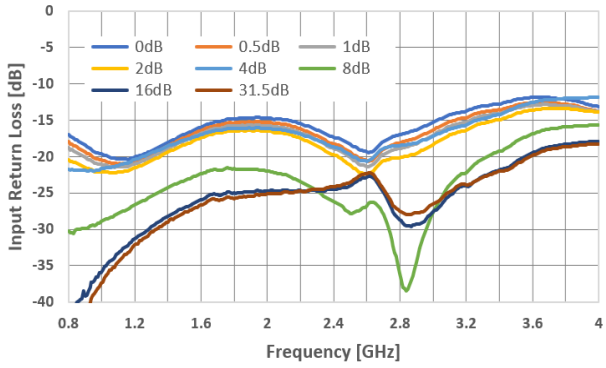


Figure 31. Output Return Loss

: Max Gain

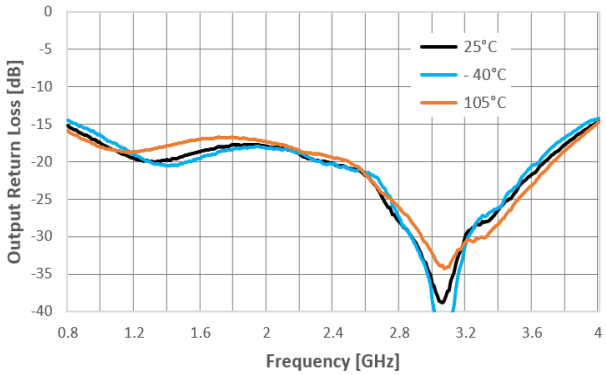
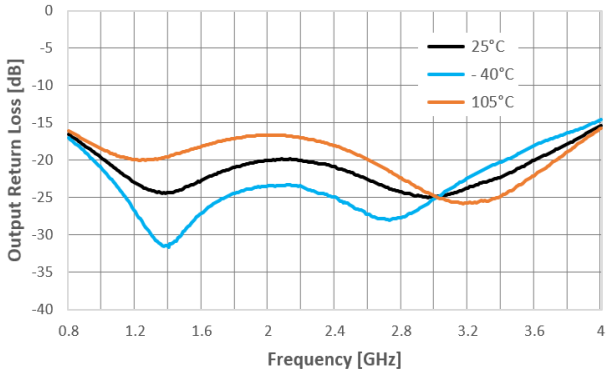


Figure 32. Output Return Loss

: Min Gain



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 13

Figure 33. Output Return Loss

: Major Attenuation States

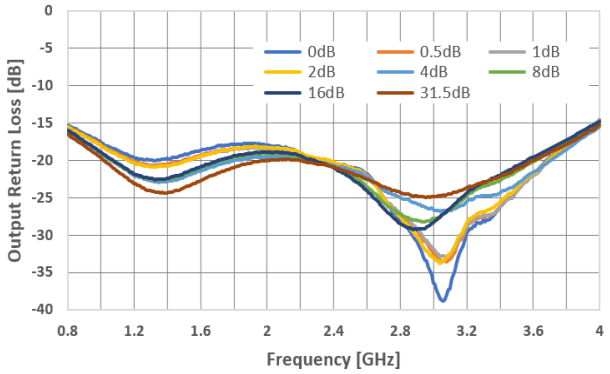


Figure 34. Attenuation Error

: Major Attenuation States

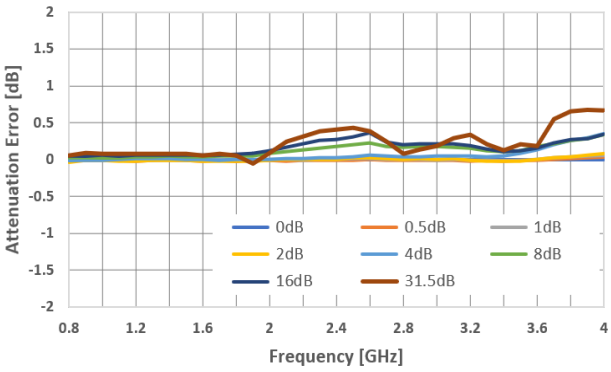


Figure 35. Attenuation Error

: Frequency

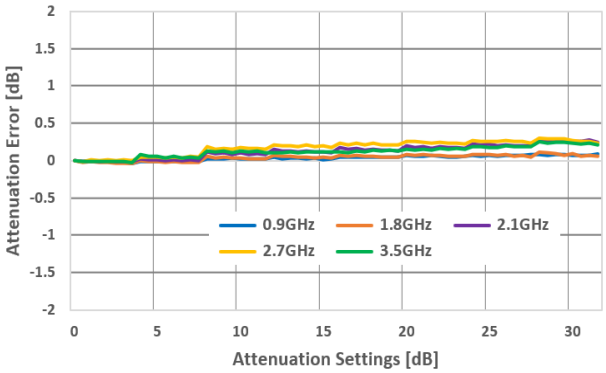


Figure 36. Attenuation Error @ 900MHz

: 900MHz

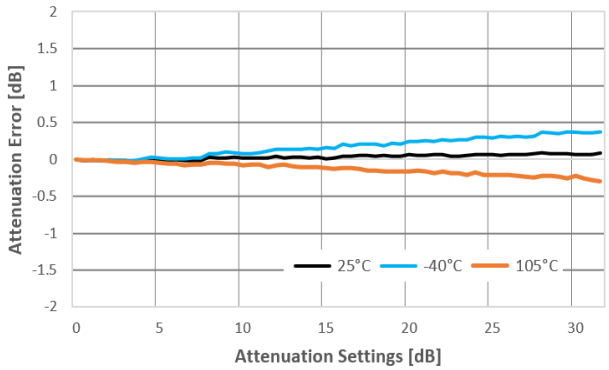


Figure 37. Attenuation Error @ 1800MHz

: 1800MHz

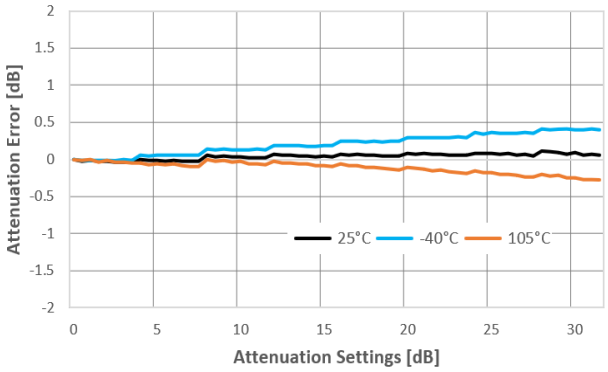
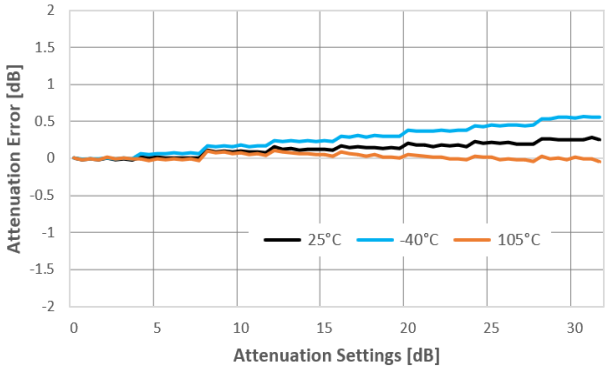


Figure 38. Attenuation Error @ 2100MHz

: 2100MHz



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 13

Figure 39. Attenuation Error @ 2700MHz

: 2700MHz

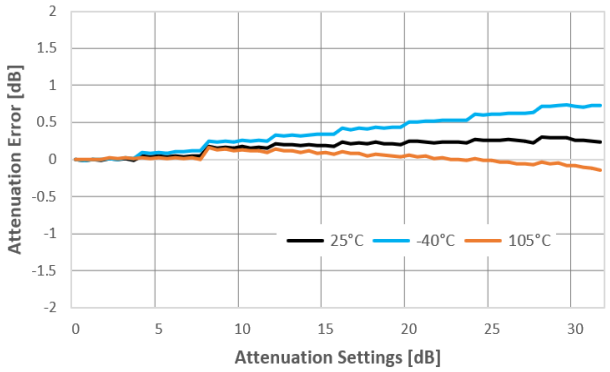


Figure 40. Attenuation Error @ 3500MHz

: 3500MHz

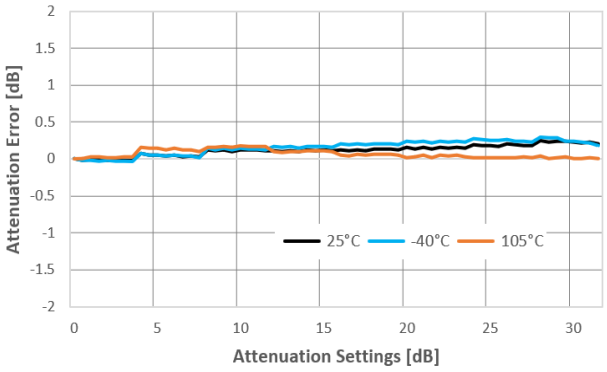


Figure 41. OIP3

: Max Gain

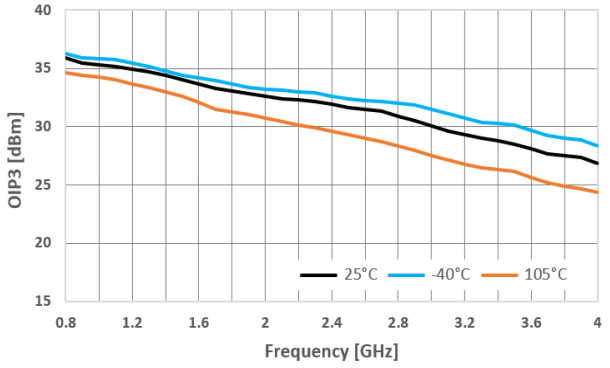


Figure 42. OP1dB

: Max Gain

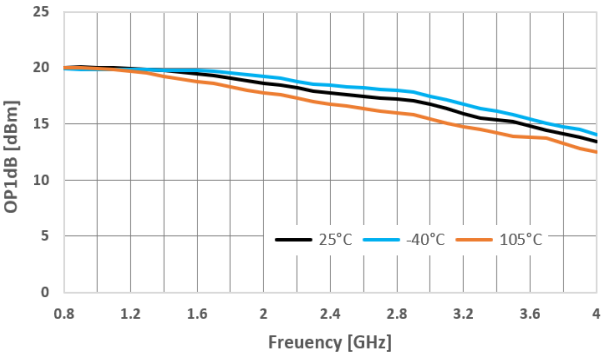


Figure 43. ACLR @ 900MHz

: Max Gain, 5GNR 100MBW PAR=9.6dB

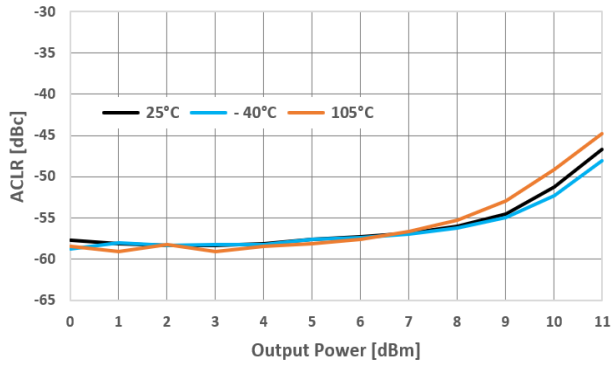
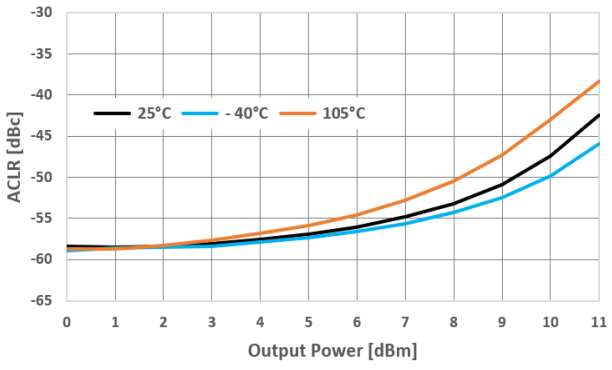


Figure 44. ACLR @ 1800MHz

: Max Gain, 5GNR 100MBW PAR=9.6dB



Typical RF Performance Plot - BVA518C EVK - PCB (Application Circuit : 800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 13

Figure 45. ACLR @ 2100MHz

: Max Gain, 5GNR 100MBW PAR=9.6dB

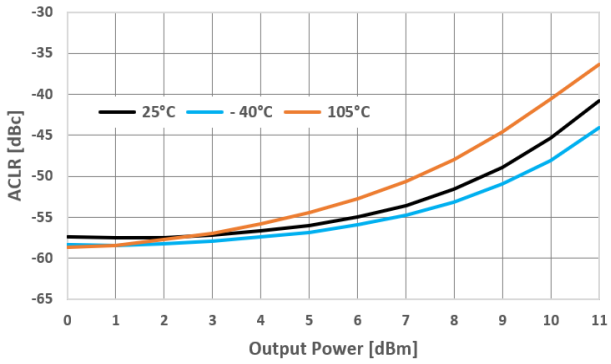


Figure 46. ACLR @ 2700MHz

: Max Gain, 5GNR 100MBW PAR=9.6dB

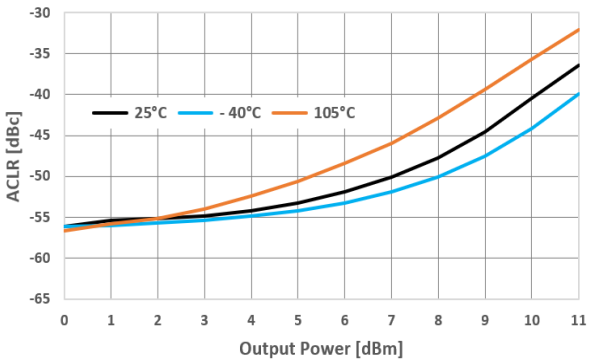


Figure 47. ACLR @ 3500MHz

: Max Gain, 5GNR 100MBW PAR=9.6dB

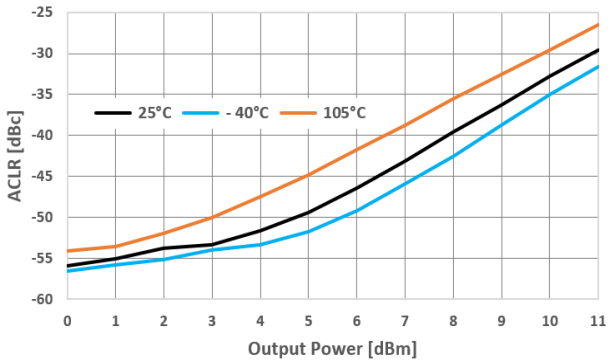


Figure 48. ACLR 50dBc @ 1800MHz

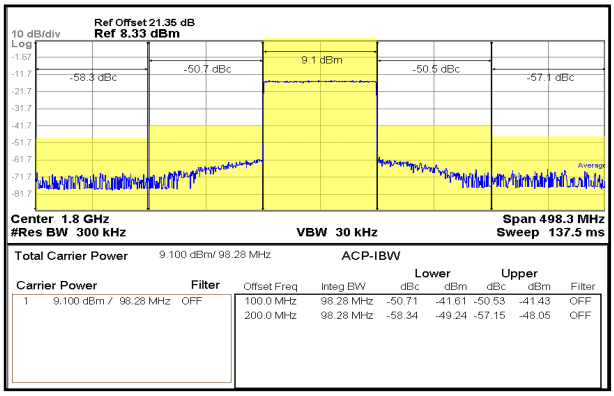


Figure 49. ACLR 50dBc @ 2700MHz

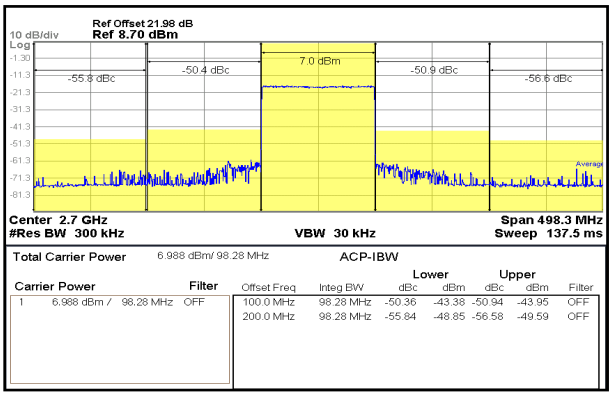


Figure 50. Noise Figure

: Max Gain

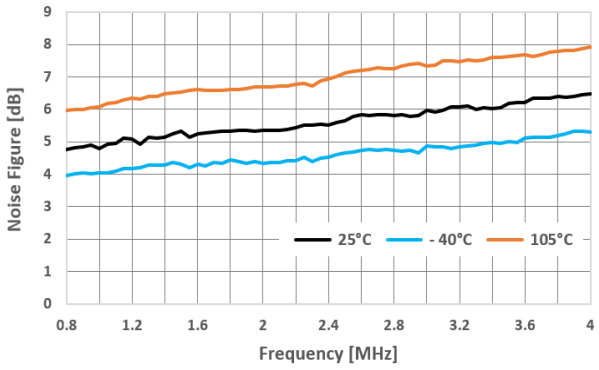


Figure 51. Evaluation Board Schematic

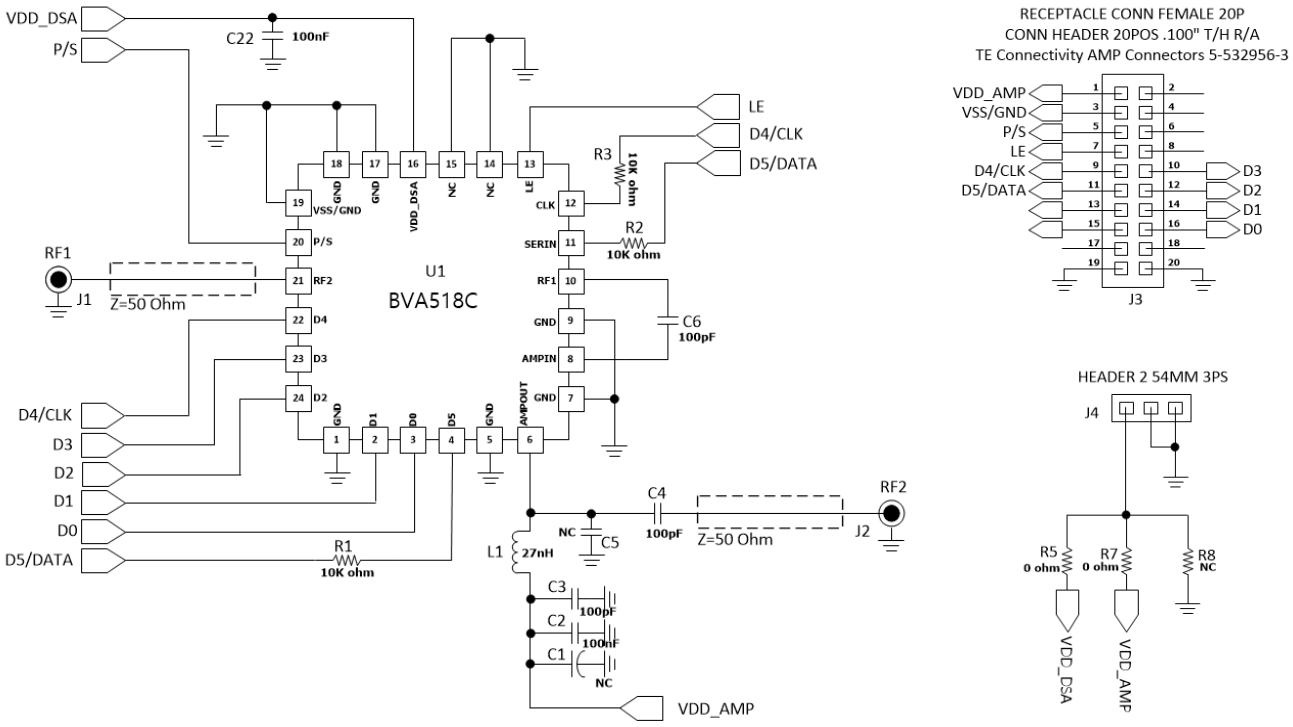


Table 15. Application Circuit

Application Circuit Values Example			
Freq. Band	IF Circuit 5 - 100MHz	IF Circuit 100 - 700MHz	RF Circuit 800MHz - 4GHz
C4/C6	10nF	10nF	100pF
L1	4.7uH	270nH	27nH

This value can be changed little by little according to the frequency band and bandwidth.

Figure 52. Evaluation Board layout

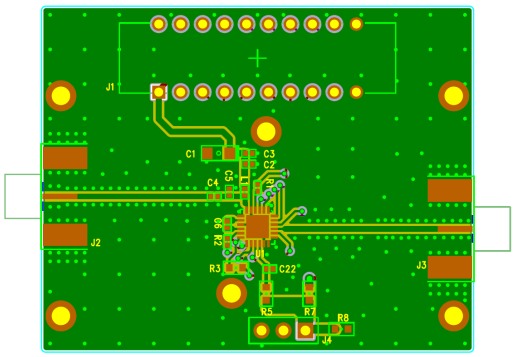


Table 16. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Part Number	REMARK
1	C4,C6	2	CAP 0402 100pF J 50V	
2	C2,C22	1	CAP 0402 100nF J 50V	
5	L1	1	IND 0402 27nH	
6	C3	1	CAP 0402 100pF J 50V	
7	R1,R2,R3	3	RES 0402 J 10K	
8	R5,R7	2	RES 0603 J 0ohm	
9	J1	1	Receptacle connector 20pin	
10	U1	1	QFN4X4_24L_BVA518C	
11	J2,J3	2	SMA_END_LAUNCH	
12	J4	1	Header 2.54mm 3pin	

This BOM is defined based on the 800MHz to 4GHz application circuit.

Figure 53. Suggested PCB Land Pattern and PAD Layout

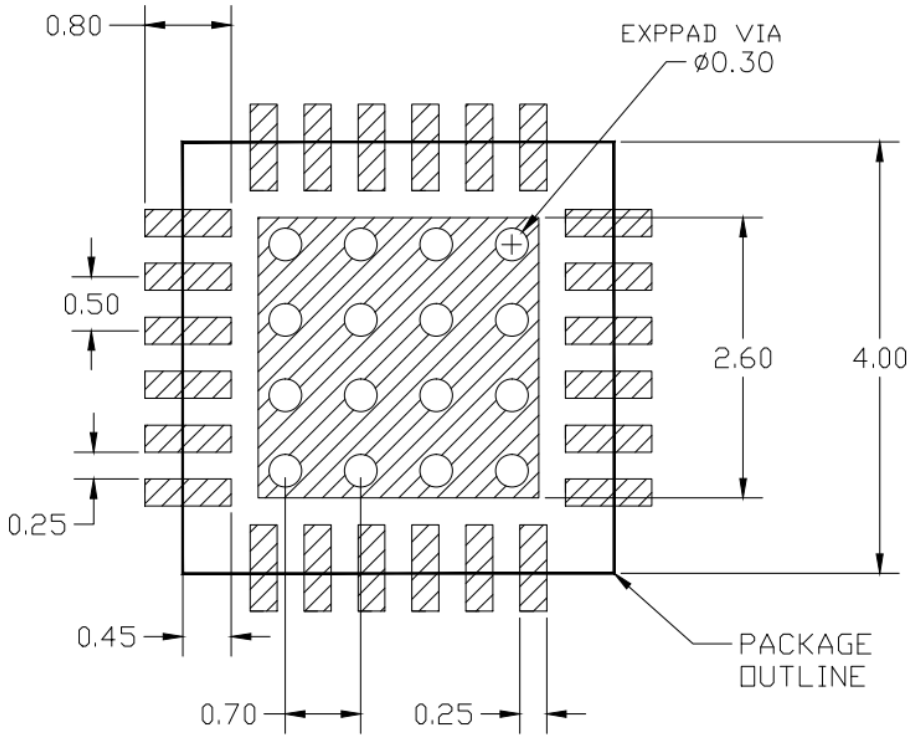


Figure 54. Evaluation Board PCB Layer Information

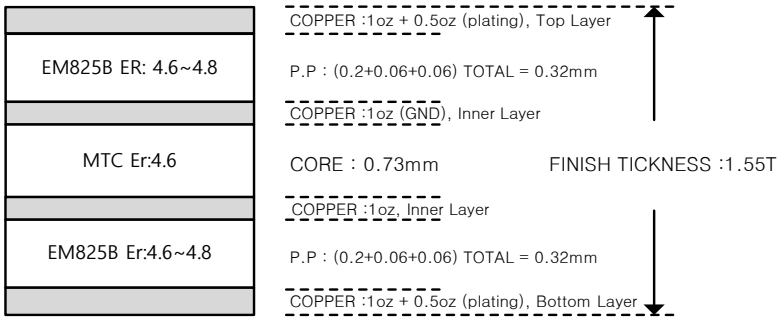
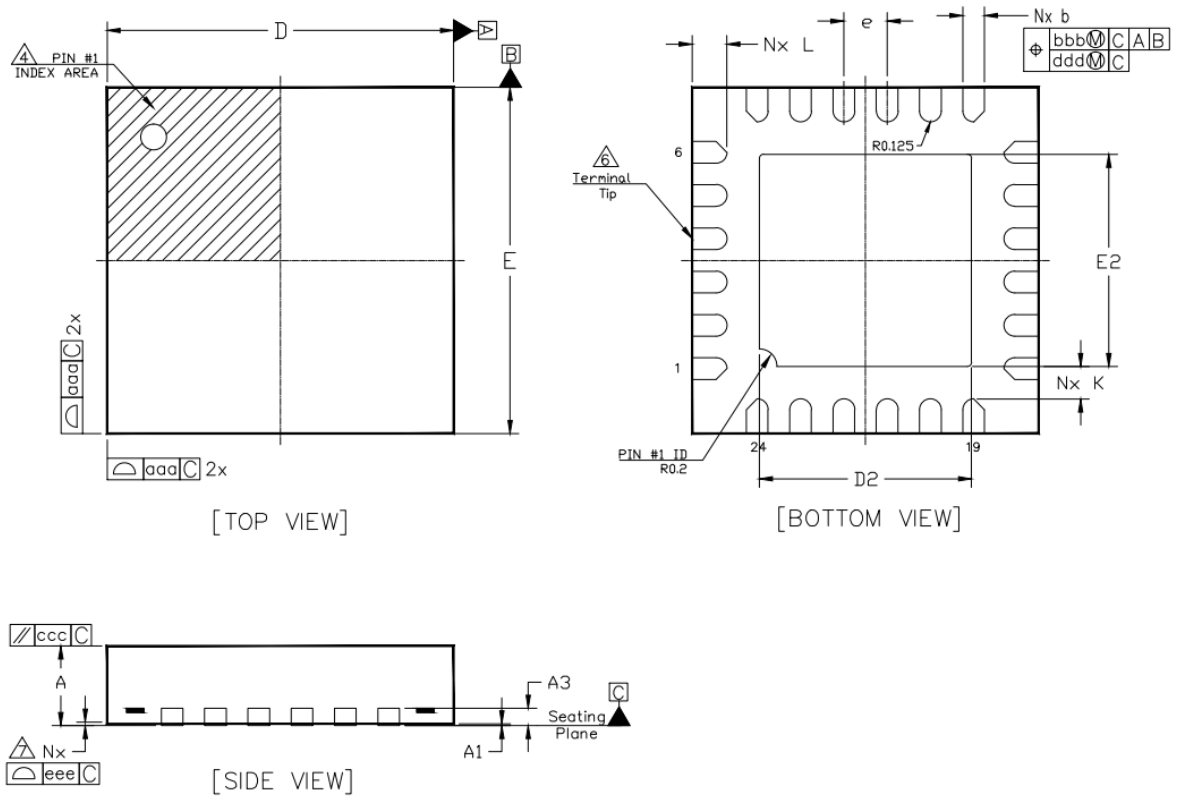


Figure 55. Package Outline Dimension

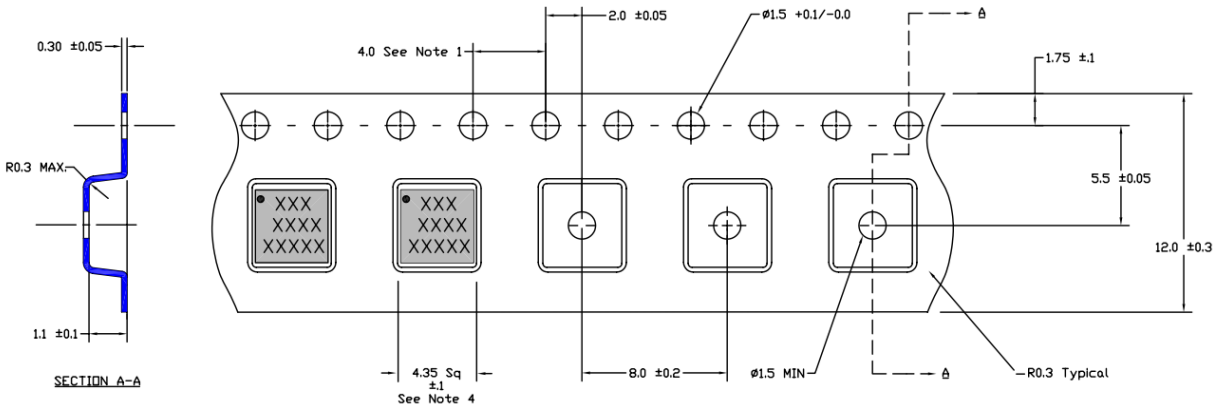


NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5–2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals each D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.3mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Dimension Table (Notes 1,2)				
Symbol Thickness	Min	Nominal	Max	Note
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.18	0.25	0.30	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	2.30	2.45	2.55	
E2	2.30	2.45	2.55	
K	0.2	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		24		3
ND		6		5
NE		6		5

Figure 56. Tape & Reel



Packaging information:	
Tape Width	12mm
Reel Size	7”
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 57. Package Marking

Marking information:	
BVA518C	Device Name
YY	Year
WW	Work Week
XX	Wafer Run Number

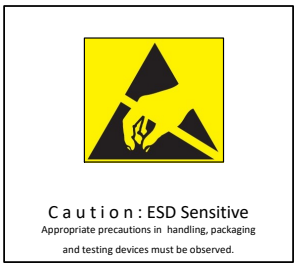
Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	**±1000V**
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**