BVA7202

1/4W Flat Gain Digital Variable Gain Amplifier

400MHz – 1100MHz

Product Description

The BVA7202 is a digitally controlled variable gain amplifier (DVGA) in a 6mm x 6mm LGA package, with a frequency range of 0.4GHz to 1.1GHz at VDD of 5.0V.

The BVA7202 is a high performance and high dynamic range makes it ideally suited for use in LTE/3G/5G wireless infrastructure and other high performance wireless RF applications.

The BVA7202 is an integration of a high performance digital 6-bit attenuator (DSA) that provides a 31.5dB attenuation range in 0.5dB steps and two amplifiers. Two amplifiers in BVA7202 provide high OIP3 and OP1dB.

The BVA7202 supports digital control interface for serial programming of the Step attenuator (DSA) and has a power down feature for power savings with Power Down (P/D) mode.

This device is packaged in a 28-pin LGA, 6mm x 6mm x 0.95mm with 50Ω single-ended RF input and RF output impedances for ease of integration into the signal-path.

The BVA7202 does not require blocking capacitors. If DC is presented at the RF port, add a blocking capacitor.

Figure 1. Functional Block Diagram

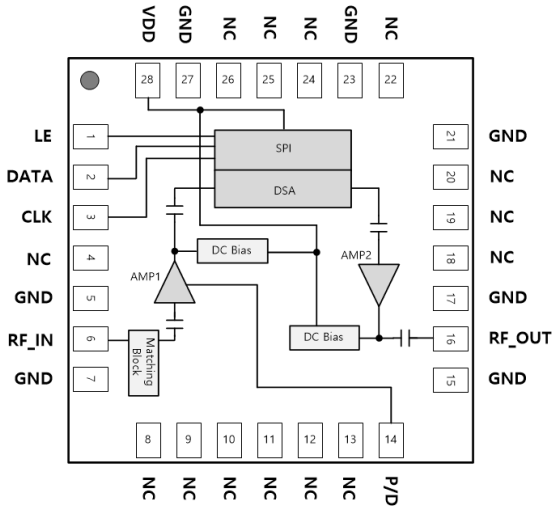


Figure 2. Package Type

28-pin 6mm x 6mm x 0.95mm LGA

Device Features

- 28-pin 6mm x 6mm x 0.95mm LGA Package
- Integrated AMP1 + DSA + AMP2
- A Single Voltage Supply : +5.0V / 165mA
- 0.4 - 1.1GHz Frequency Range
- 33.9dB Gain @ 0.8GHz
- Gain Flatness
  Under 0.8dB @ 700MBW (0.4 - 1.1GHz)
- 4.5dB Noise Figure @ 0.8GHz (Max gain)
- 23.7dBm Output P1dB @ 0.8GHz (Max gain)
- High Output IP3
  40.5dBm @ 0.8GHz, ATT 0dB (Max gain)
  39.5dBm @ 0.8GHz, ATT 6dB
  32.8dBm @ 0.8GHz, ATT 20dB
- Attenuation: 0 - 31.5dB / 0.5 dB step
- Glitch-less attenuation state during transitions
- High attenuation accuracy
  ±(0.25dB + 5% x ATT. Setting) @ 0.4 - 1.1GHz
- Serial Programming Interface only
- Power Down Mode (P/D)
- Lead-free/RoHS2-compliant SiP LGA SMT Package

Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

Table 1. Electrical Specifications

Typical Performance Data @ 25°C and VDD = 5.0V, ATT = 0dB state (Max. gain) unless otherwise noted.
(De-embedded PCB and connector Loss)

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			0.4		1.1	GHz
Gain		ATT = 0dB @ 0.8GHz	31.4	33.9	36.4	dB
Gain Flatness		0.7GHz to 1.1GHz		0.8		dBpp
		0.4GHz to 1.1GHz		0.8		dBpp
Attenuation Control range		0.5dB step		0 - 31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy		Any bit or bit combination	- (0.25 +5% of ATT. setting)		+ (0.25 +5% of ATT. setting)	dB
Return loss	**Input Return Loss**	Attenuation = 0dB		15		dB
	Output Return Loss			15		
Output Power for 1dB Compression		ATT = 0dB , @ 0.8GHz		23.5		dBm
Output Third Order Intercept Point		ATT = 0dB, @ 0.8GHz Pout= 7dBm/tone △f=1MHz	36	40.5		dBm
		ATT= 20dB, @ 0.8GHz Pin= -20dBm/tone △f=1MHz		32.8		dBm
Noise Figure		ATT = 0dB, @ 1.9GHz		4.5		dB
DSA Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Power Down (P/D) Switching time		50% CTRL to 90% or 10% RF		150		ns
Supply voltage		AMP1, DSA, AMP2	4.75	5	5.25	V
Supply Current		AMP1, DSA, AMP2	132	165	198	mA
DSA control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.63	V
P/D control Voltage		P/D high (AMP1 Off)	1.17		5	V
		P/D low (AMP1 On)	0		0.63	V
		Current(AMP2) @ P/D High (AMP1 off)		85		mA
Impedance				50		Ω

Table 2. Typical RF Performance[1]

Parameter	Frequency					Unit
Frequency	**0.4**	**0.7**	**0.8**	**0.9**	**1.1**	**GHz**
Gain	33.4	33.9	33.9	33.9	33.3	dB
S11	-17.6	-18.9	-18	-16.5	-14.7	dB
S22	-17.3	-27.7	-30.7	-19.7	-12.5	dB
OIP3[2] (Max Gain, ATT=0dB)	39.5	41	40.5	40	38.8	dBm
OIP3[2] (ATT=20dB)	32.1	32.8	32.8	32.6	32	dBm
OP1dB	24	23.8	23.7	23.5	23.3	dBm
N.F (Max Gain, ATT=0dB)	4.8	4.6	4.6	4.6	4.7	dB
N.F (ATT=20dB)	11.1	11.1	11.1	11.3	11.4	dB

[1] Device performance measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. measure on Evaluation Board De-embedded PCB and Connector Loss.

[2] OIP3 measured with two tones at an output of +7dBm(ATT=0dB) and –3dBm(ATT=20dB) per tone separated by 1MHz.

Table 3. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage (VDD)	-0.3		5.5	V
Digital Input voltage	-0.3		3.6	V
Maximum Input power			+15	dBm
Storage Temperature	-55		+150	℃
Junction Temperature			+165	℃

[1] Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Unit
Frequency Range	0.4		1.1	GHz
Supply Voltage (VDD)	4.75	5	5.25	V
Operating Temperature	-40		+105	˚C
Thermal Resistance, $R_{TH}(\theta_{JA})$		41.5		˚C/W

[1] Specifications are not guaranteed over all recommended operating conditions.

Programming Option

Programming Mode

The BVA7202 is only operating in Serial Mode.

Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 4 (Serial Interface Timing Diagram) and Table 6 (Serial Interface AC Characteristics).

Power-up Control Settings

The BVA7202 always assumes a specifiable attenuation setting on power-up.

The BVA7202 is set to 30dB Attenuation setting by default on power-up. This attenuation setting is kept on until an initial serial control word is provided.

Table 5. Serial Attenuation word Truth Table[1]

Attenuation Word						Attenuation State
C16	C8	C4	C2	C1	C0.5	
0	0	0	0	0	0	Reference Loss
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1 dB
0	0	0	1	0	0	2 dB
0	0	1	0	0	0	4 dB
0	1	0	0	0	0	8 dB
1	0	0	0	0	0	16 dB
1	1	1	1	1	1	31.5 dB

[1] Not all 64 possible combinations of C0.5–C16 are shown in table.

Figure 3. 6-Bit Attenuator Serial Programming Register Map

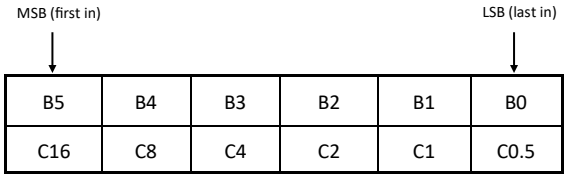


Figure 4. Serial Interface Timing Diagram

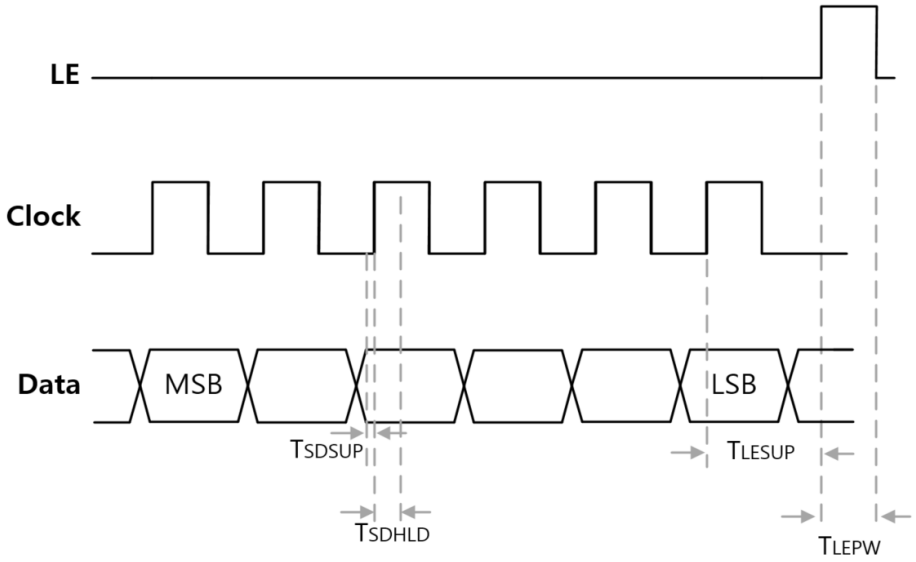


Table 6. Serial Interface AC Characteristics

VDD= 5.0V with DSA only, -40°C ≤ T_A ≤ 105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial data clock frequency[1]		10	MHz
T_{CLKH}	Serial clock HIGH time	30		ns
T_{CLKL}	Serial clock LOW time	30		ns
T_{LESUP}	LE set-up time after last clock rising edge	10		ns
T_{LEPW}	LE minimum pulse width	30		ns
T_{SDSUP}	Serial data setup time before rising edge	10		ns
T_{SDHLD}	Serial data hold time after clock rising edge	10		ns

[1] F_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify F_{CLK} specification

Figure 5. Pin Configuration

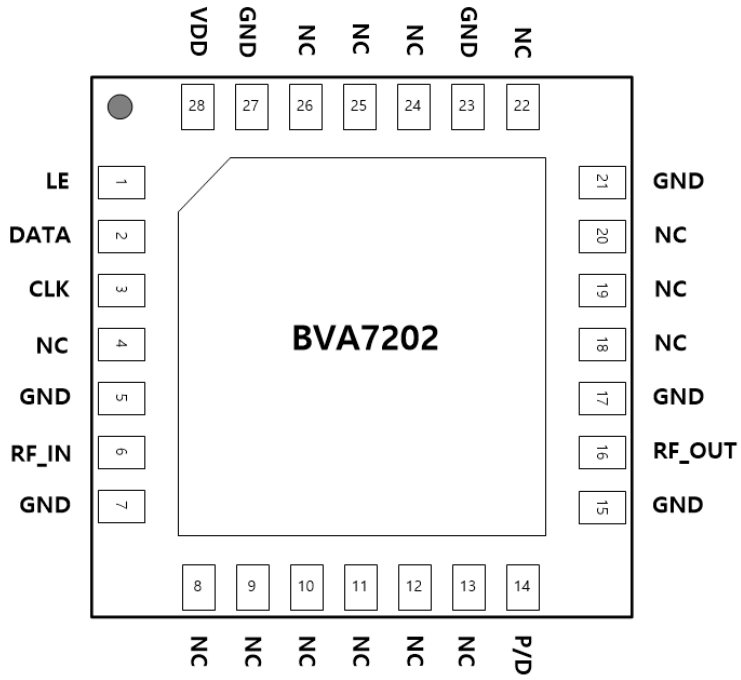


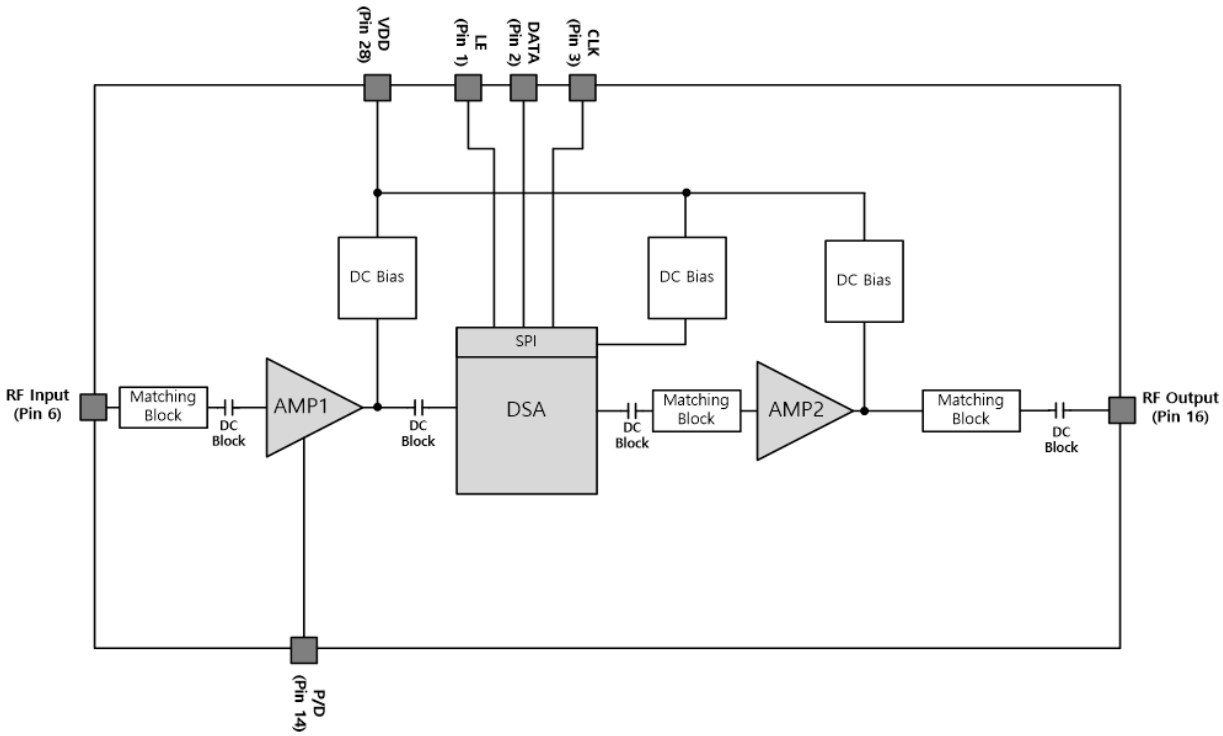
Table 7. Pin Description

Pin	Pin name	Description
5,7,15,17, 21,23,27	GND	RF/DC Ground
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial Clock Input.
6	RF_IN	RF input, matched to 50 ohm. Internally DC blocked.
14	P/D	VDD Power Down control Input. With Logic High(1.17 to 5V), Amplifier is Disabled. With Logic Low (0 to 0.63V), Amplifier is Enabled.
16	RF_OUT	RF output, matched to 50 ohm. Internally DC blocked.
28	VDD	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
4,8-13,18-20, 22,24-26	NC	Doesn't matter how these pins are NC (No Connection) or recommend connect to ground.
Exposed Pad	GND	RF/DC Ground

Figure 6. Internal Function Block Diagram

The BVA7202 is integrated two gain blocks (AMP1, AMP2) and one digital step attenuator (DSA). Additionally, the BVA7202 includes an internal bias circuits and RF Matching to improve the RF performances at 0.4GHz - 1.1GHz.

The block diagram of BVA7202 is shown below.

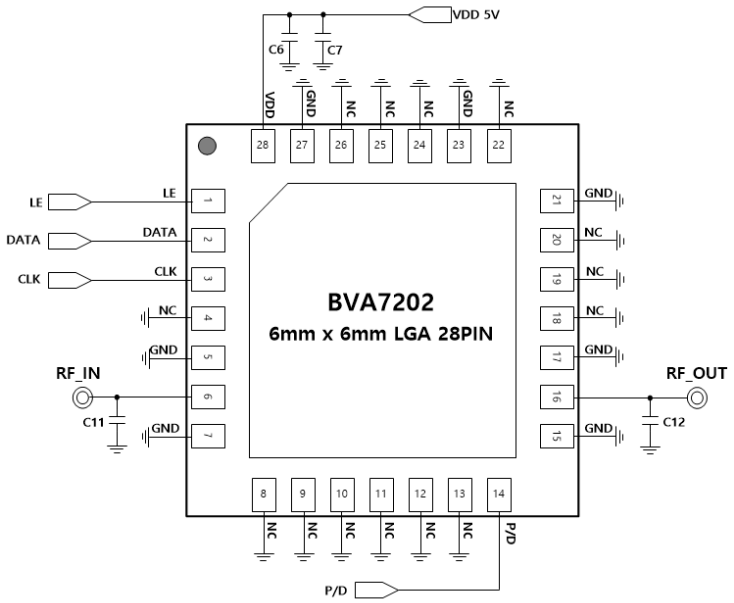


Typical RF Performance - BVA7202 EVK - PCB

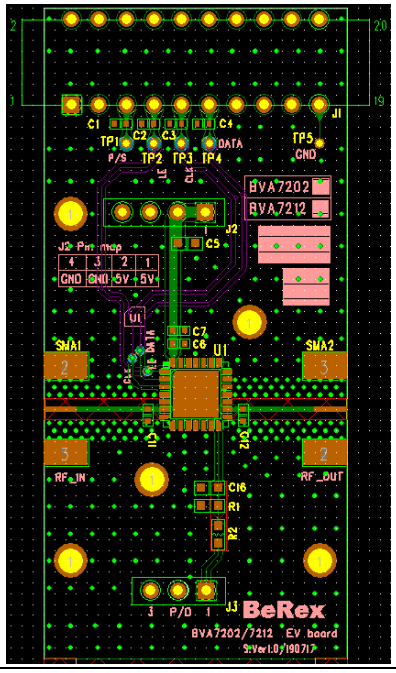
Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Table 8. Application Circuit

Schematic Diagram



BOM			Remark
Ref	Size	Value	
C6	0402	1 nF	
C7	0402	100 nF	
C11	0402	DNI	
C12	0402	DNI	



NOTE

1. J1 Information
   - Pin 5 : Not used. P/S (TP1)
   - Pin 7 : LE (TP2)
   - Pin 9 : CLK (TP3)
   - Pin 11 : DATA (TP4)
   - Pin 19 : GND (TP5)
2. J2 Information
   - Pin 1, 2 : VDD pin
   - Pin 3,4 : GND
3. J3 Information
   - Pin 1 : P/D pin
   - Pin 2, 3 : GND
   - Pin 1 Logic High AMP1 Disabled.
   - Pin 1 Logic Low AMP1 Enabled.

Typical RF Performance - BVA7202 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Table 9. Typical Performance by Temperature[2] : 0.8GHz

Parameter	Typical Values				Units
Temperature	-40	25	85	105	°C
VDD	5	5	5	5	Vdc
Current	163	162	157	154	mA
Gain	34.9	33.9	33.1	32.7	dB
S11	-18.1	-18	-17.8	-17.8	dB
S22	-30.8	-30.7	-29.5	-27.6	dB
OIP3[1]	41.2	40.5	38	37	dBm
OP1dB	24	23.7	23.3	23.2	dBm
Noise Figure	3.9	4.5	5.2	5.4	dB

[1] OIP3 measured with two tones at an output of 7dBm per tone separated by 1MHz.

[2] Above test parameters are measured at Max Gain State (ATT=0dB)

Figure 7. Gain
: Max. Gain, Temp.

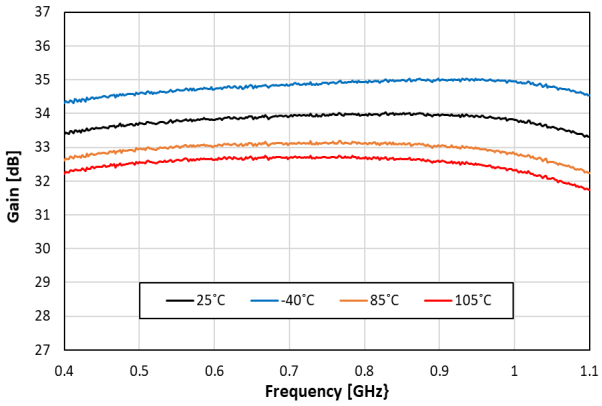


Figure 8. Gain
: Min. Gain, Temp.

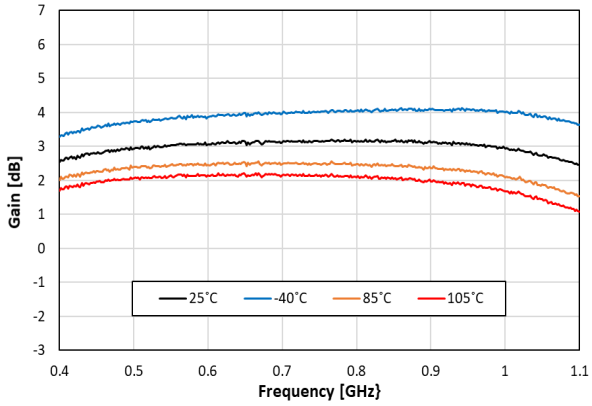


Figure 9. Gain
: Attenuation Setting

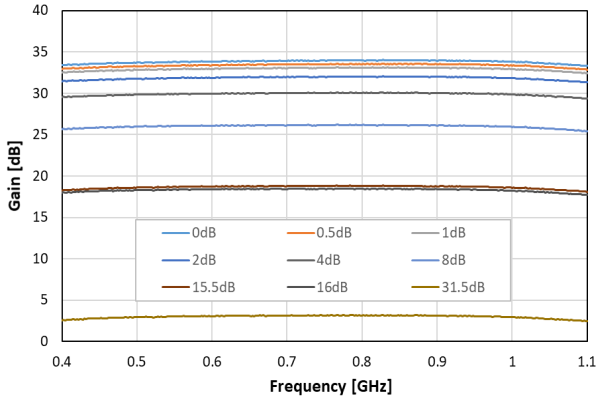
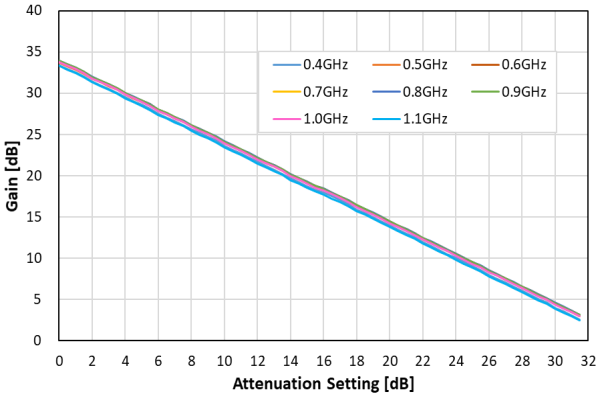


Figure 10. Gain
: Frequency, Attenuation Setting



Typical RF Performance - BVA7202 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 11. Gain

: 0.8GHz, Attenuation Setting, Temp.

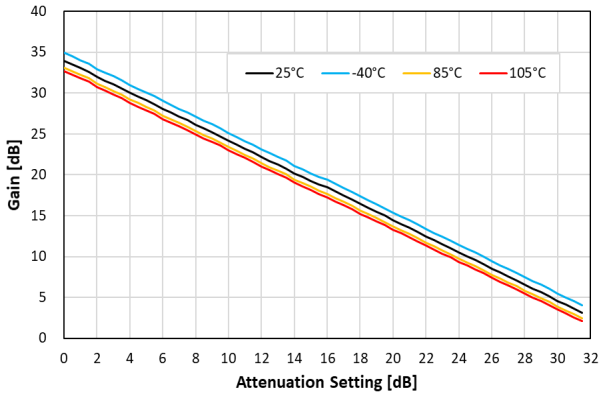


Figure 12. Input Return Loss

: Max. Gain, Temp.

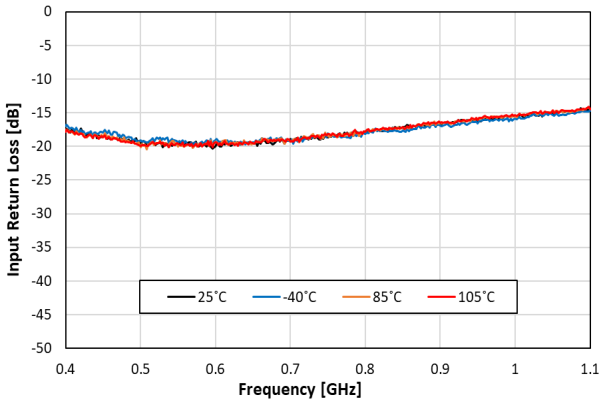


Figure 13. Input Return Loss

: Min. Gain, Temp.

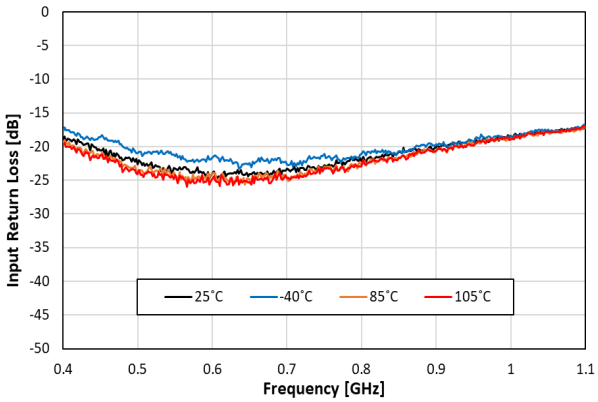


Figure 14. Output Return Loss

: Max. Gain, Temp.

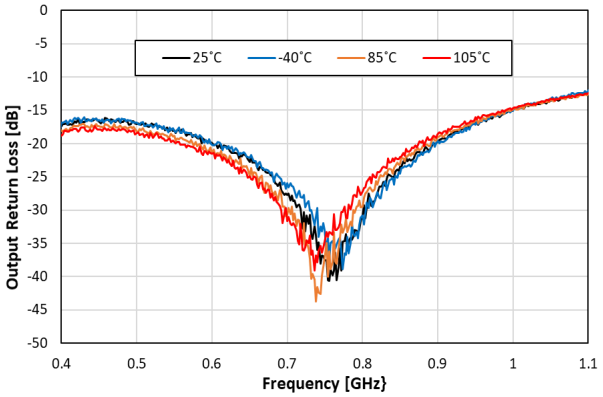
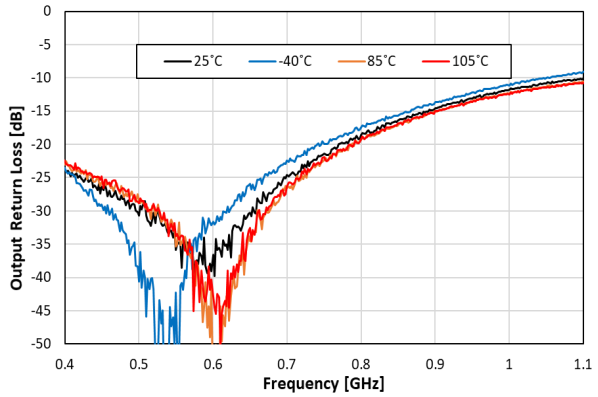


Figure 15. Output Return Loss

: Min. Gain, Temp.



Typical RF Performance - BVA7202 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 16. Attenuation Error
: 0.4GHz, Temp.

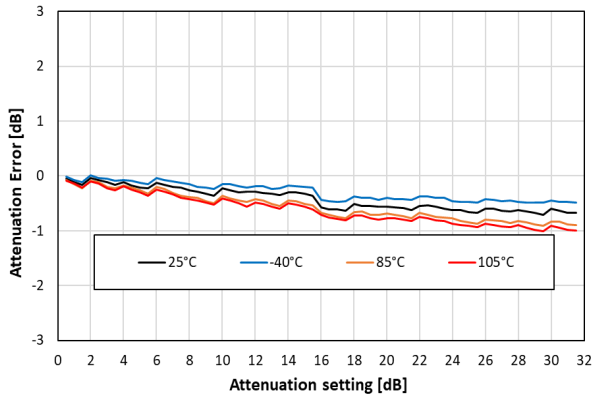


Figure 17. Attenuation Error
: 0.7GHz, Temp.

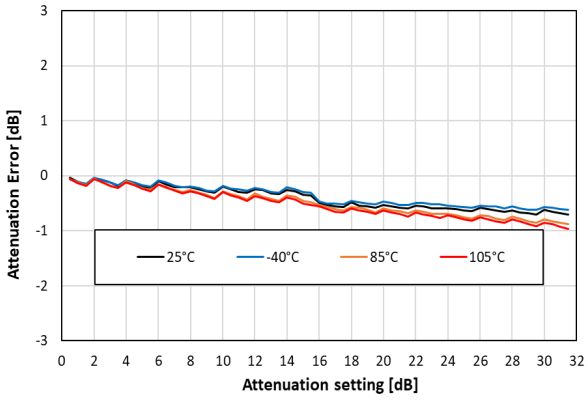


Figure 18. Attenuation Error
: 1.1GHz, Temp

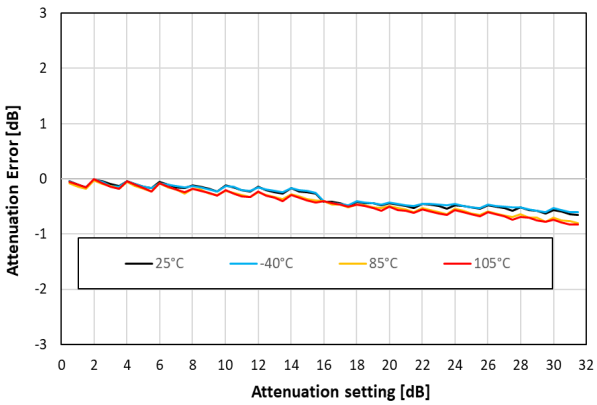
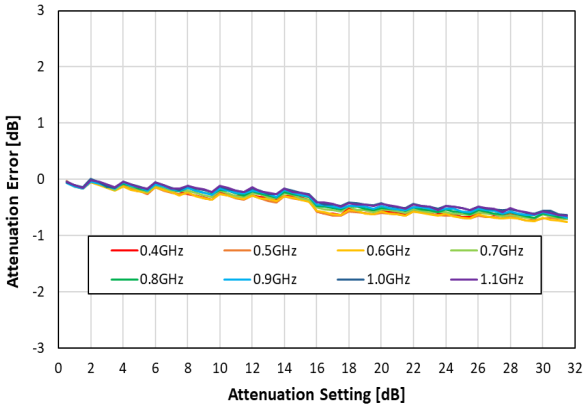


Figure 19. Attenuation Error
: Frequency



Typical RF Performance - BVA7202 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 20. OIP3

: ATT=0dB, Temp, Output=7dBm/tone, 1MHz interval

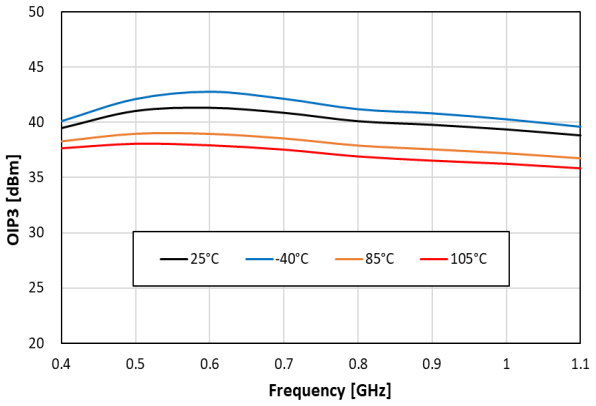


Figure 21. OIP3

: ATT=6dB, Temp, Output=7dBm/tone, 1MHz interval

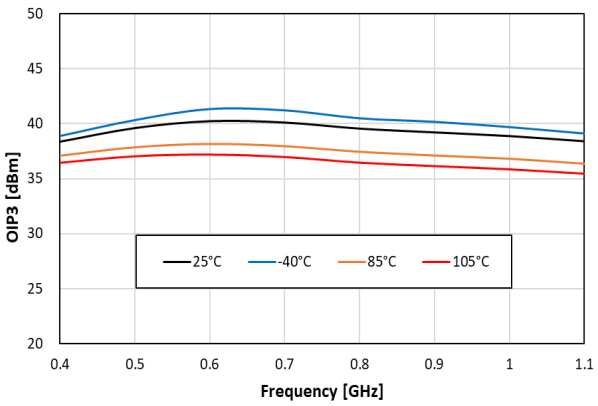


Figure 22. OIP3

: ATT=20dB, Temp, Output=-3dBm/tone, 1MHz interval

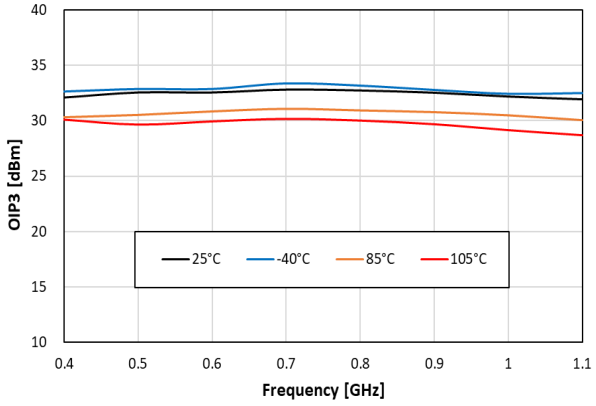


Figure 23. OIP3

: ATT=0dB (Max Gain), Output Power

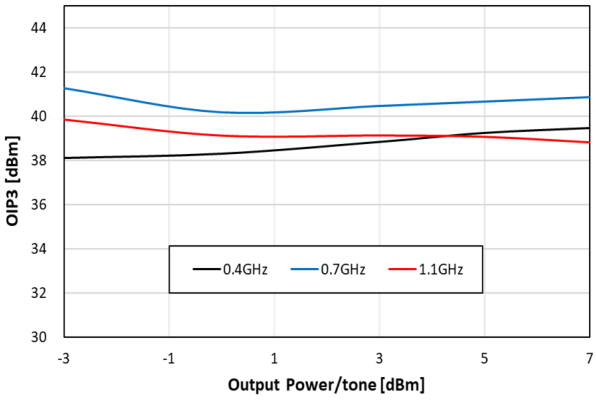


Figure 24. OP1dB

: Attenuation Setting

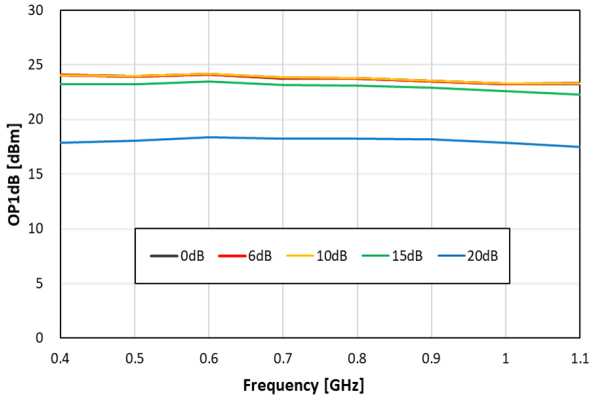
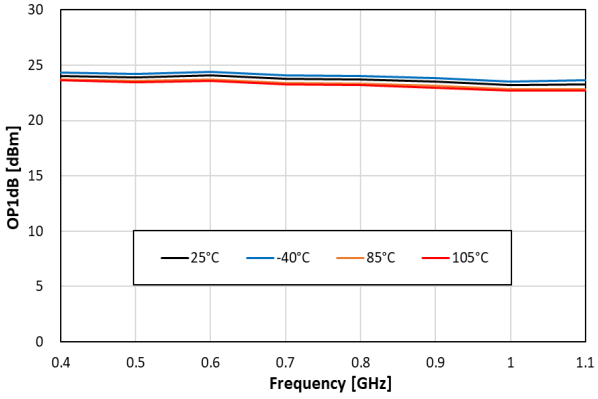


Figure 25. OP1dB

: ATT=0dB(Max Gain), Temp.



Typical RF Performance - BVA7202 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 26. OP1dB

: ATT=10dB, Temp.

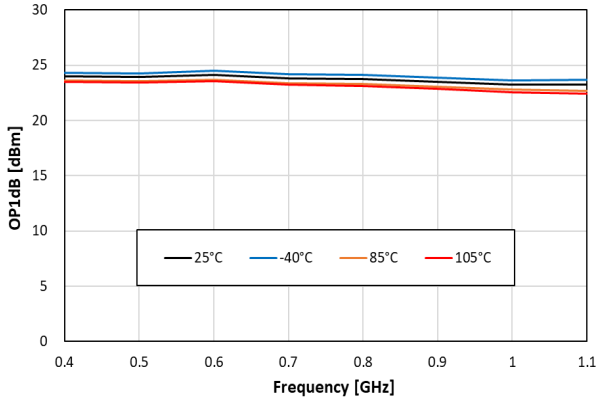


Figure 27. OP1dB

: ATT=20dB, Temp

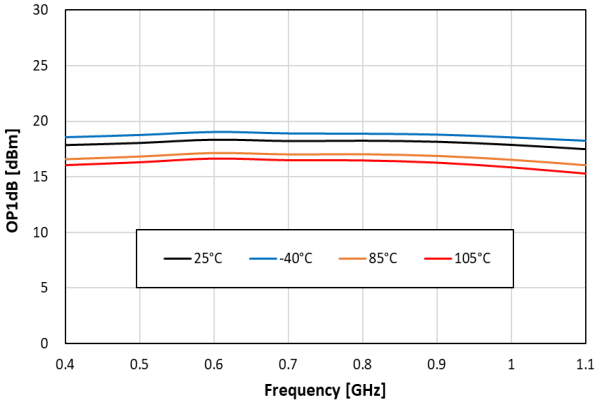


Figure 28. NF

: ATT. Setting

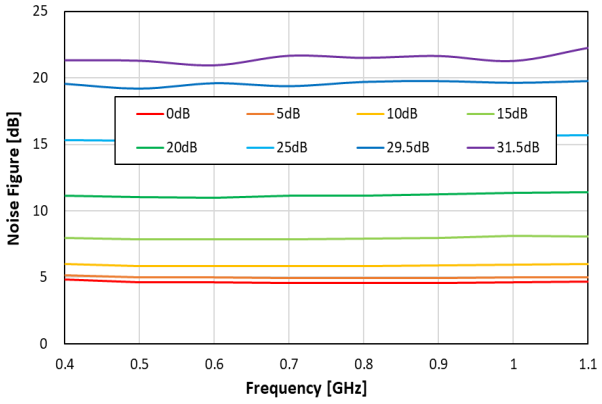


Figure 29. NF

: ATT=0 (Max Gain), Temp.

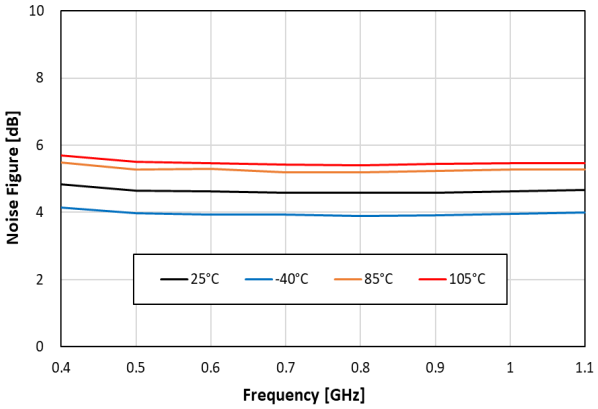


Figure 30. NF

: ATT=15dB, Temp.

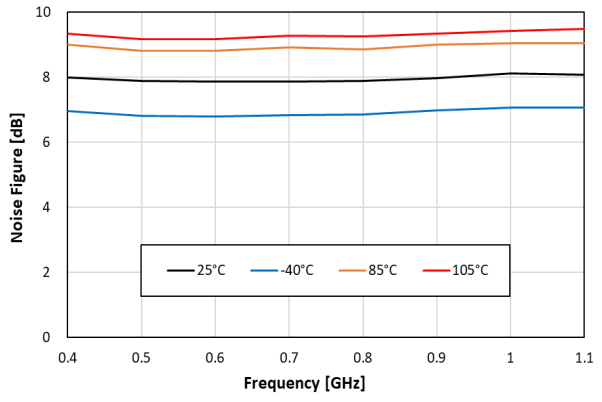
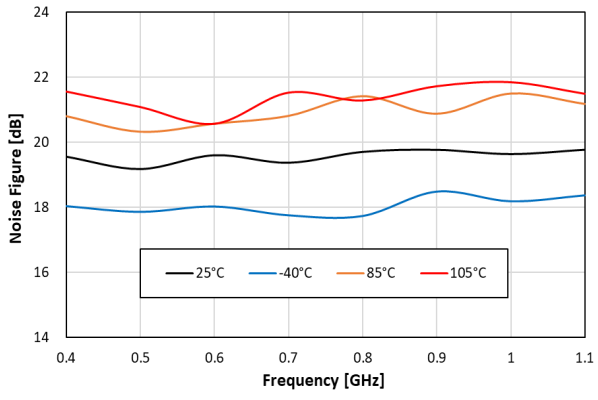


Figure 31. NF

: ATT=29.5dB, Temp.



Typical RF Performance - BVA7202 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 32. Power On/Off Time

: Rising Time (Control 50% to RF 90%)

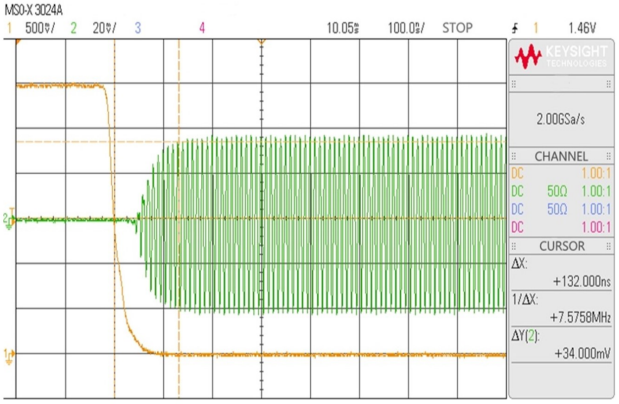


Figure 33. Power On/Off Time

: Falling Time (Control 50% to RF 10%)

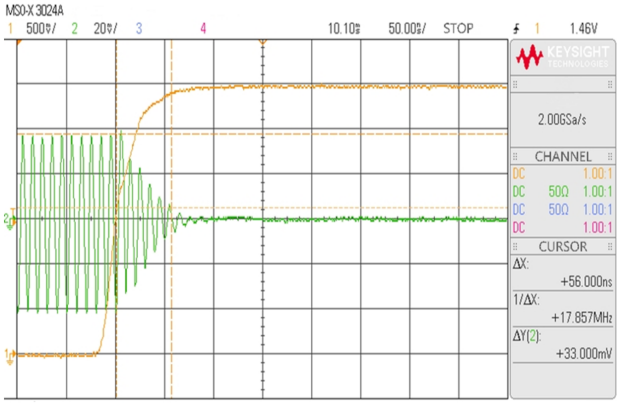


Figure 34. ACLR

: @778MHz, LTE PAR 9.6dB 20MBW 2FA, 50dBc

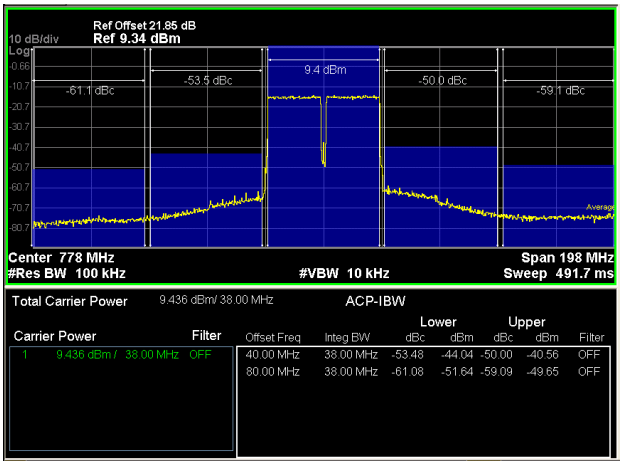


Figure 35. ACLR

: @880MHz, LTE PAR 9.6dB 20MBW, 50dBc

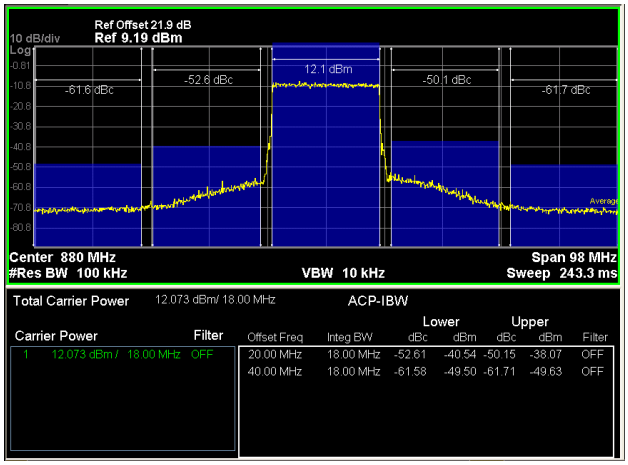


Figure 36. Evaluation Board Schematic

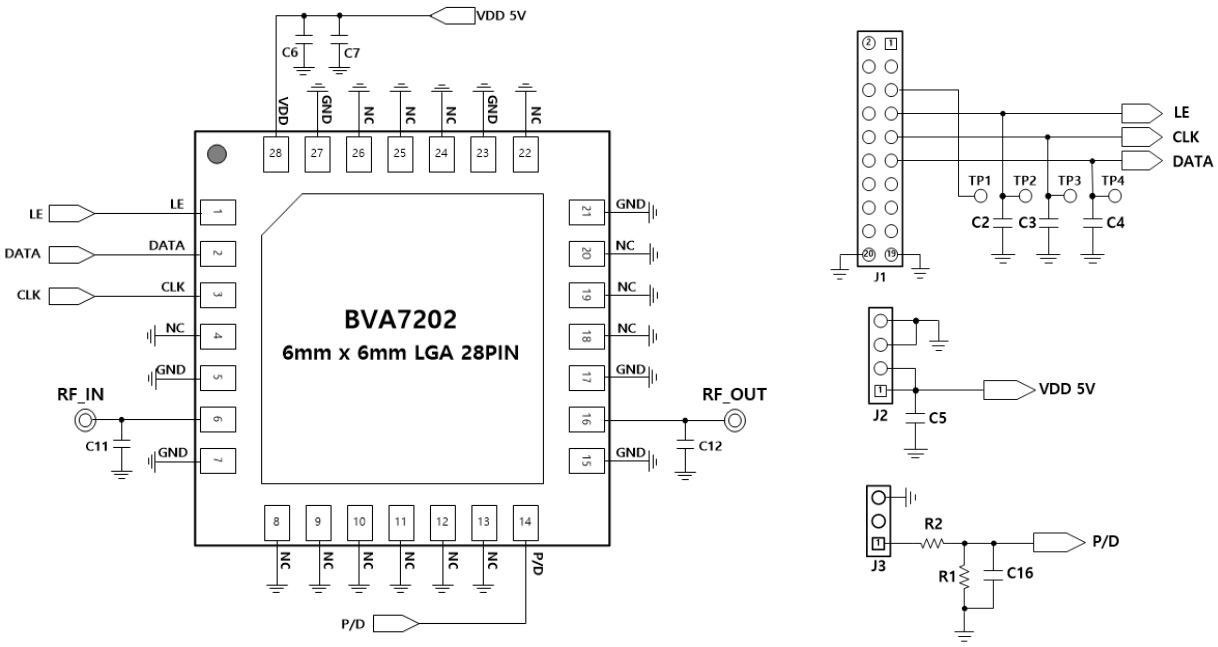
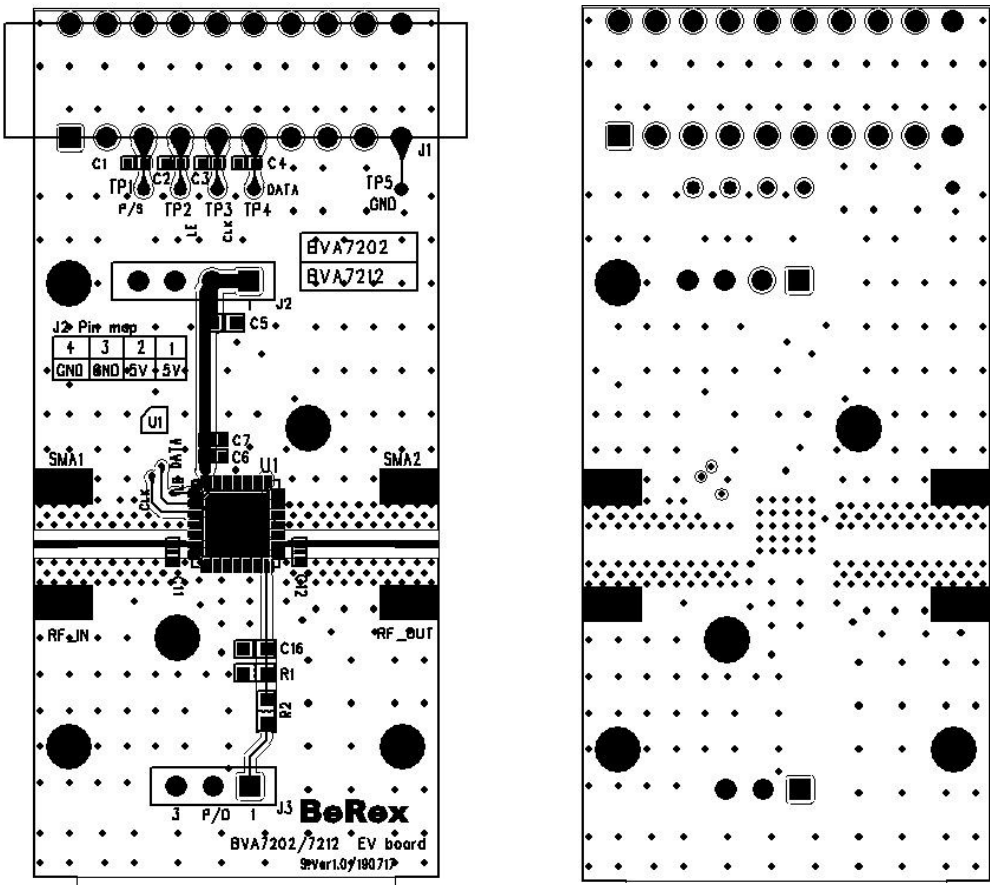


Table 10. Bill of material

No.	Ref. Number	Value	Description	Remark
1	R2	0 ohm	Resistor, 0603, Chip, 5%	Walsin
2	C6	1000 pF	1 nF ±5%, 16V, X7R Ceramic Capacitor (0402)	Murata
3	C7	100 nF	100 nF ±10%, 16V, X7R Ceramic Capacitor (0402)	Murata
4	SMA1	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
5	SMA2	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
6	J1	20pin	Receptacle Connector, 5-532955-3, Female, RT/A Dual	AMP Connectors
7	J2	4pin	2.54mm Breakaway Male Header, Straight, Black	
8	J3	3pin	2.54mm Breakaway Male Header, Straight, Black	
9	R1,C1,C2,C3,C4, C5,C11,C12,C16	DNI		

RF Input was matched by Inductor internally. So that it needs DC Blocking Capacitors when DC voltage is presented at RF input port.

Figure 37. Evaluation Board Layout



[Top View] [Bottom View]

Figure 38. Evaluation Board PCB Layer Information

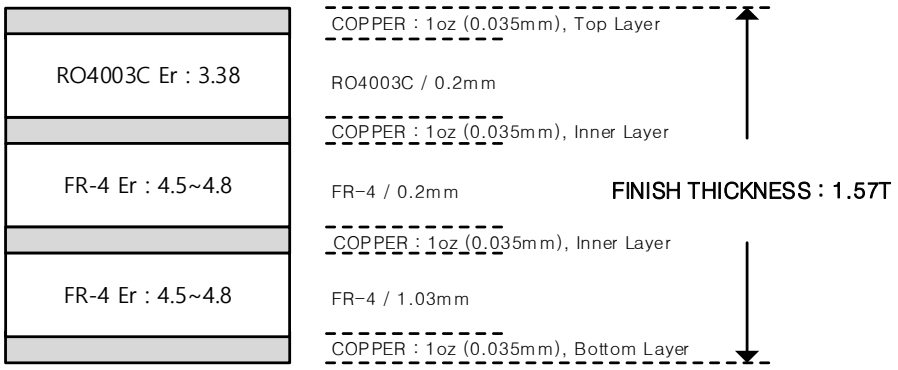


Figure 39. Suggested PCB Land Pattern and PAD Layout

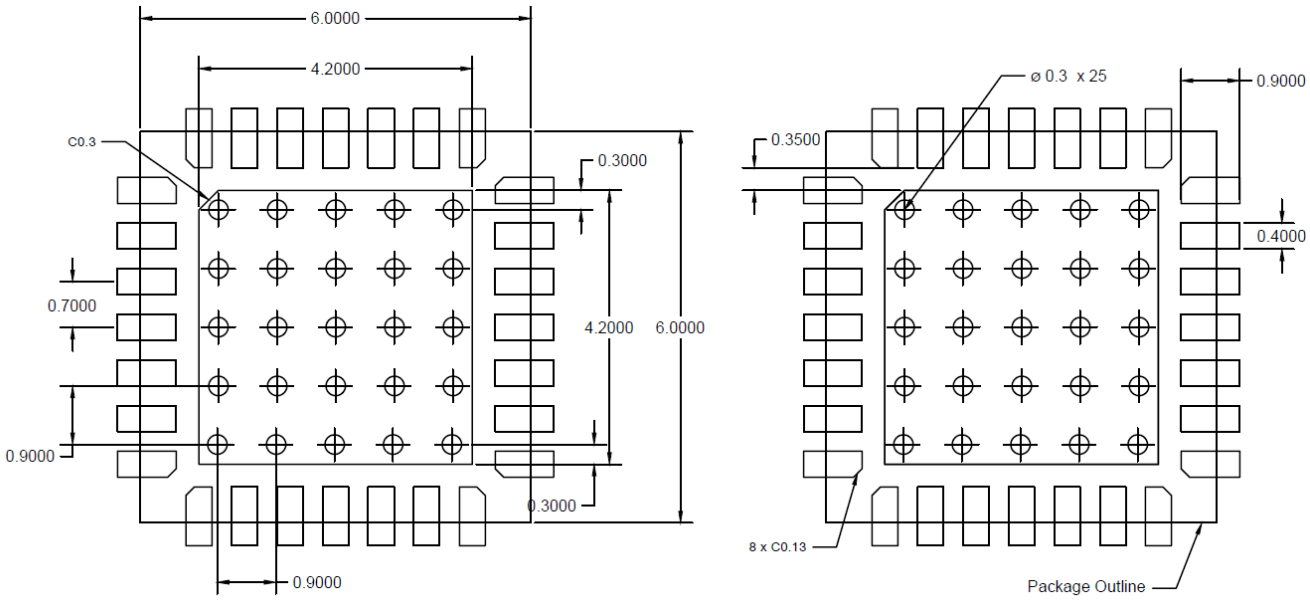
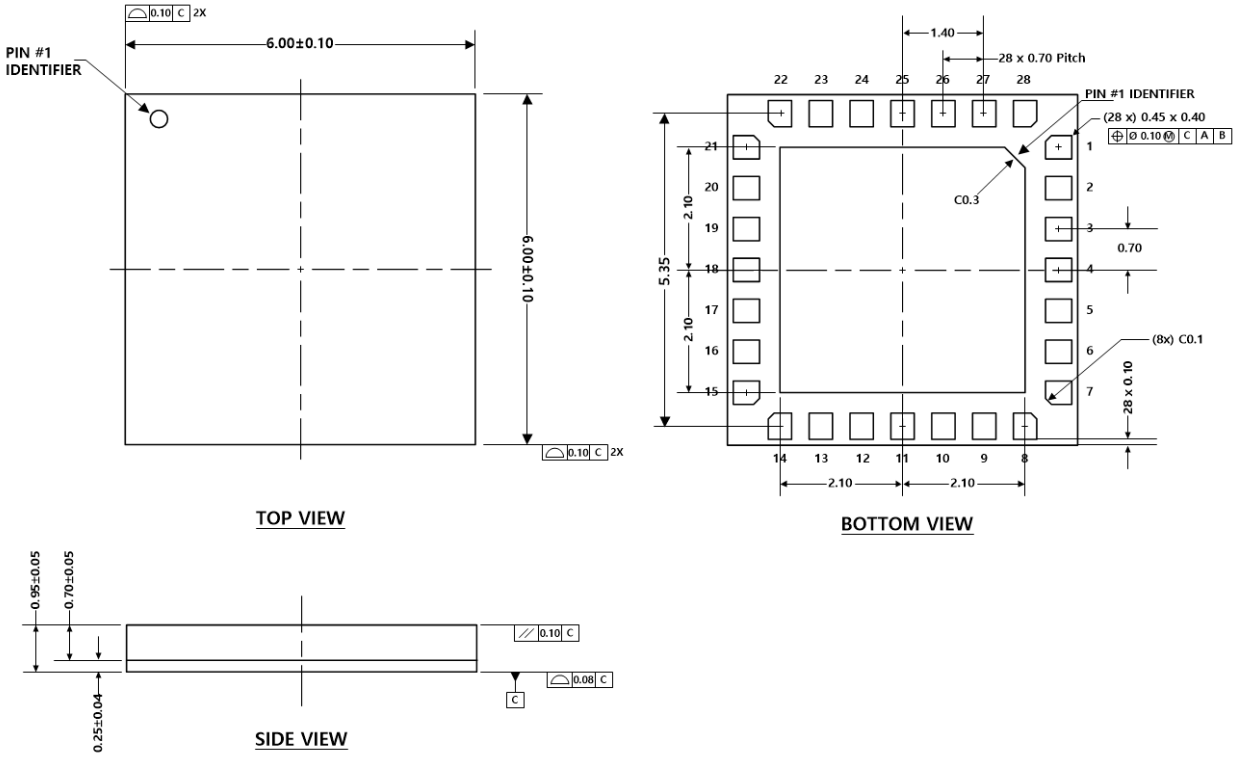


Figure 40. Package Outline Dimension



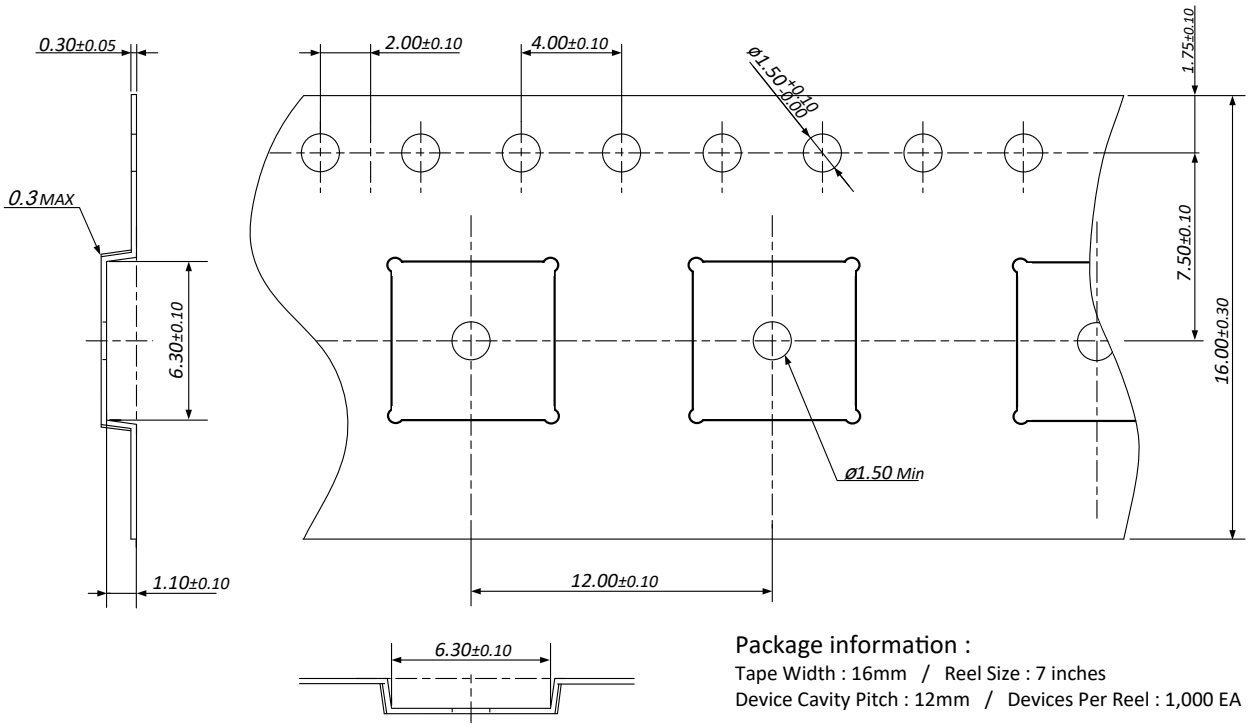
Notes

1. All dimensions are in millimeters. Angles are in degrees
2. Dimensions and tolerance conform with ASME Y14.5M-1994.

Figure 41. Package Marking Information

YY = Year
WW = Working Week
XXX = Wafer Lot Number

Figure 42. Tape and Reel



Package information :

Tape Width : 16mm / Reel Size : 7 inches

Device Cavity Pitch : 12mm / Devices Per Reel : 1,000 EA

Lead Plating Finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating :	Class 1C
Value :	1000V
Test :	Human Body Model (HBM)
Standard :	JEDEC Standard JS-001-2017

ESD Rating :	Class C5
Value :	1000V
Test :	Charged Device Model (CDM)
Standard :	JEDEC Standard JESD22-C101F

MSL Rating :	MSL3 at +260°C convection reflow
Standard :	JEDEC Standard J-STD-020

Caution : ESD Sensitive

Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling the device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO GAGE Code :

2	N	9	6	F