BVA7242N

Flat Gain Digital Variable Gain Amplifier

3000MHz – 4200MHz

Product Description

The BVA7242N is a digitally controlled variable gain amplifier (DVGA) in a 6mm x 6mm LGA package, with a frequency range of 3GHz to 4.2GHz at VDD of 5.0V.

BVA7242N is a high performance and high dynamic range makes it ideally suited for use in 5G/LTE wireless infrastructure and other high performance wireless RF applications.

The BVA7242N is an integration of a high performance digital 7bit step attenuator (DSA) that provides a 31.75 dB attenuation range in 0.25 dB steps and two amplifiers. Two amplifiers in BVA7242N provide high ACP and P1dB.

The BVA7242N digital control interface supports serial programming of the Step attenuator (DSA) and has a power down feature for power savings with Power Down (P/D) mode.

Implementation requires only a few external components, such as matching capacitors on input and output pins. (No need DC Blocking Capacitors when DC voltage is not presented.)

Figure 1. Functional Block Diagram

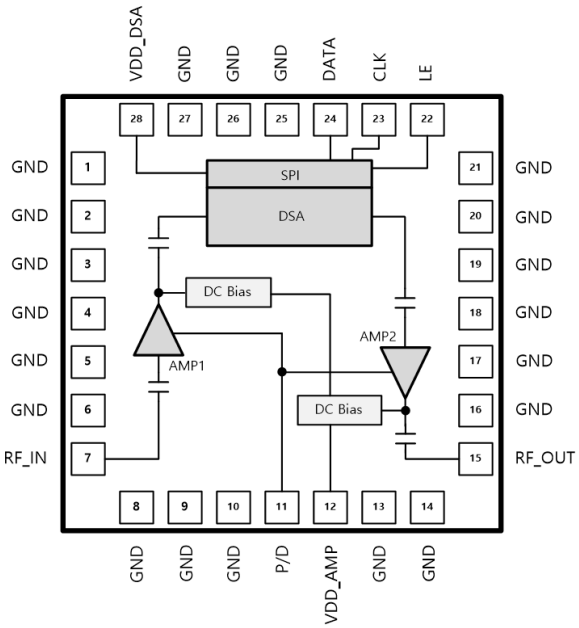


Figure 2. Package Type

28-pin 6mm x 6 mmx 0.95mm LGA

Device Features

- 28-pin 6mm x 6mm x 0.95mm LGA Package
- Integrated AMP1 + DSA + AMP2
- A Single Voltage Supply : +5.0V / 165mA
- 3.0 - 4.2GHz Frequency Range
- 33.5dB Gain @ 3.6GHz
- Gain Flatness
  Under 1dB @ 800MBW (3.2 - 4GHz)
- 1.9dB Noise Figure @ 3.6GHz, max gain setting
- 19.6dBm Output P1dB @ 3.6GHz
- High Output IP3
  37.5dBm @3.6GHz, Atten 0dB (Max gain)
  33dBm @3.6GHz, Atten 20dB
- Attenuation: 0 - 31.75 dB / 0.25 dB step
- Glitch-less attenuation state during transitions
- High attenuation accuracy
  ±(0.25dB + 5% x ATT. Setting) @ 3.2-4.2GHz
- Serial Programming Interface only
- Power Down Mode (P/D)
- Lead-free/RoHS2-compliant SiP LGA SMT Package

Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Table 1. Electrical Specifications

Typical Performance Data @ 25°C and VDD = 5.0V, ATT=0dB state (Max. gain) unless otherwise noted.
(De-embedded PCB and connector Loss)

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			3		4.2	GHz
Gain		Attenuation = 0dB, @ 3.6GHz	31	33.5	36	dB
Gain Flatness		3.2GHz to 4.2GHz		1	1.5	dBpp
		3GHz to 4.2GHz		1.5	2	dBpp
Attenuation Control range		0.25dB step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	**3.2GHz to 4GHz**	Any bit or bit combination	- (0.25 +5% of ATT. setting)		+ (0.25 +5% of ATT. setting)	dB
	3GHz to 4.2GHz	Any bit or bit combination	- (0.5 +6% of ATT. setting)		+ (0.5 +6% of ATT. setting)	dB
Return loss	**Input Return Loss**	Attenuation = 0dB		15		dB
	Output Return Loss			10		
Output Power for 1dB Compression		Attenuation = 0dB , @ 3.6GHz		19.6		dBm
Output Third Order Intercept Point		Attenuation = 0dB, @ 3.6GHz Pout= -3dBm/tone △f=100MHz	34	37.5		dBm
		Attenuation = 20dB, @ 3.6GHz Pout= -3dBm/tone △f=100MHz.		33		dBm
Noise Figure		Attenuation = 0dB, @ 3.6GHz		1.9		dB
DSA Switching time		50% CTRL to 90% or 10% RF		275		ns
Power Down (P/D) Switching time		50% CTRL to 90% or 10% RF		150		ns
Supply voltage		VDD_DSA	3.3	5	5.5	V
		VDD_AMP	3.3	5	5.25	V
Supply Current		AMP1+DSA+AMP2	135	165	195	mA
Control Interface		Serial mode		8		Bit
DSA control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
P/D control Voltage		P/D high (Amp Off)	0.8		5	V
		P/D low (Amp On)	0		0.5	V
Impedance				50		Ω

Specifications and information are subject to change without notice.
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Table 2. Typical RF Performance[1]

Parameter	Frequency					Unit
Frequency	**3**	**3.2**	**3.6**	**4**	**4.2**	**GHz**
Gain	32.3	33.2	33.5	32.9	32	dB
S11	-9.4	-13.5	-21.9	-24.0	-21.3	dB
S22	-5.8	-8.2	-16.9	-16.4	-11.2	dB
OIP3[2] (Max Gain, ATT=0dB)	36.9	37.2	37.5	37.5	35.9	dBm
OIP3[2] (ATT=20dB)	32.1	33.1	33	31.7	30	dBm
OP1dB	19.4	19.5	19.6	19.2	18.9	dBm
N.F (Max Gain, ATT=0dB)	1.8	1.8	1.9	1.9	2.2	dB
N.F (ATT=20dB)	7	6.9	7.1	7.8	8.4	dB

[1] Device performance measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. measure on Evaluation Board De-embedded PCB and Connector Loss.

[2] OIP3 measured with two tones at an output of -3dBm per tone separated by 100MHz.

Table 3. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage (VDD)	-0.3		5.5	V
Supply Current			380	mA
Digital input voltage	-0.3		3.6	V
Maximum input power			+10	dBm
Storage Temperature	-55		+150	℃
Junction Temperature			+165	℃

[1] Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Unit
Frequency Range	3		4.2	GHz
Supply Voltage (VDD)	4.75	5	5.25	V
Operating Temperature	-40		+105	˚C
$R_{TH}(\theta_{JC})$		26		˚C/W

[1] Specifications are not guaranteed over all recommended operating conditions

Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Programming Option

Programming Mode

The BVA7242N is only operating in Serial Mode.

Serial Interface

The Serial interface is an 8-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The 8-bits make up the Attenuation Word that controls the DSA. Figure 4 illustrates an example timing diagram for a programming state.

The Serial interface is controlled by using three CMOS compatible signals: SI (DATA), Clock (CLK) and LE. The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Attenuation Word truth table is listed in Table 5. A programming example of the serial register is illustrated in Figure 3. The Serial timing diagram is illustrated in Figure 4.

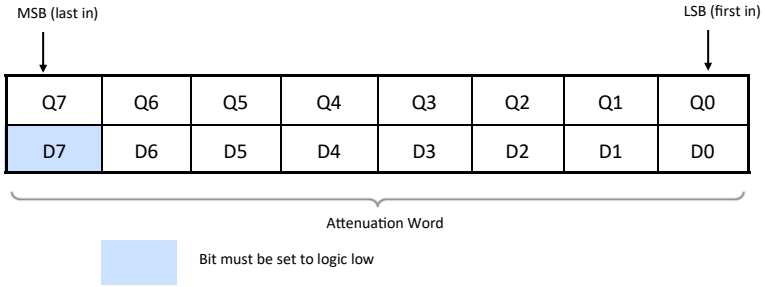
Table 5. Serial Attenuation word Truth Table

Attenuation Word								Attenuation setting
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Max. Gain
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Power-up Control Settings

The BVA7242N will be always initialized to the max. attenuation setting (Atten=31.75dB) on power-up sequence and will remain at the max. attenuation setting until user latches the next programming word.

Figure 3. Serial Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 12.5dB state;

4 x 12.5 = 50
50 → 00110010

Serial Input : 00110010

Glitch-less Attenuation State Transitions

The BVA7242N features a novel architecture to provide the best-in-class glitch-less transition behavior when changing attenuation states. When RF input power is applied, the output power spikes are greatly reduced (≤0.3 dB) during attenuation state changes when comparing to previous generations of DSAs.

Specifications and information are subject to change without notice.
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Figure 4. Serial Interface Timing Diagram

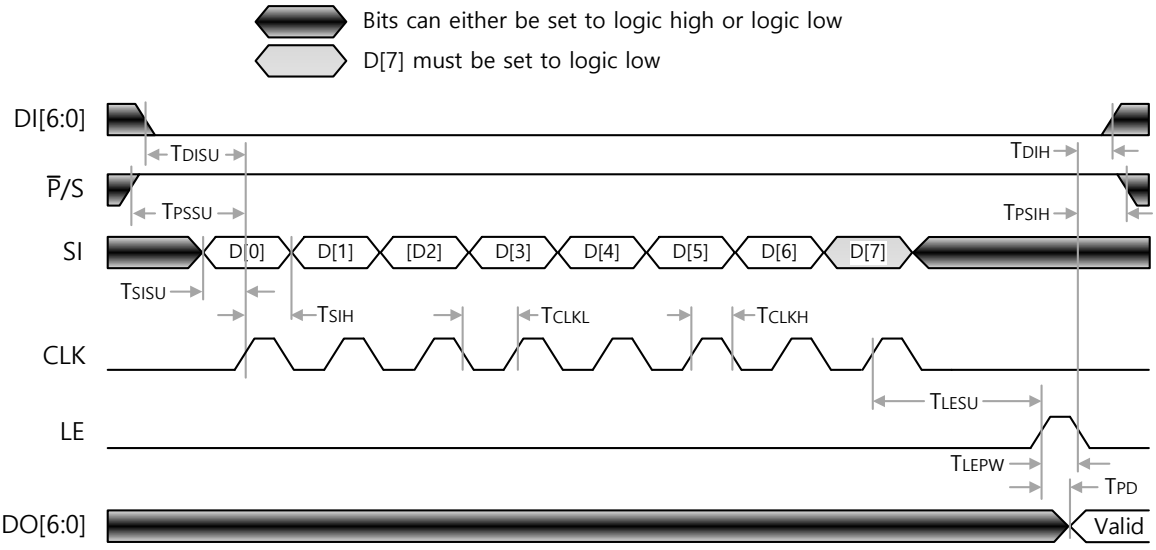


Table 6. Serial Interface AC Characteristics

VDD = 5.0V with DSA only, -40°C ≤ TA ≤ 105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial data clock frequency		10	MHz
T_{CLKH}	Serial clock HIGH time	30		ns
T_{CLKL}	Serial clock LOW time	30		ns
T_{LESU}	Last Serial clock rising edge setup time to Latch Enable rising edge	10		ns
T_{LEPW}	Latch Enable minimum pulse width	30		ns
T_{SISU}	Serial data setup time	10		ns
T_{SIH}	Serial data hold time	10		ns
T_{DISU}	Parallel data setup time	100		ns
T_{DIH}	Parallel data hold time	100		ns
T_{PSSU}	Parallel / Serial setup time	100		ns
T_{PSIH}	Parallel / Serial hold time	100		ns
T_{ASU}	Address setup time	100		ns
T_{AH}	Address hold time	100		ns
T_{PD}	Digital register delay (internal)		10	ns

Specifications and information are subject to change without notice.
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Figure 5. Pin Configuration

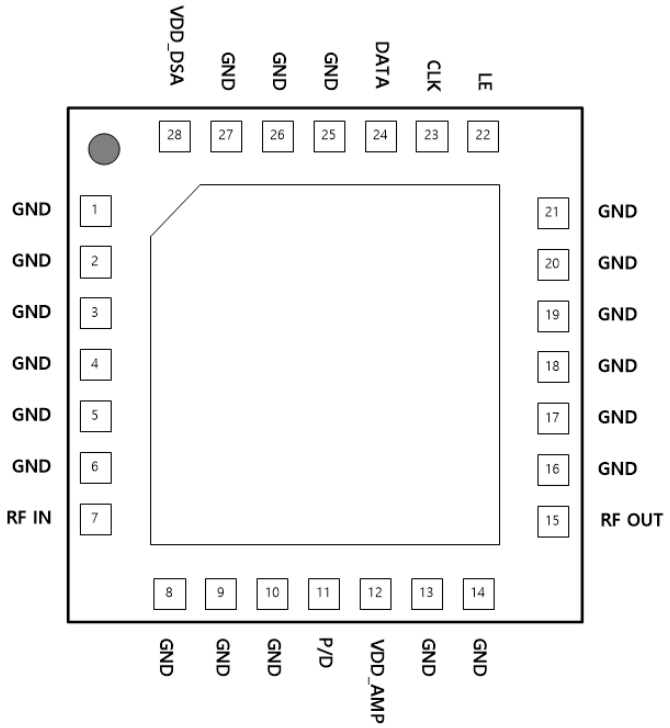


Table 7. Pin Description

Pin	Pin name	Description
1-6, 8-10, 13-14, 16-21, 25-27	GND	RF/DC Ground
7	RF IN	RF Input, matched to 50 ohm. Internally DC blocked.
11	P/D	VDD Power Down control Input. With Logic High(0.8 to 5V), Amplifier is Disabled. With Logic Low(0 to 0.5V), Amplifier is Enabled.
12	VDD_AMP	Supply Voltage to Amplifier (AMP1 and AMP2). This pin is connected internally to bypass capacitors followed by inductor inside the module.
15	RF OUT	RF output, matched to 50 ohm. Internally DC blocked.
22	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
23	CLK	Serial Clock Input.
24	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
28	VDD_DSA	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
Exposed Pad	GND	RF/DC Ground

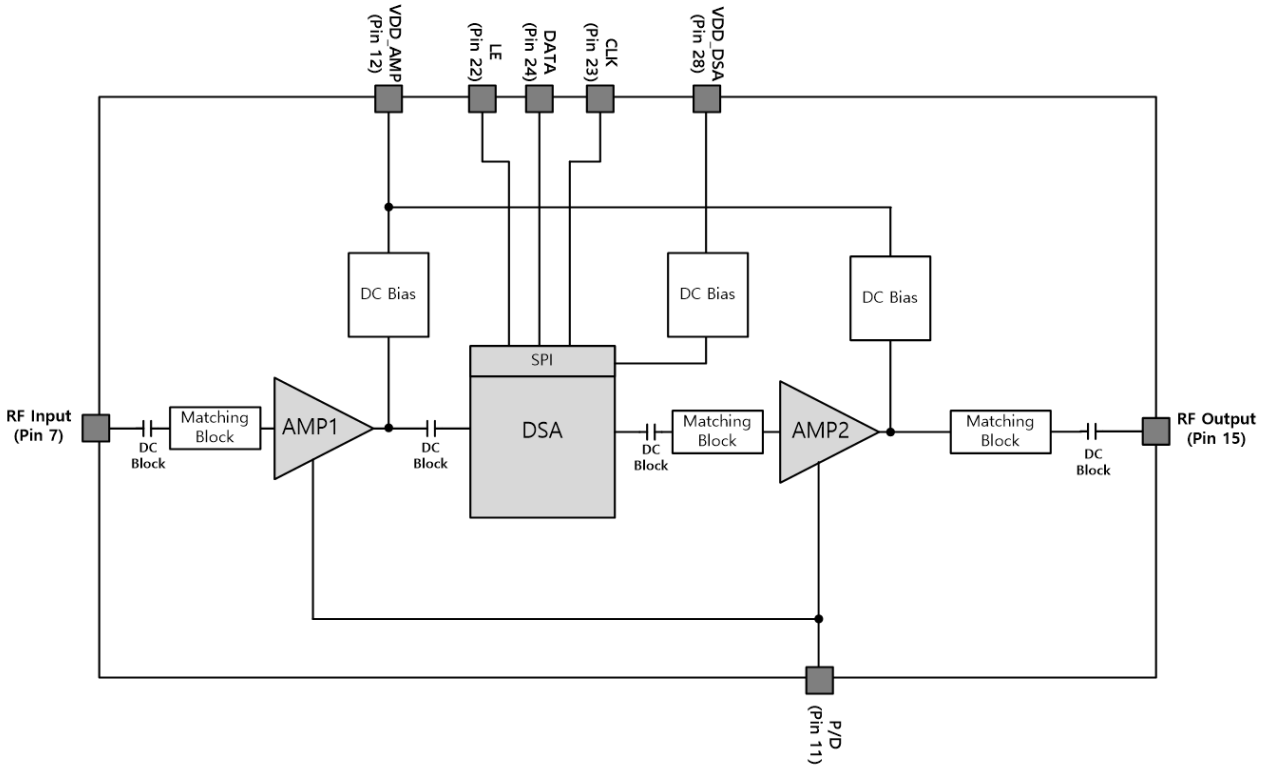
Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Figure 6. Internal Function Block Diagram

The BVA7242N is integrated two gain blocks (AMP1, AMP2) and one digital step attenuator (DSA) . Additionally, the BVA7242N includes an internal bias circuits and RF Matching to improve the RF performances at 3GHz - 4.2GHz.

The block diagram of BVA7242N is shown below.



Specifications and information are subject to change without notice.

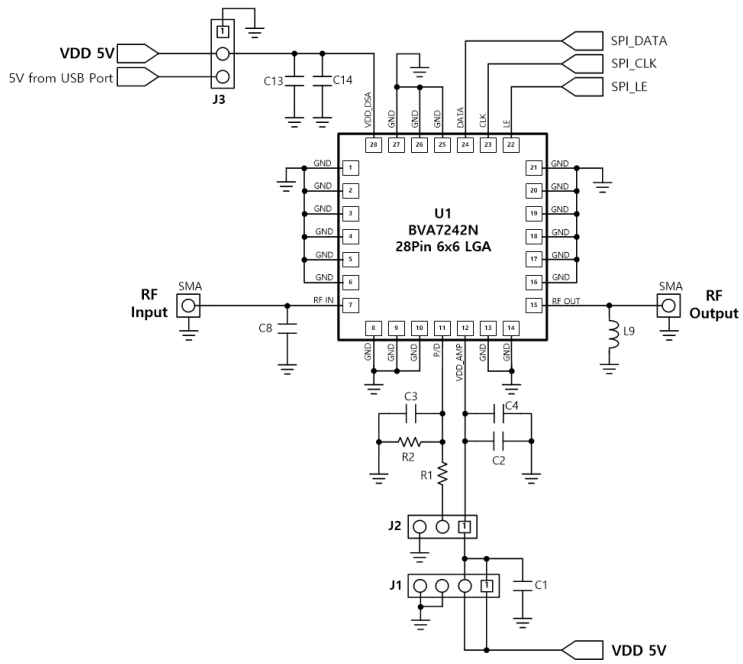
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Typical RF Performance - BVA7242N EVK - PCB

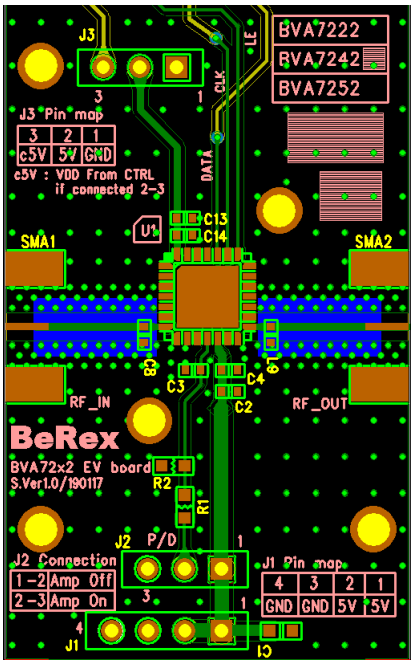
Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted .

Table 8. Application Circuit

Schematic Diagram



BOM			Remark
Ref	Size	Value	
C1	0603	1 uF	
C2	0402	100 nF	
C4	0402	100 pF	
C8	0402	0.4 pF	
L9	0402	4.7 nH	
C13	0402	100 pF	
C14	0402	100 nF	
R1	0603	20 KΩ	
R2	0603	30 KΩ	
C3	0402	NC	



NOTE

1. J1 Information
   - Pin 1, 2 : 5Vdc (VDD Amp)
   - Pin 3, 4 : Ground
2. J2 Information
   - Not connected (Floating) : Amp ON
   - Connected 1-2 : Amp OFF
   - Connected 2-3 : Amp ON
3. J3 Information
   - Not connected (Floating) : VDD DSA OFF
   - Pin 1 : GND
   - Pin 2 : VDD DSA 5Vdc
   - Connected 2-3 : VDD DSA 5V from USB

Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Typical RF Performance - BVA7242N EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Table 9. Typical Performance by Temperature: 3.6GHz

Parameter	Typical Values				Units
Temperature	-40	25	85	105	°C
VDD	5	5	5	5	Vdc
Current	173	165	156	152	mA
Gain	34.8	33.5	32.7	32.3	dB
S11	-25	-21.5	-27.7	-27.5	dB
S22	-16.3	-16.5	-18.1	-17.8	dB
OIP3[1]	37.2	37.5	37.2	37.1	dBm
OP1dB	19.3	19.6	20.1	19.9	dBm
Noise Figure	1.4	1.9	2.3	2.5	dB

[1] OIP3 measured with two tones at an output of –3dBm per tone separated by 100MHz.

[2] Above test parameters are measured at Max Gain State (ATT=0dB)

Figure 7. Gain Flatness

: Max Gain State, Temp.

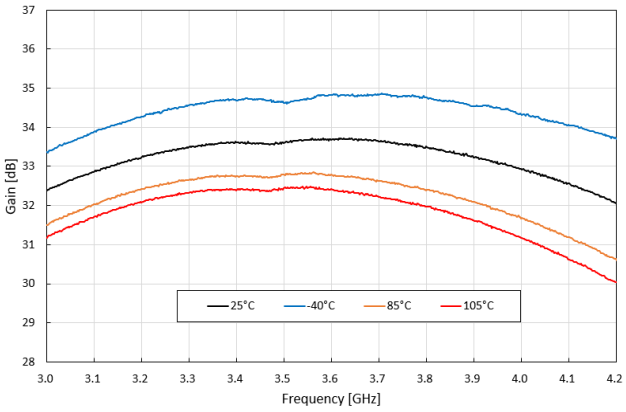


Figure 8. Gain Flatness

: Min Gain State, Temp.

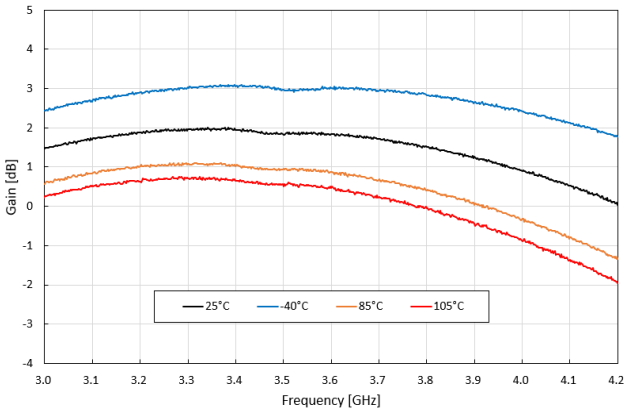


Figure 9. Input Return Loss

: Max Gain State, Temp.

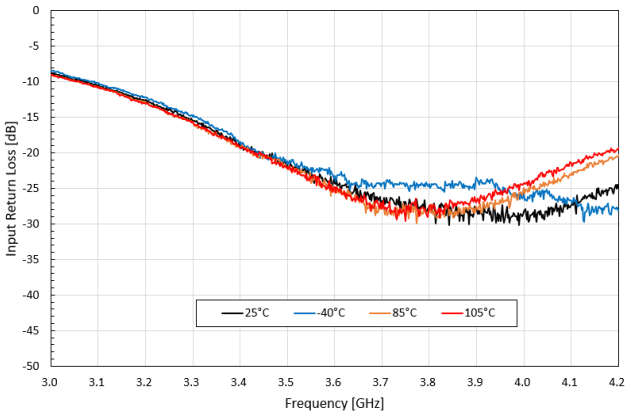
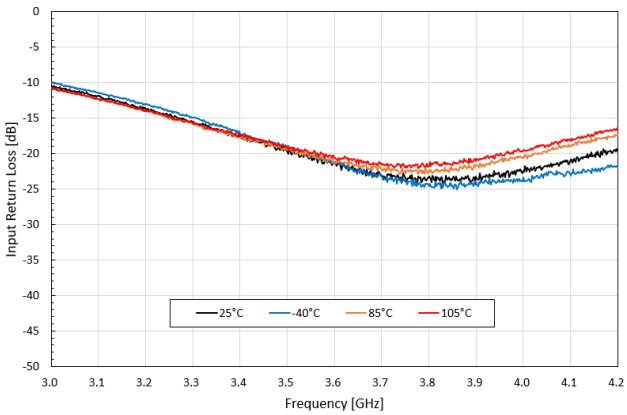


Figure 10. Input Return Loss

: Min Gain State, Temp.



Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Typical RF Performance - BVA7242N EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 11. Output Return Loss

: Max Gain State, Temp.

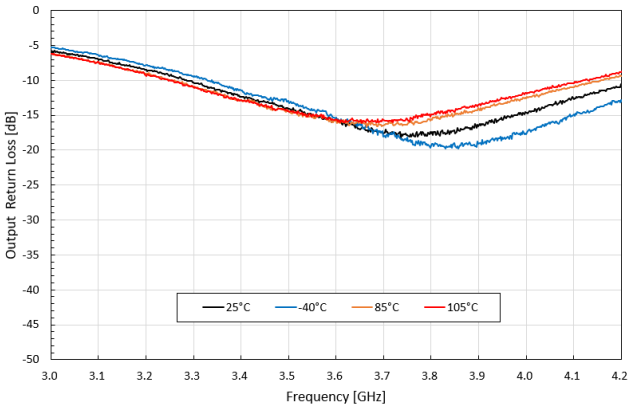


Figure 12. Output Return Loss

: Min Gain State, Temp.

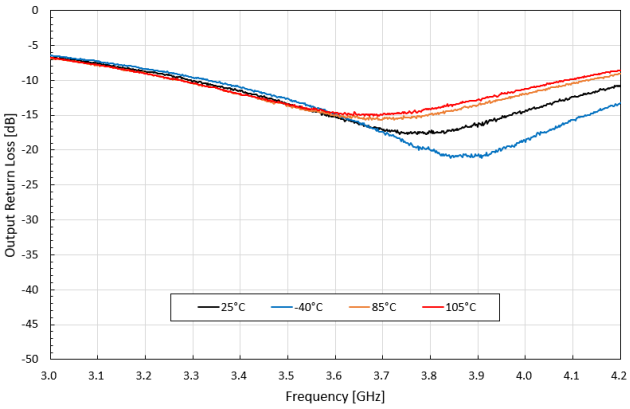


Figure 13. Gain vs Frequency

: Attenuation Step

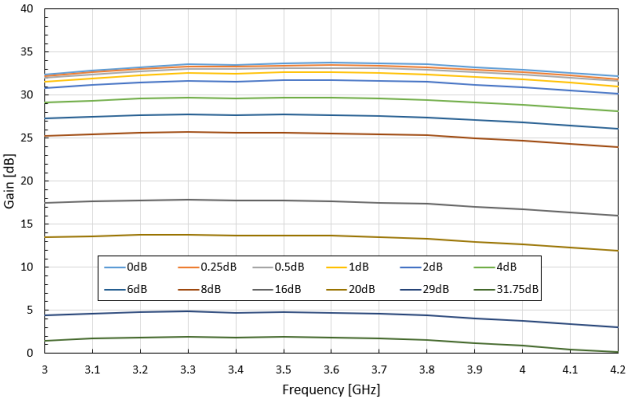


Figure 14. Gain vs Attenuation Settings

: Frequency

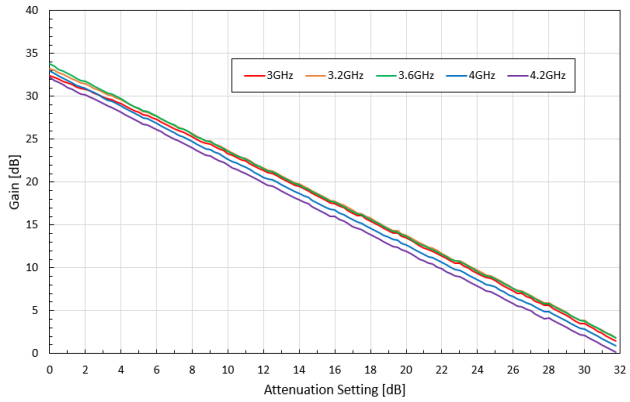
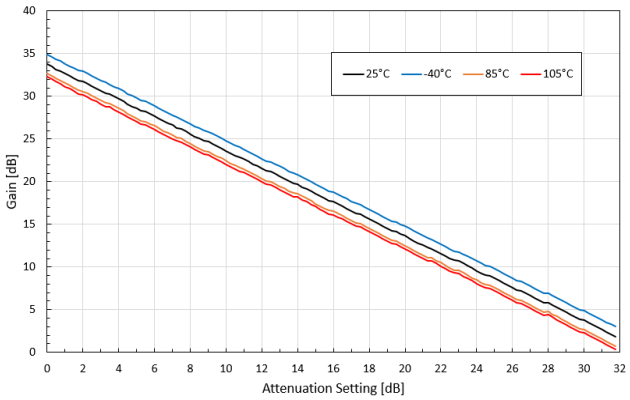


Figure 15. Gain vs Attenuation Settings

: 3.6GHz, Temp.



Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Typical RF Performance - BVA7242N EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 16. Attenuation Error
: 3.6GHz, Temp.

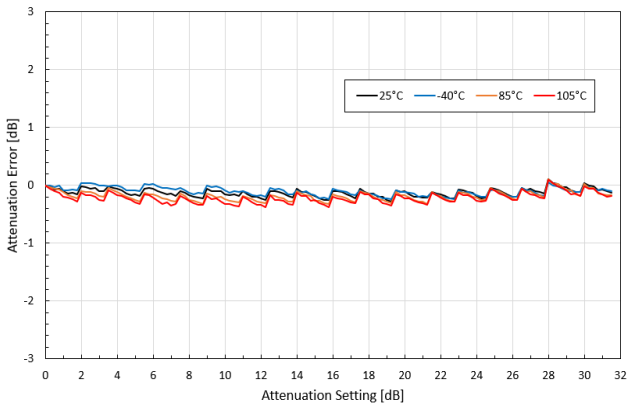


Figure 17. Attenuation Error
: Frequency

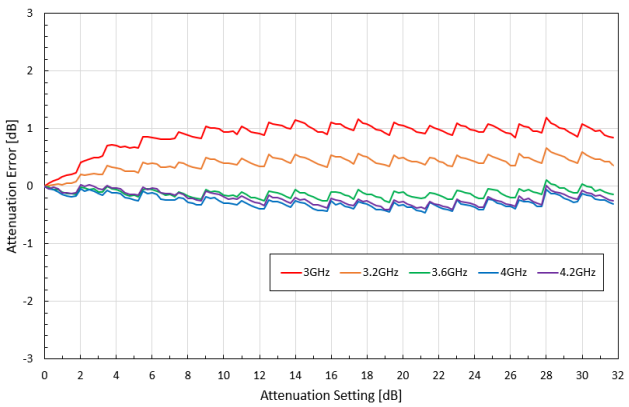


Figure 18. Attenuation Error
: Attenuation Step

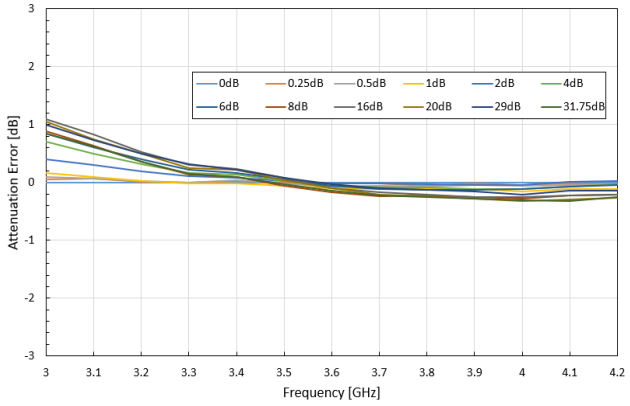


Figure 19. Relative Phase Error
: 3.6GHz, Temp.

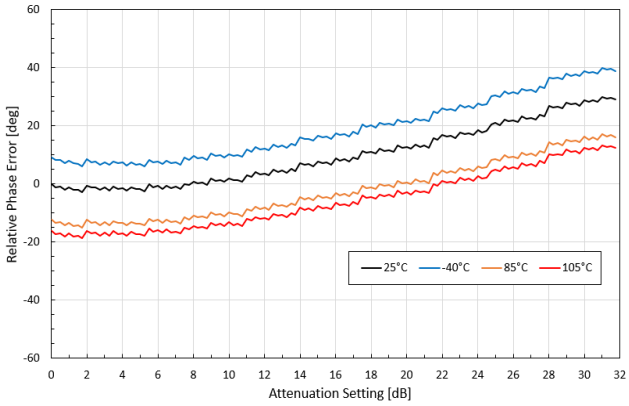
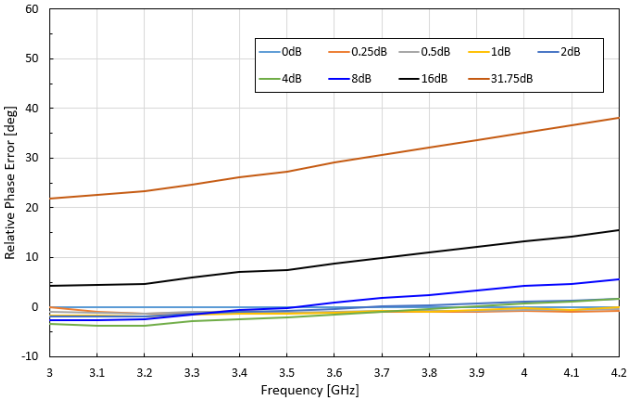


Figure 20. Relative Phase Error
: Attenuation Step



Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Typical RF Performance - BVA7242N EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 21. OIP3

: 3.6GHz, Temp., Output=-3dBm/tone, 100MHz interval

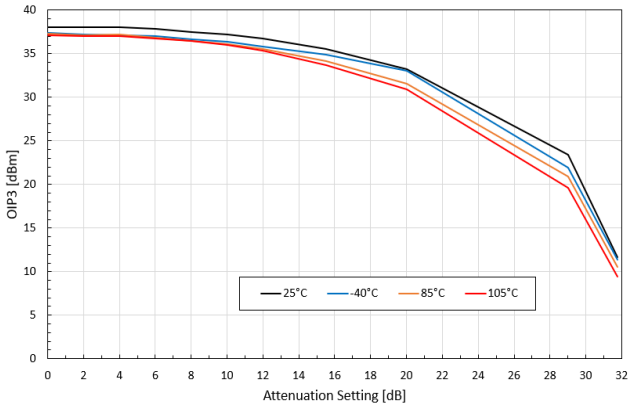


Figure 22. OIP3

: Frequency, Output=-3dBm/tone, 100MHz interval

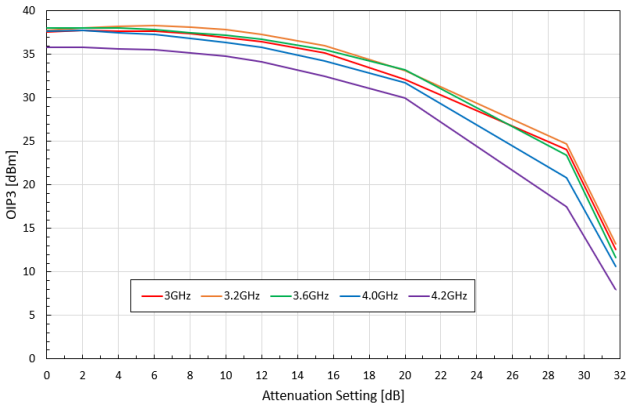


Figure 23. OIP3

: ATT=0dB, Temp., Output=-3dBm/tone, 100MHz interval

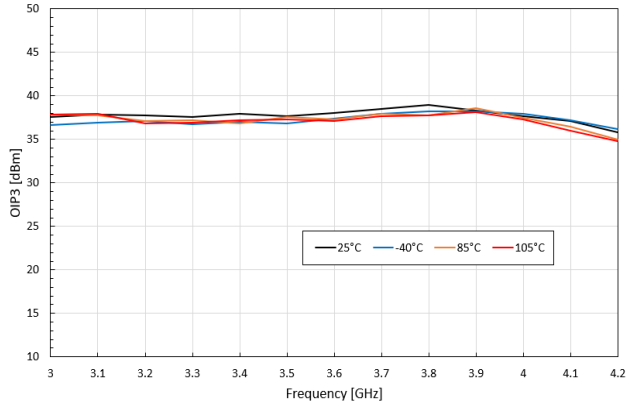


Figure 24. 2nd Harmonics

: ATT=0dB, Temp., Input=-20dBm (Output=13.5dBm)

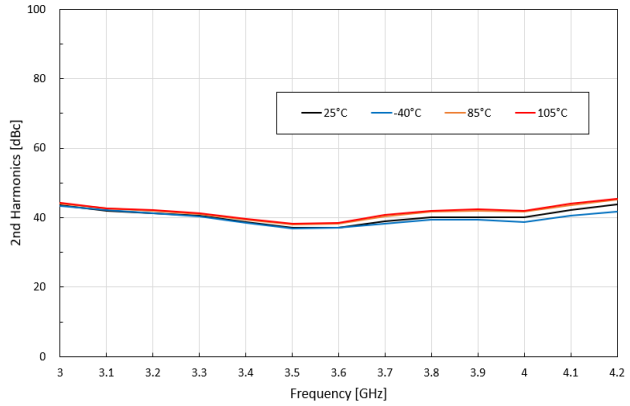


Figure 25. 2nd Harmonics

: Attenuation Step, Input=-20dBm

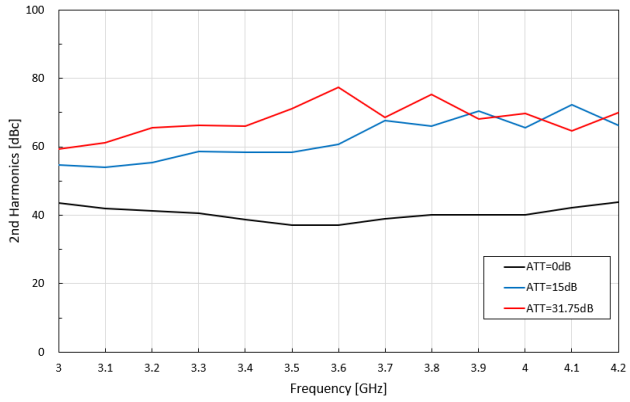
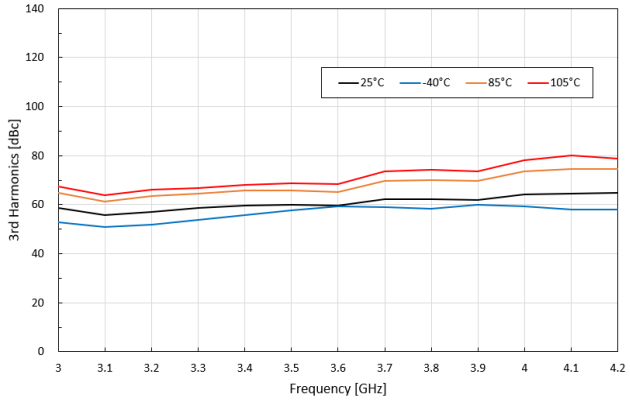


Figure 26. 3rd Harmonics

: ATT = 0dB(Max Gain), Input=-20dBm (Output=13.5dBm)



Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Typical RF Performance - BVA7242N EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 27. 3rd Harmonics

: Attenuation Step, Input=-20dBm

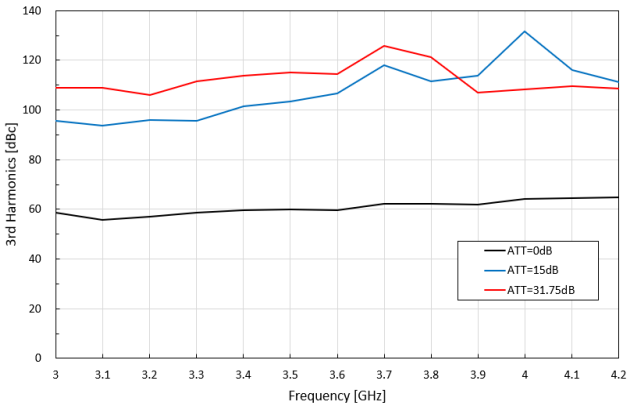


Figure 28. OP1dB

: 3.6GHz, Temp.

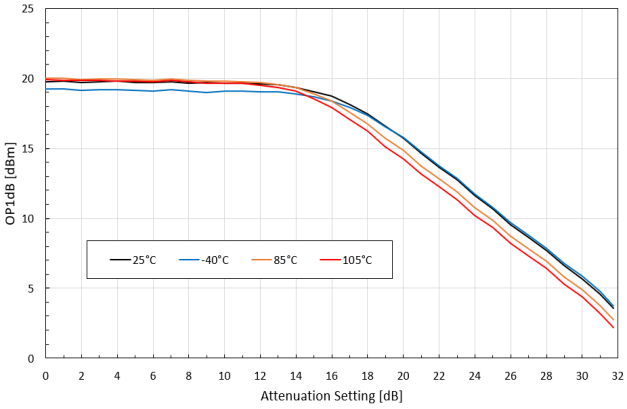


Figure 29. OP1dB

: Frequency

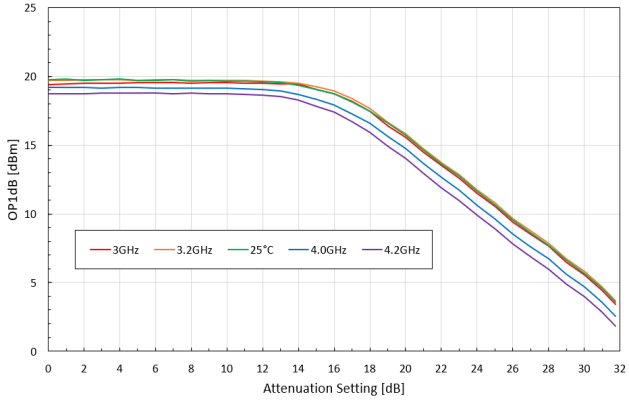


Figure 30. OP1dB

: ATT=0dB (Max Gain), Temp.

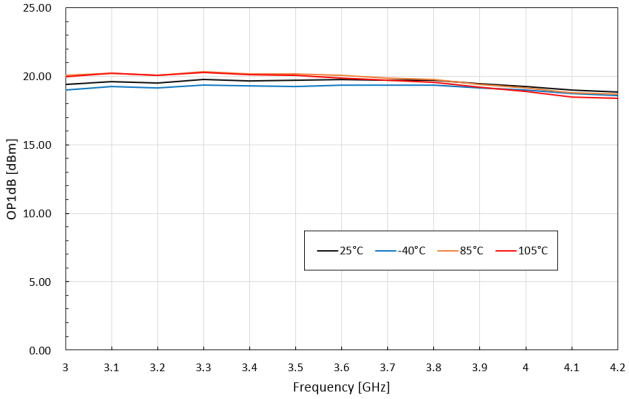


Figure 31. NF

: 3.6GHz

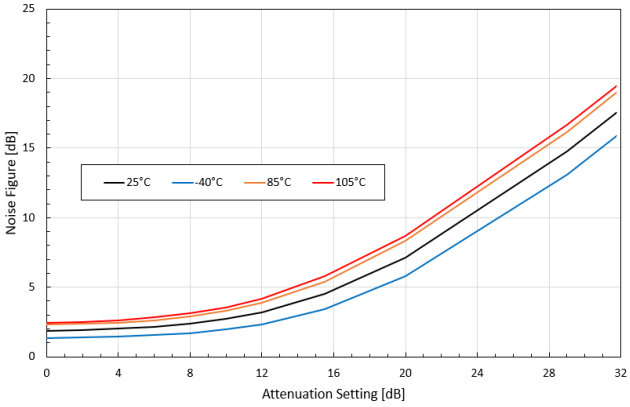
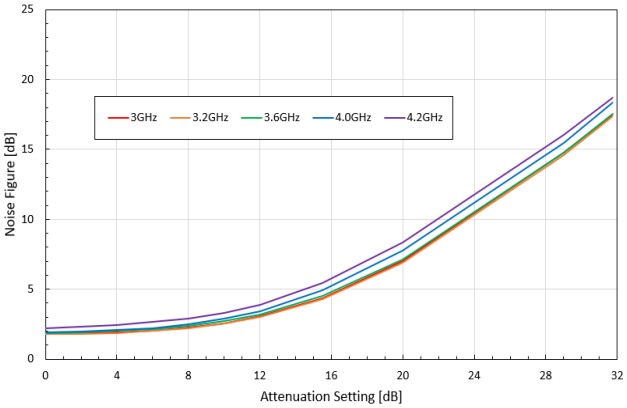


Figure 32. NF

: Frequency



Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Typical RF Performance - BVA7242N EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 33. NF

: ATT=0dB (Max Gain), Temp.

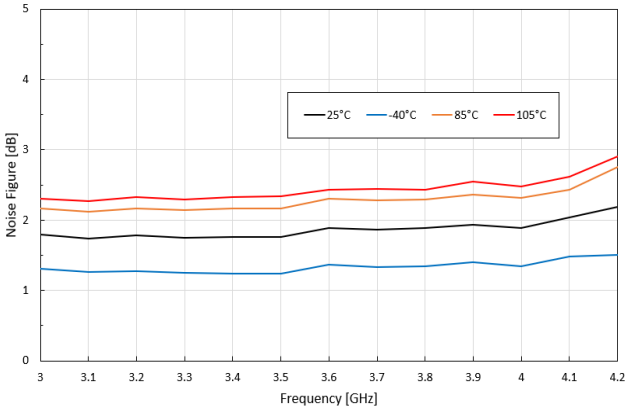


Figure 34. ACLR @ 5G NR, 100MBW

: Fc=3.05GHz, ATT=0dB, Output Power@-50dBc ACLR

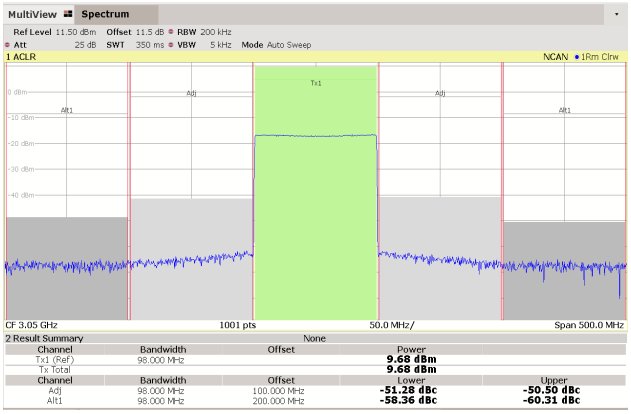


Figure 35. ACLR @ 5G NR, 100MBW

: Fc=3.6GHz, ATT=0dB, Output Power@-50dBc ACLR

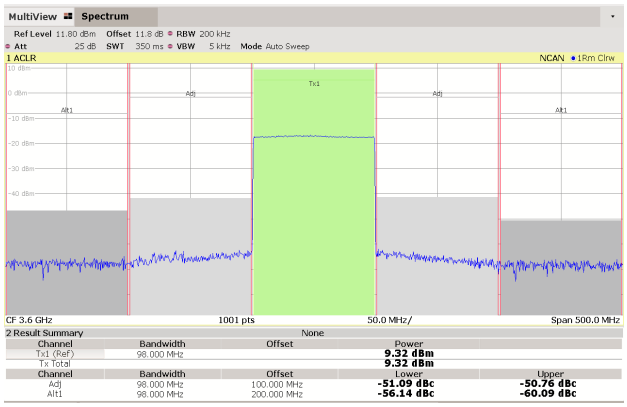


Figure 36. ACLR @ 5G NR, 100MBW

: Fc=4.15GHz, ATT=0dB, Output Power@-50dBc ACLR

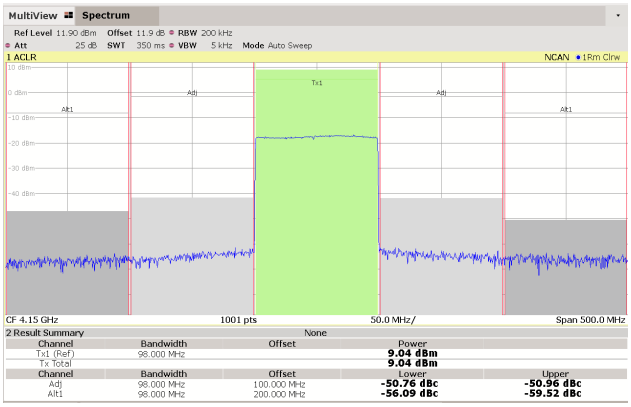


Figure 37. Power On/Off Time

: Rising Time (Control 50% to RF 90%)

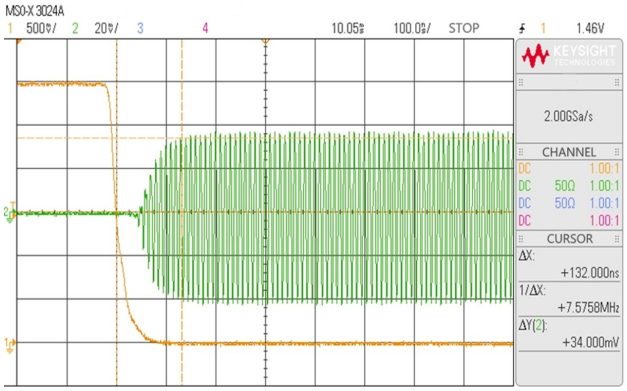
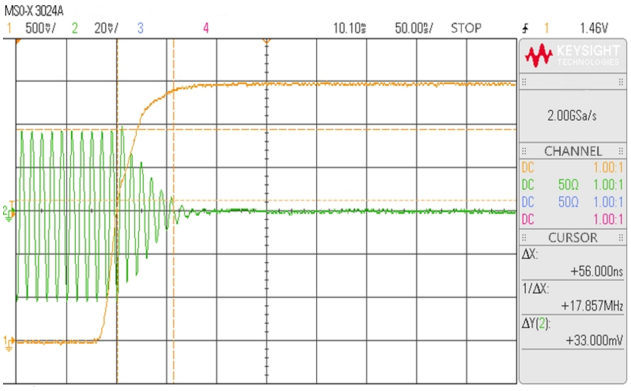


Figure 38. Power On/Off Time

: Falling Time (Control 50% to RF 10%)



Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Figure 39. Evaluation Board Schematic

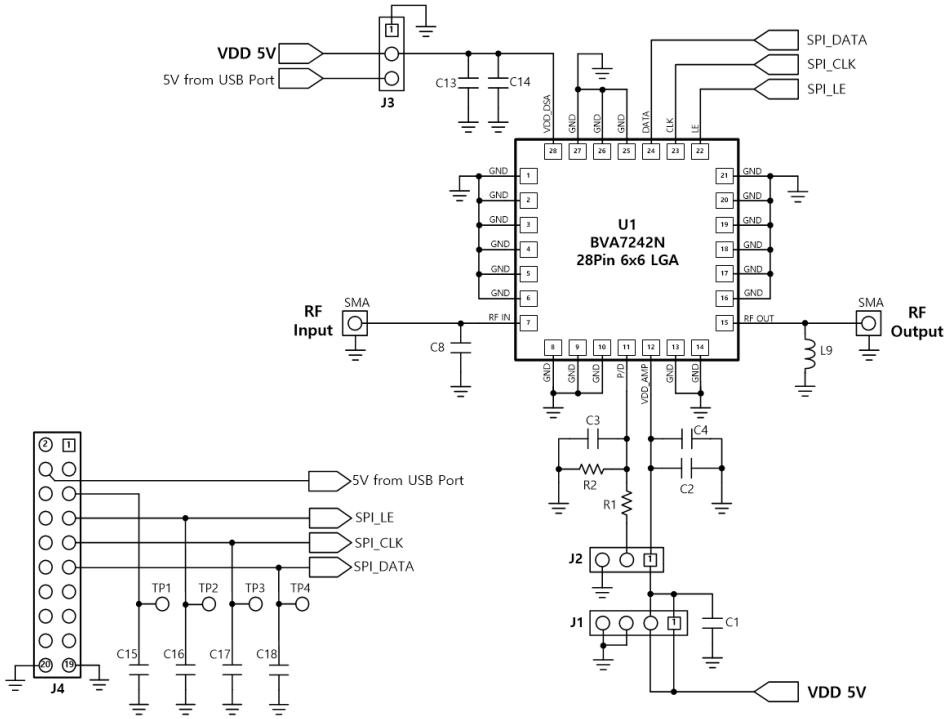
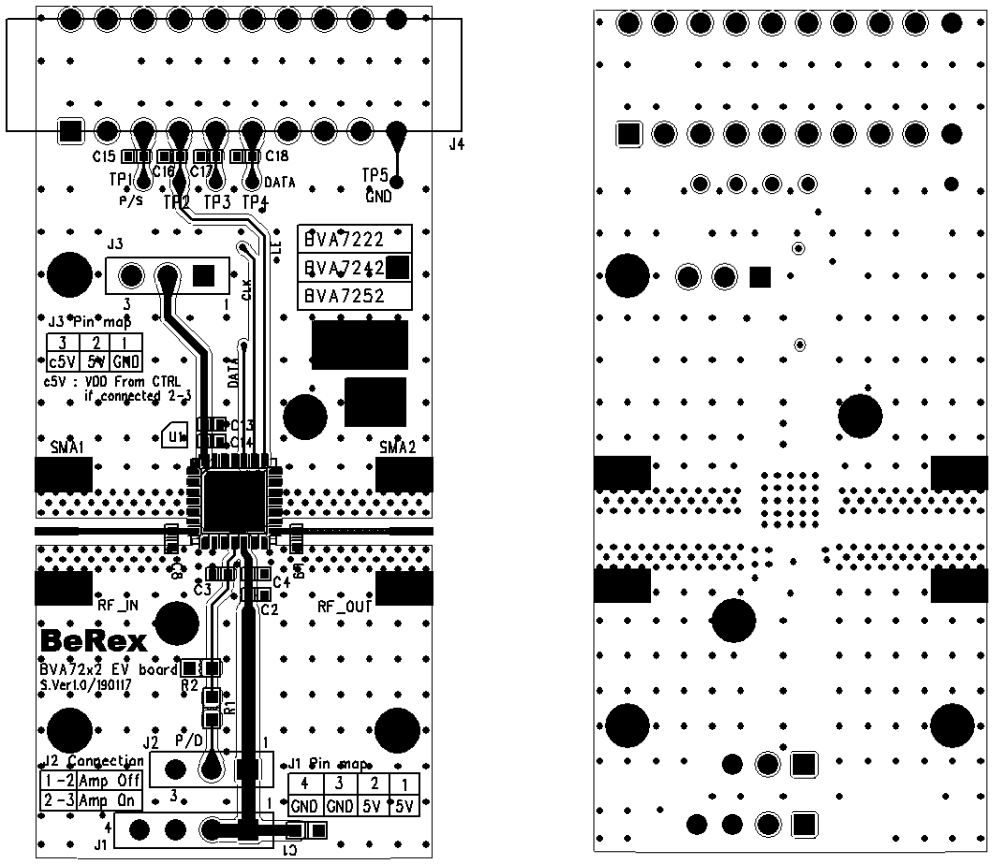


Table 10. Bill of material

No.	Ref. Number	Value	Description	Manufacturer
1	R1	20 Kohm	Resistor, 0603, Chip, 5%	Walsin
2	R2	30 Kohm	Resistor, 0603, Chip, 5%	Walsin
3	C1	1 uF	Capacitor, 0603, Chip, 5%	Murata
4	C2	100 nF	Capacitor, 0402, Chip, 5%	Murata
5	C3	100 pF	Capacitor, 0402, Chip, 5%	Murata
6	C4	100 pF	Capacitor, 0402, Chip, 5%	Murata
7	C8	0.4 pF	Capacitor, 0402, Chip, 5%	Murata
8	L9	4.7 nH	Inductor, 0402, Chip, 5%	Murata
9	C13	100 nF	Capacitor, 0402, Chip, 5%	Murata
10	C14	100 pF	Capacitor, 0402, Chip, 5%	Murata
11	SMA1	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
12	SMA2	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
13	J1	4pin	2.54mm Breakaway Male Header, Straight, Black	
14	J2	3pin	2.54mm Breakaway Male Header, Straight, Black	
15	J3	3pin	2.54mm Breakaway Male Header, Straight, Black	
16	J4	20pin	Receptacle Connector, 5-532955-3, Female,RT/A Dual	AMP Connectors
17	C15,C16,C17,C18	DNI	Not connected	

Specifications and information are subject to change without notice.
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

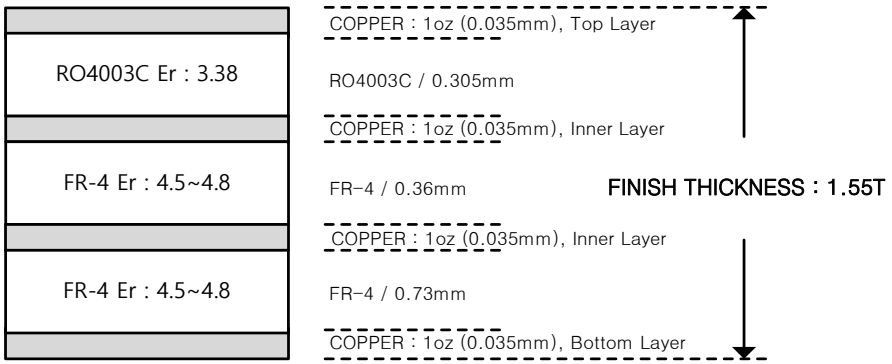
Figure 40. Evaluation Board Layout



[Top View]

[Bottom View]

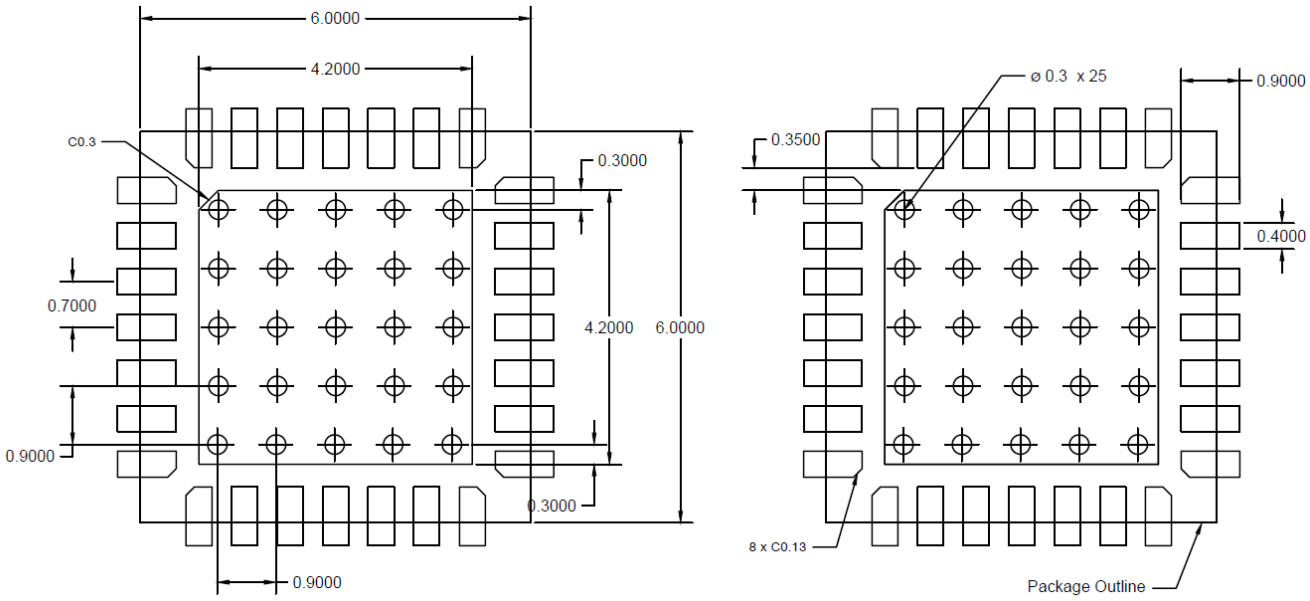
Figure 41. Evaluation Board PCB Layer Information



Specifications and information are subject to change without notice.

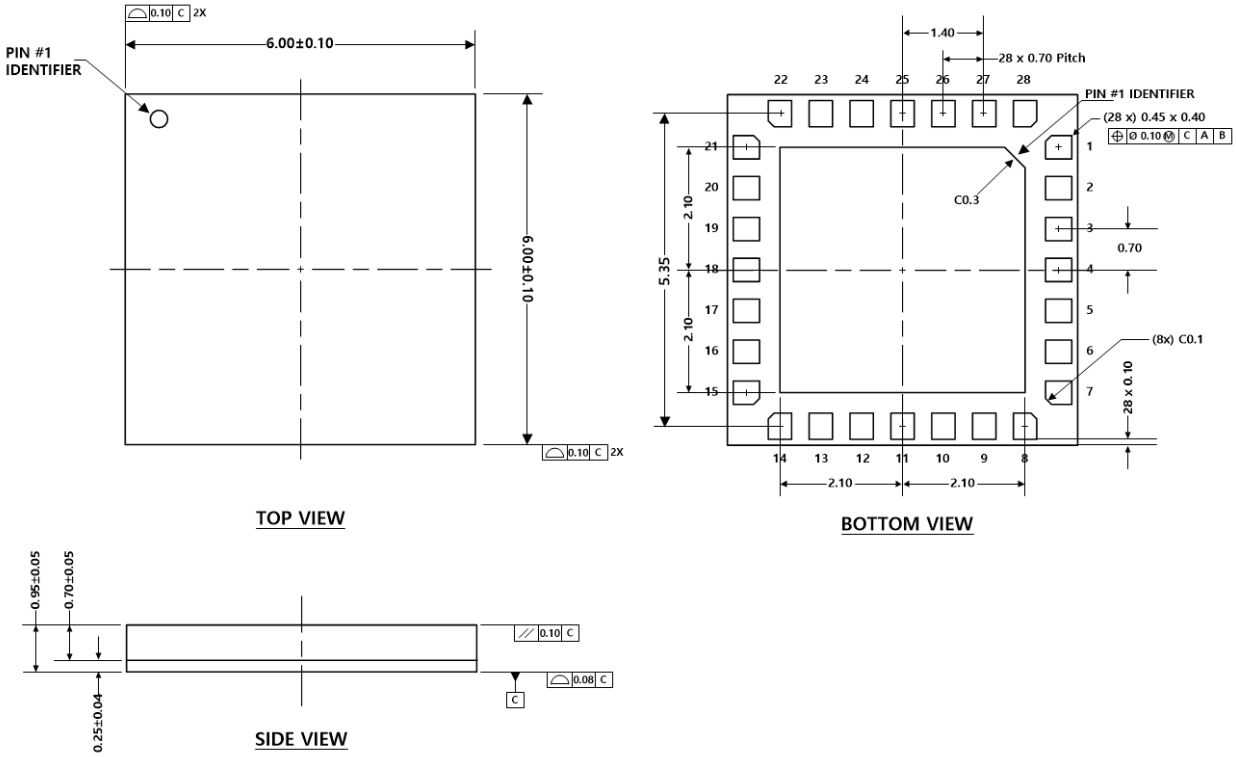
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Figure 42. Suggested PCB Land Pattern and PAD Layout



Specifications and information are subject to change without notice.
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Figure 43. Package Outline Dimension



Notes

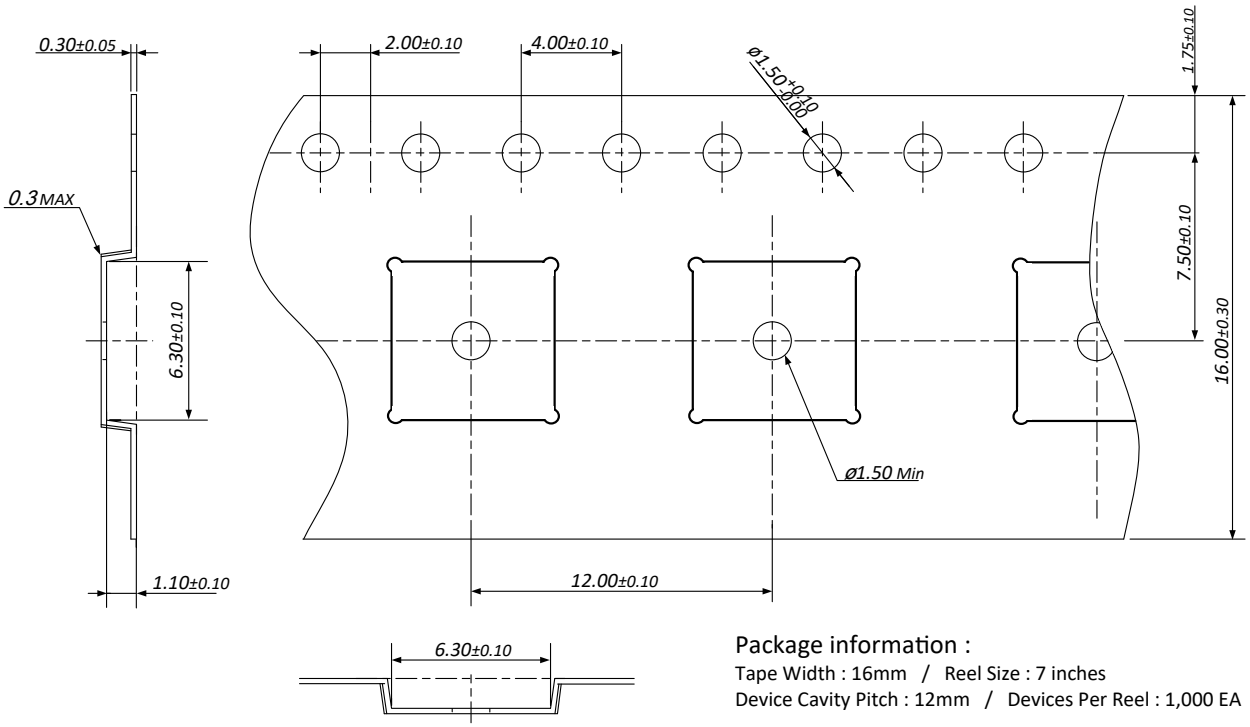
1. All dimensions are in millimeters. Angles are in degrees
2. Dimensions and tolerance conform with ASME Y14.5M-1994.

Figure 44. Package Marking Information

YY = Year
WW = Working Week
XX = Wafer Lot Number

Specifications and information are subject to change without notice.
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Figure 45. Tape and Reel



Package information :

Tape Width : 16mm / Reel Size : 7 inches

Device Cavity Pitch : 12mm / Devices Per Reel : 1,000 EA

Specifications and information are subject to change without notice.

BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex

Lead Plating Finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating :	Class 1C
Value :	1000V
Test :	Human Body Model (HBM)
Standard :	JEDEC Standard JS-001-2017

ESD Rating :	Class C5
Value :	1000V
Test :	Charged Device Model (CDM)
Standard :	JEDEC Standard JESD22-C101F

MSL Rating :	MSL3 at +260°C convection reflow
Standard :	JEDEC Standard J-STD-020

Caution : ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling the device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO GAGE Code :

2	N	9	6	F

Specifications and information are subject to change without notice.
BeRex is a trademark of BeRex. All other trademarks are the property of their respective owners. © 2021 BeRex