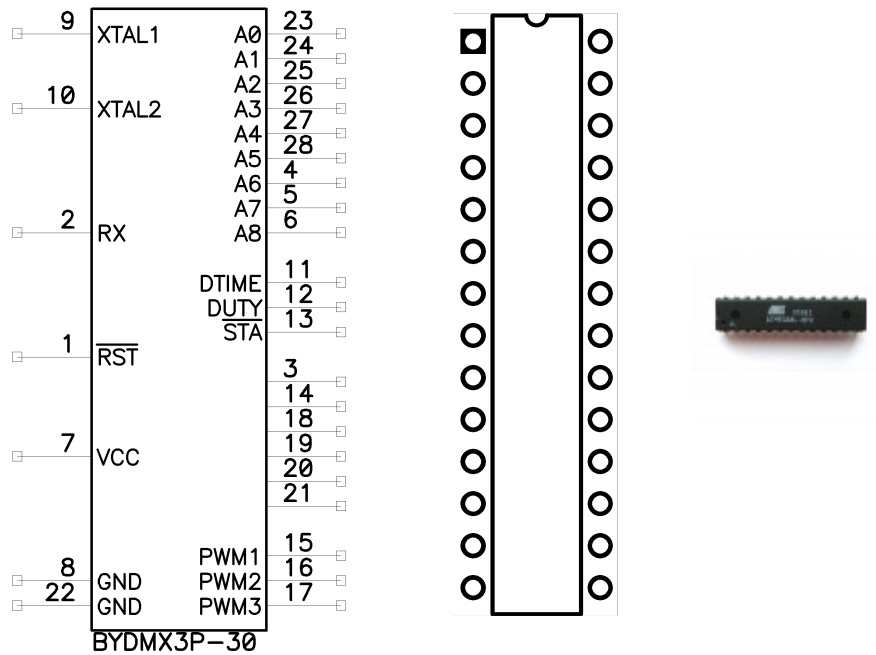


BYDMX3P-30/SP
BYDMX3P-31/TQFP

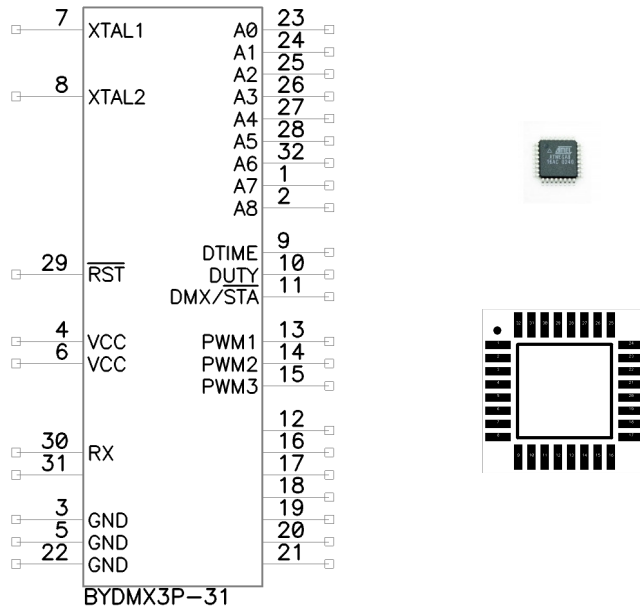
Data Sheet
(Rev 1.2)

Net-Control

1. Pin Diagram



28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)



32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)

2. Pin Description (BYDMX3P-30/SP)

Pin No.	Pin Name	Type	Description
1	/RST	Input	Chip Reset input. This pin is an active low RESET to the device.
2	RX	Input	DMX Signal Input.
3			
4	A6	Input	Address bit 6.
5	A7	Input	Address bit 7.
6	A8	Input	Address bit 8.
7	VCC	Power	Positive supply for logic and I/O pins(5VDC).
8	GND	Power	Ground reference for logic and I/O pins(0V).
9	XTAL1	Input	Crystal input(16MHz Only).
10	XTAL2	Input	Crystal input(16MHz Only).
11	DTIME	Input	STA mode delay time(H- Fast, L- Slow).
12	DUTY	Input	no use
13	DMX/STA	Input	H- DMX Mode, L- Stand Alone Mode
14			
15	PWM1	Output	Pulse width modulation output #1.
16	PWM2	Output	Pulse width modulation output #2.
17	PWM3	Output	Pulse width modulation output #3.
18			
19			
20			
21			
22	GND	Power	Ground reference for logic and I/O pins(0V).
23	A0	Input	Address bit 0.
24	A1	Input	Address bit 1.
25	A2	Input	Address bit 2.
26	A3	Input	Address bit 3.
27	A4	Input	Address bit 4.
28	A5	Input	Address bit 5.

* Address and DTIME, DUTY, DMX/STA pins are normal high(Internal pullup).

(BYDMX3P-31/TQFP)

Pin No.	Pin Name	Type	Description
1	A7	Input	Address bit 7.
2	A8	Input	Address bit 8.
3	GND	Power	Ground reference for logic and I/O pins(0V).
4	VCC	Power	Positive supply for logic and I/O pins(5VDC).
5	GND	Power	Ground reference for logic and I/O pins(0V).
6	VCC	Power	Positive supply for logic and I/O pins(5VDC).
7	XTAL1	Power	Crystal input(16MHz Only).
8	XTAL2	Power	Crystal input(16MHz Only).
9	DTIME	Input	STA mode delay time(H- Fast, L- Slow).
10	DUTY	Input	no use
11	DMX/STA	Input	H- DMX Mode, L- Stand Alone Mode
12			
13	PWM1	Output	Pulse width modulation output #1.
14	PWM2	Output	Pulse width modulation output #2.
15	PWM3	Output	Pulse width modulation output #3.
16			
17			
18			
19			
20			
21			
22	GND	Power	Ground reference for logic and I/O pins(0V).
23	A0	Input	Address bit 0.
24	A1	Input	Address bit 1.
25	A2	Input	Address bit 2.
26	A3	Input	Address bit 3.
27	A4	Input	Address bit 4.
28	A5	Input	Address bit 5.
29	/RST	Input	Chip Reset input. This pin is an active low RESET to the device.
30	RX	Input	DMX Signal Input.
31			
32	A6	Input	Address bit 6.

3. Address Select.

L(Logic level low) == Selected.

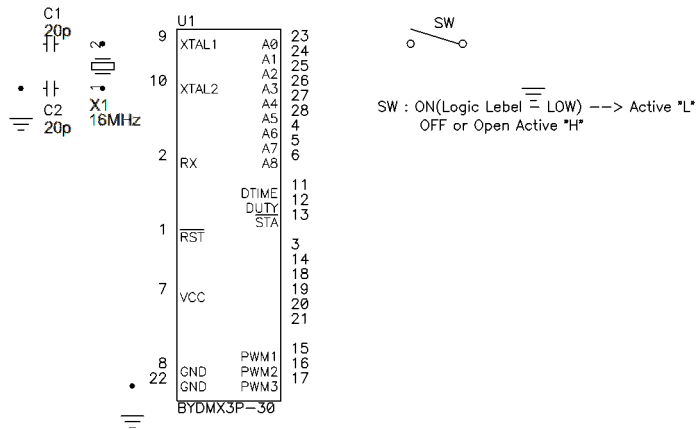
H(Logic level high) == Unselected.

*Address input is normal pullup.

Address	Hex	Dec	A8	A7	A6	A5	A4	A3	A2	A1	A0
00000000	000	000	H	H	H	H	H	H	H	H	H
00000001	001	001	H	H	H	H	H	H	H	H	L
00000010	002	002	H	H	H	H	H	H	H	L	H
00000011	003	003	H	H	H	H	H	H	H	L	L
00000100	004	004	H	H	H	H	H	H	L	H	H
00000101	005	005	H	H	H	H	H	H	L	H	L
00000110	006	006	H	H	H	H	H	H	L	L	H
00000111	007	007	H	H	H	H	H	H	L	L	L
00001000	008	008	H	H	H	H	H	L	H	H	H
00001001	009	009	H	H	H	H	H	L	H	H	L
00001010	00A	010	H	H	H	H	H	L	H	L	H
00001011	00B	011	H	H	H	H	H	L	H	L	L
00001100	00C	012	H	H	H	H	H	L	L	H	H
00001101	00D	013	H	H	H	H	H	L	L	H	L
00001110	00E	014	H	H	H	H	H	L	L	L	H
00001111	00F	015	H	H	H	H	H	L	L	L	L
00010000	010	016	H	H	H	H	L	H	H	H	H
00010001	011	017	H	H	H	H	L	H	H	H	L
00010010	012	018	H	H	H	H	L	H	H	L	H
00010011	013	019	H	H	H	H	L	H	H	L	L
00010100	014	020	H	H	H	H	L	H	L	H	H
00010101	015	021	H	H	H	H	L	H	L	H	L
00010110	016	022	H	H	H	H	L	H	L	L	H
00010111	017	023	H	H	H	H	L	H	L	L	L
00011000	018	024	H	H	H	H	L	L	H	H	H
00011001	019	025	H	H	H	H	L	L	H	H	L
00011010	01A	026	H	H	H	H	L	L	H	L	H
00011011	01B	027	H	H	H	H	L	L	H	L	L
00011100	01C	028	H	H	H	H	L	L	L	H	H
00011101	01D	029	H	H	H	H	L	L	L	H	L
00011110	01E	030	H	H	H	H	L	L	L	L	H
00011111	01F	031	H	H	H	H	L	L	L	L	L
00010000	020	032	H	H	H	L	H	H	H	H	H
00010001	021	033	H	H	H	L	H	H	H	H	L
00010010	022	034	H	H	H	L	H	H	H	L	H
00010011	023	035	H	H	H	L	H	H	H	L	L
..
..
..
..
11111100	1FC	508	L	L	L	L	L	L	L	H	H
11111101	1FD	509	L	L	L	L	L	L	L	H	L
11111110	1FE	510	L	L	L	L	L	L	L	L	H
11111111	1FF	511	L	L	L	L	L	L	L	L	L

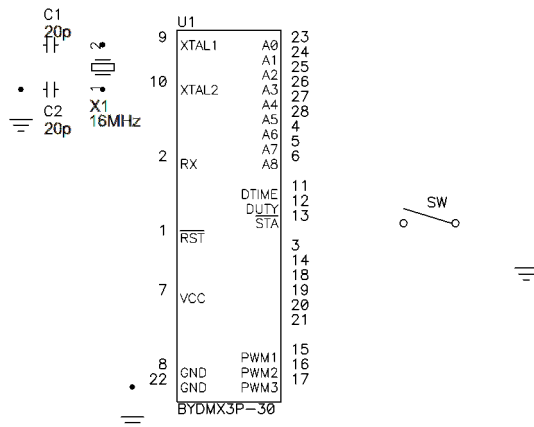
4. Wiring.

Address Select S/W Circuit example



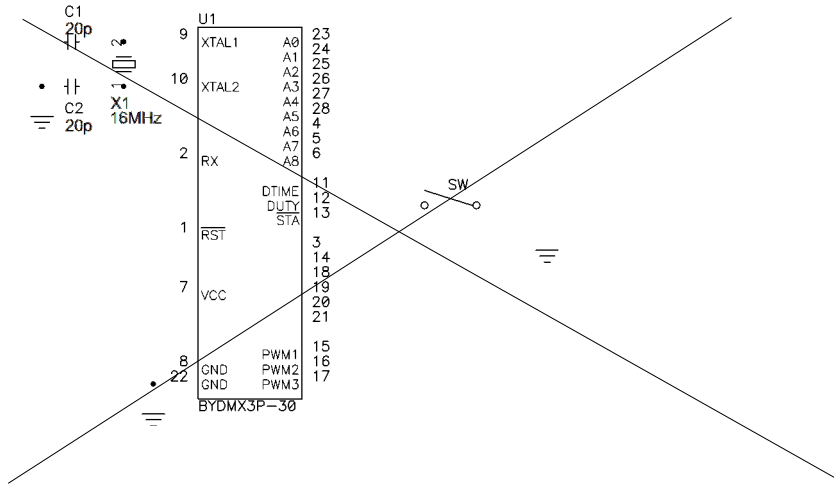
- * Logic level "H"=1
 Logic level "L"=0
- * if STA pin ="L"
 Address=Pattern No(1--11)

Stand Alone Mode S/W Circuit example

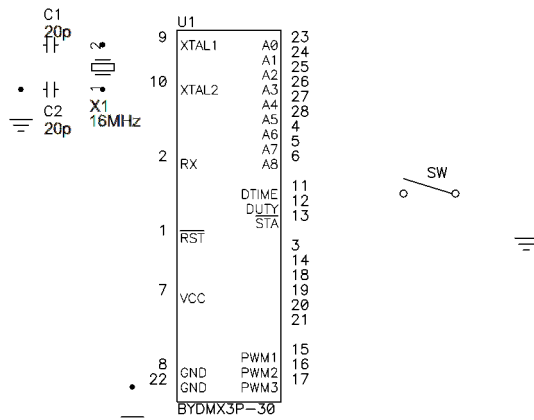


- * SW ON(Logic Level "L") = Stand Alone Mode.
- * SW OFF(Logic Level "H") = DMX Mode.

Duty S/W Circuit example



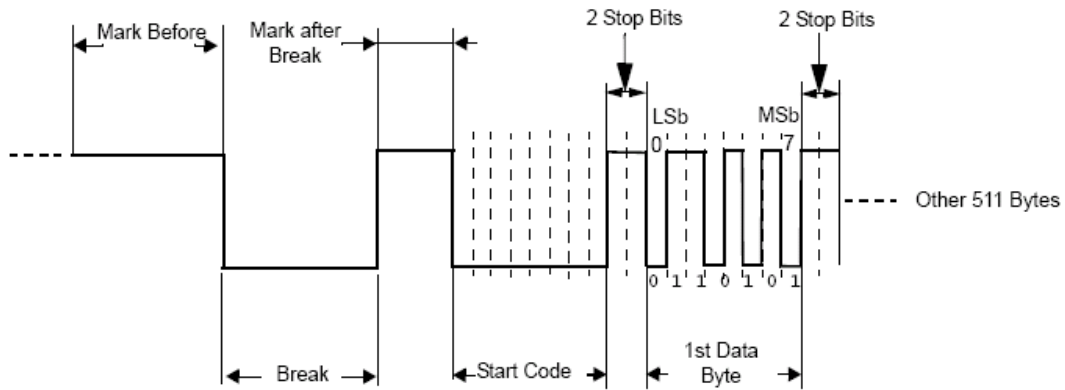
DTIME S/W Circuit example



DTIME input sw ON (active "L") --> Slow Speed Mode
 DTIME input sw OFF (active "H") --> Normal Speed Mode
 Stand Alone Mode Only

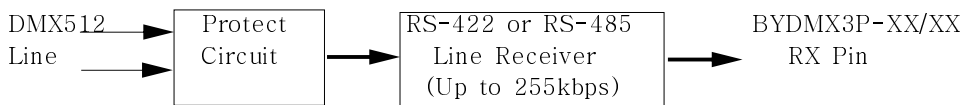
5. DMX512 Signal IN

DMX512 Timing Diagram

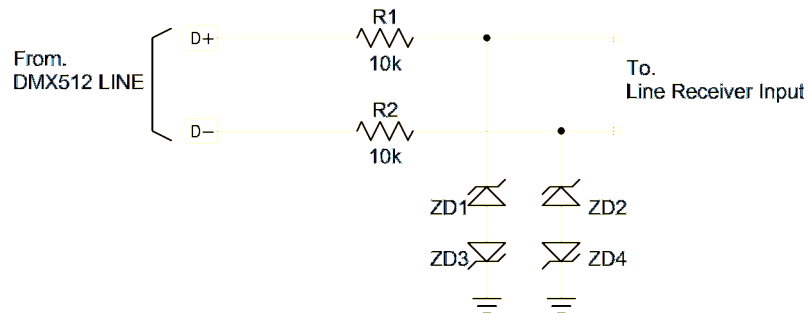


Description	Minimum	Maximum	Typical	Unit
Break	92	-	176	uSec
Mark after Break	12	<1,000,000	-	uSec
Bit Time	3.92	4.02	4	uSec
DMX512 Packet	1204	1,000,000	-	uSec

Receiver Circuit Block Diagram



Protect Circuit example



6. PWM OUTPUT

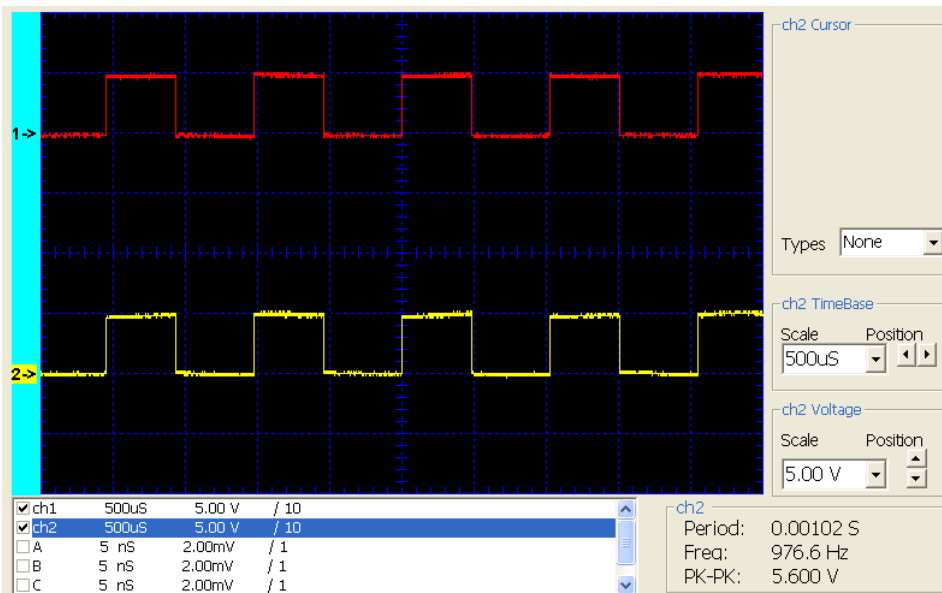
Output Address

PWM1 : Address
 PWM2 : Address + 1
 PWM3 : Address + 2

If Address set 100.
 PWM1 : 100
 PWM2 : 101
 PWM3 : 102

Output Current : Max 10(mA)
 PWM Frequency : PWM1, PWM2, PWM3
 1000Hz -- 976.6Hz (DUTY PIN HIGH or OPEN)

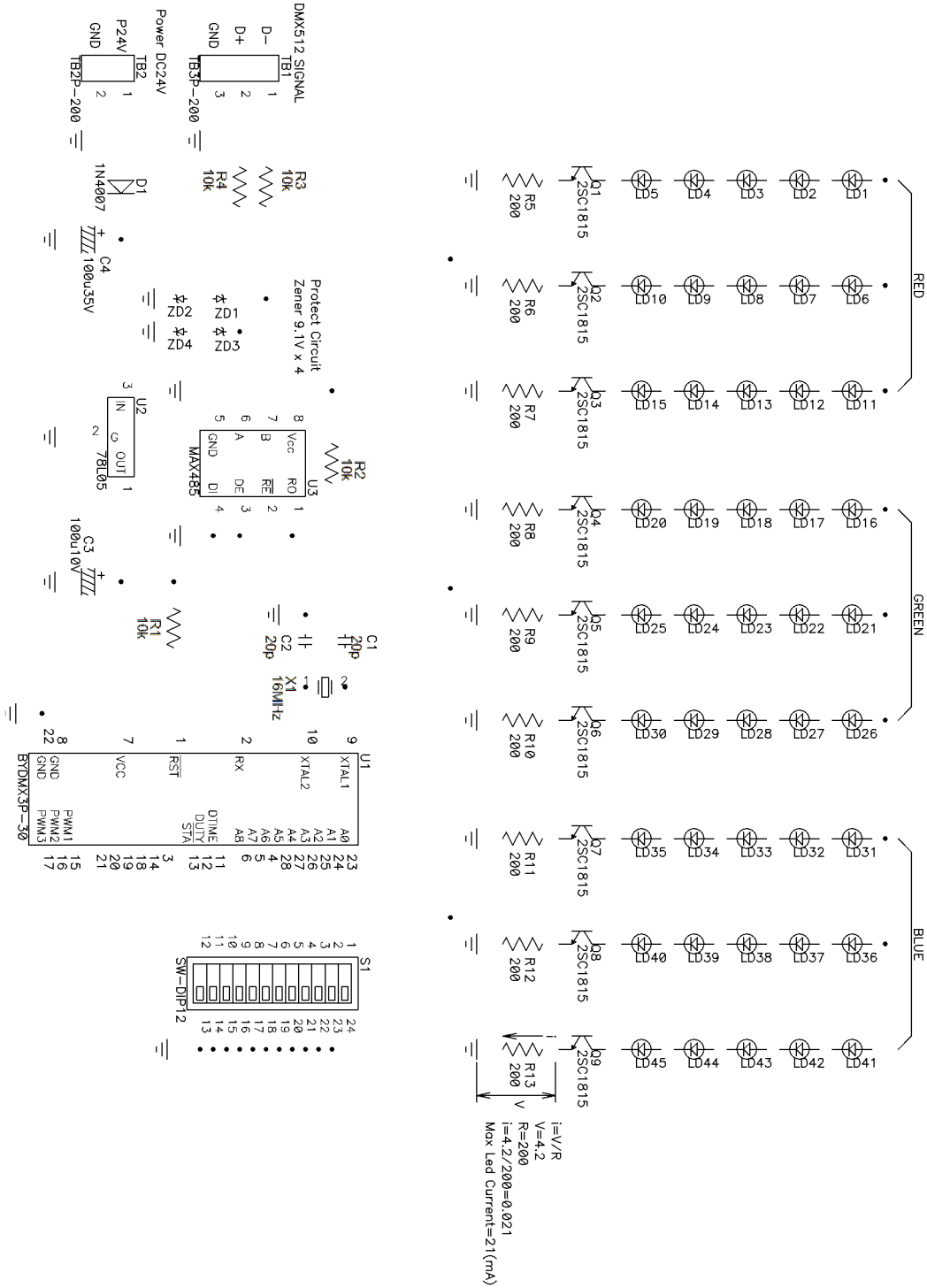
Duty Ratio : 1/255
 Data : 8bit(0 to 255(dec) or 0 to FF(Hex)).
 Power On Initial value : 1(1/255)



PWM1 DUTY = 120/255
 PWM2 DUTY = 120/255

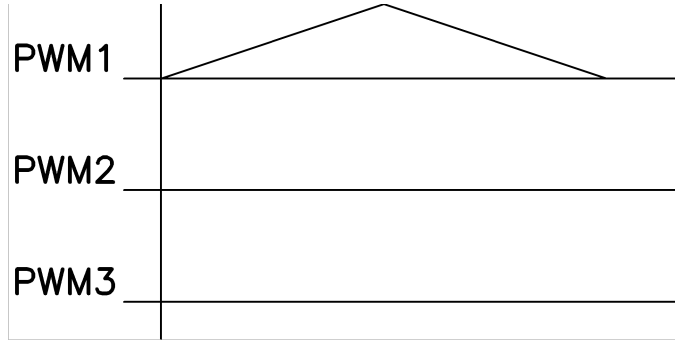
7. Sample Schematic(BYDMX3P-30)

DMX512 PWM True Color LED LAMP Sample Schematic(Using BYDMX3P-30/SP Receiver Chip)
 Net-Control(<http://www.net-control.co.kr>)
 E-mail : moon@by.co.kr

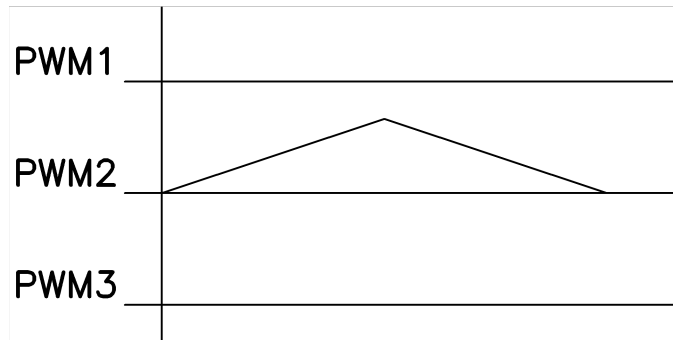


8. Stand Alone Mode Pattern

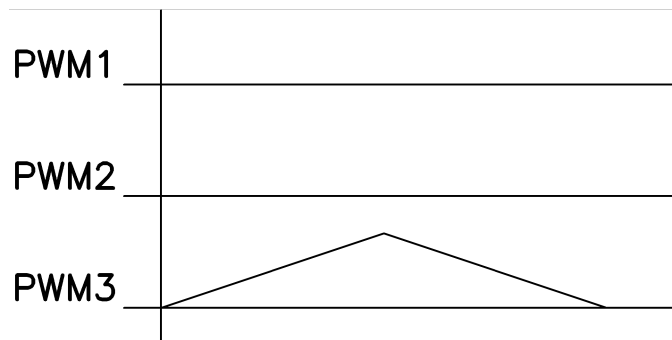
Address=1



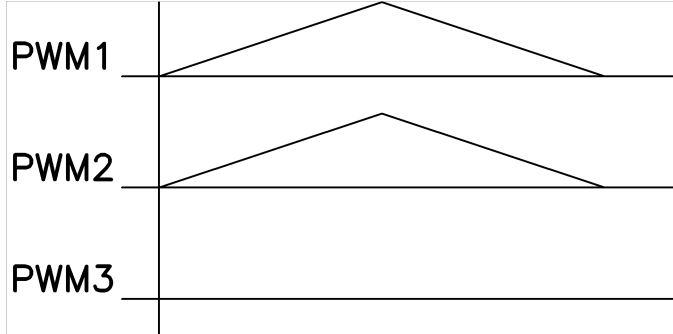
Address=2



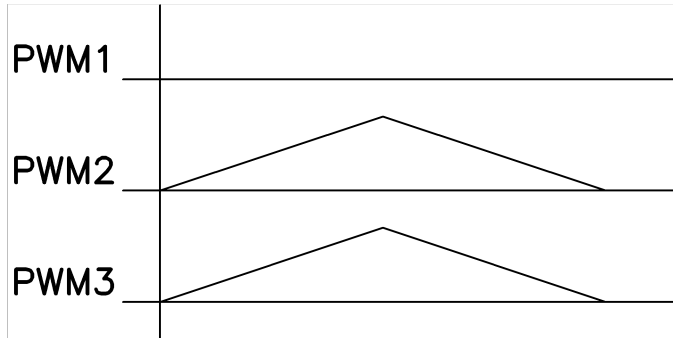
Address=3



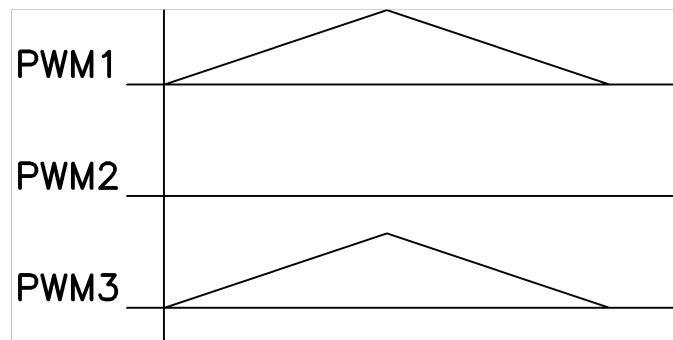
Address=4



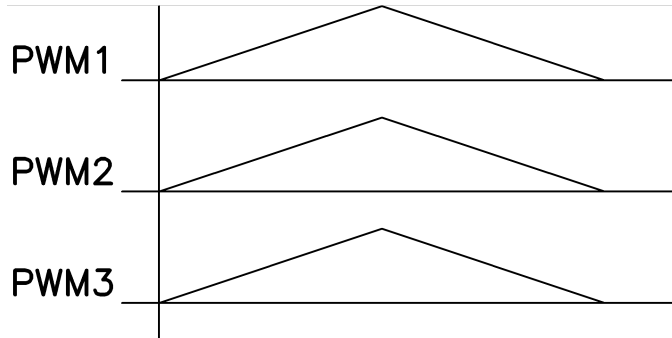
Address=5



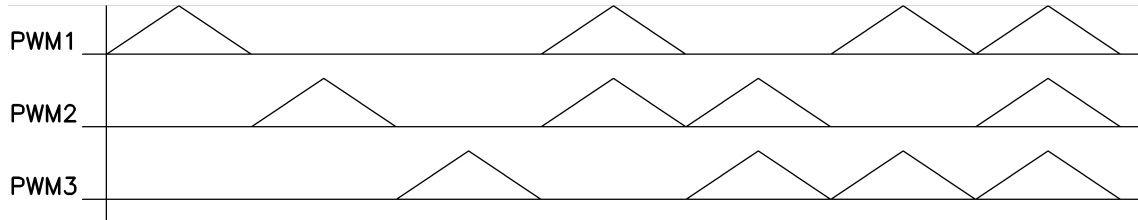
Address=6



Address=7



Address=8

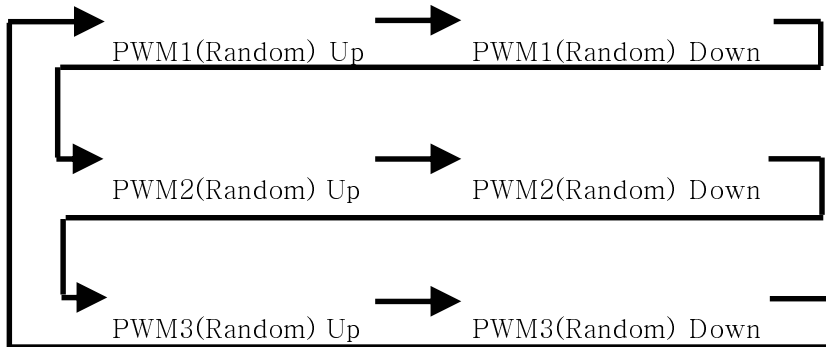


Address=9

Random up/down



Address=10



Address=11

PWM1
 PWM2 (Random Mixing Pattern)
 PWM3