IVO InfoVision Optoelectronics (Kunshan)Co., Ltd.

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IVO Product Information

To:

Product Name: C035SWN1-1

Document Issue Date: 2012-7-12

Customer	InfoVision Optoelectronics
SIGNATURE	**SIGNATURE**
	QA
	PREPARED BY **FAE**
Please return 1 copy for your confirmation with your signature and comments.	

Note: 1. Please contact InforVision Company. Before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

FQ-7-30-0-009-03D

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Revision	Date	Page	Old Description	New Description	Remark
00	2012-7-12	All		First issued	

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1 General Description

C035SWN1-1 is a Color Active Matrix Liquid Crystal Display composed of 50chip TN TFT LCD Cell. The format of screen is intended to support the HVGA resolution 320 horizontal by 480 vertical pixel array.

2 General Characteristics

Item			Specification	Unit	Remark
Active Area (W x H)			48.96 x 73.44	mm	Single Chip
Number of Dots (W x H)			320 (RGB) x 480	dot	Single Chip
Pixel Size (W x H)			0.153x0.153	mm	Single Chip
Dimension (W x H x D)			52.96x 81.34x 0.6	mm	Not include polarizer
Display Type			Transmissive	-	-
Display Mode			TN Mode, Normally White	-	-
View Direction			12 o'clock	-	-
Temperature Range	Storage		-30 ~ 80	℃	-
	Operating		-20 ~ 70	℃	
Response Time			30 (Typ.)	ms	With IVO requirement driving condition, Refer to Section Note A,B
Contrast Ratio			500 (Typ.)	-	
Viewing Angle			Up-down : 70/60 (Typ.), Left-right : 70/70 (Typ.)	deg.	Viewing Angle base on Using EWV polarizer Reference Only
Chromaticity	NTSC Ratio		60% (Typ.)	%	With reference backlight spectrum, see in 12(with reference polarizer)
CF only Chromaticity	Red	Rx	0.637 ±0.02	-	Under C light (Viewing normal angle Θx = ΘY=0°)
		Ry	0.338 ±0.02		
	Green	Gx	0.289 ±0.02		
		Gy	0.589 ±0.02		
	Blue	Bx	0.136 ±0.02		
		By	0.143 ±0.02		
	White	Wx	0.300±0.02		
		Wy	0.340±0.02		
Panel Transmittance			5.1%(min) 5.5% (Typ.)	%	

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Color Filter Structure		Stripe RGB	-	-
Weight		339.85	g	Sub 50 Chips
		6.17		Single Chip

Note: A. Definition Of Response Time (T_R, T_F)

Figure 1 Definition of Response Time
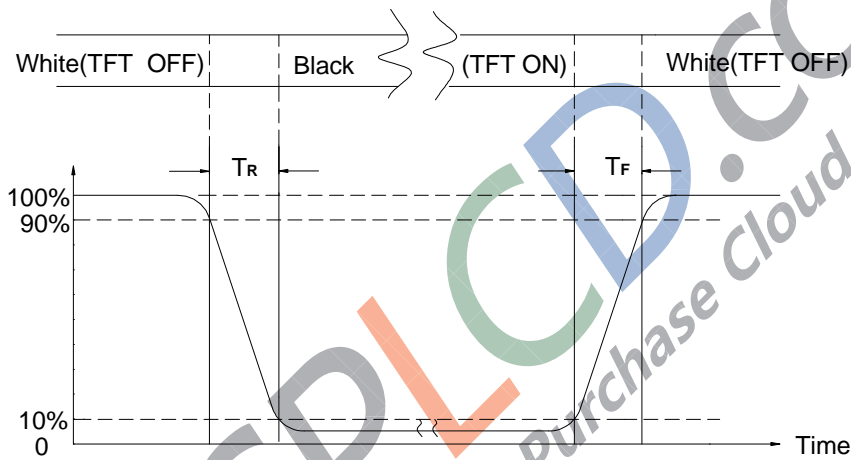
B. Measure the Response Time at 60Hz frame rate.

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3   Outline Size of Cell

52.96 ±0.2

1.8±0.1

73.44

Active Area

48.96

81.34±0.2

77.24±0.2

2±0.1   2±0.1

2±0.1

AA edge
CF edge
Array edge

4.1±0.2

Unit:mm
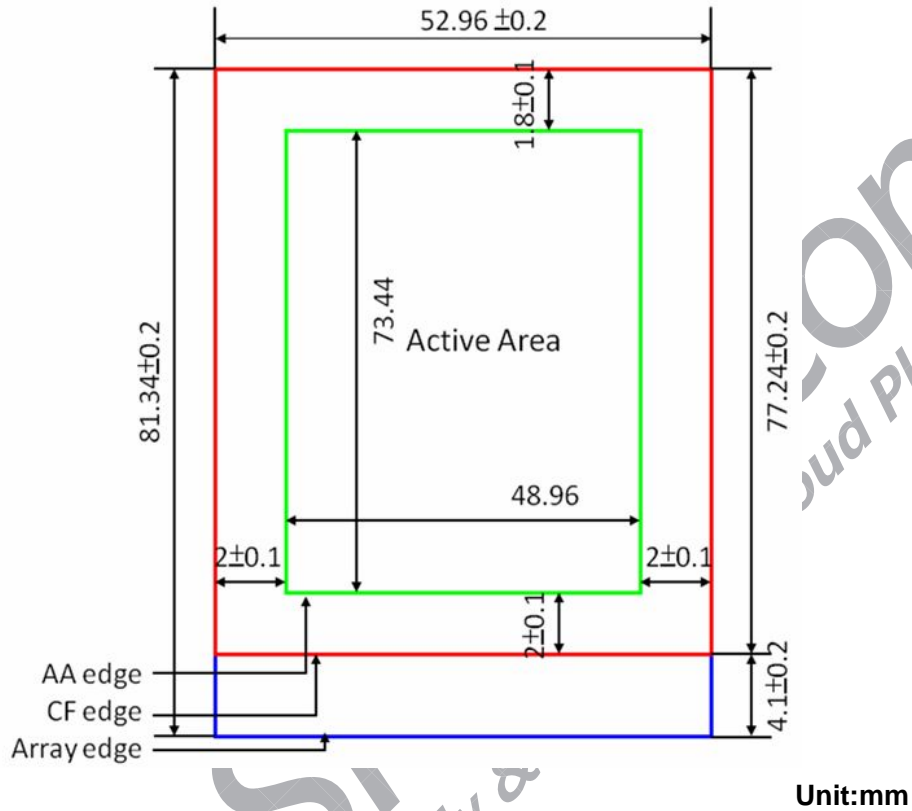
4   Cell Thickness (Single Chip)

CF Glass   0.3±0.05mm

TFTGlass   0.3±0.05mm

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5 TFT And CF Side Rubbing Direction
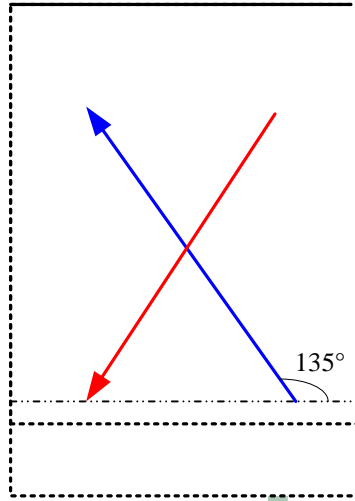
Top view from CF protective film side

→ TFT Side rubbing direction

→ CF Side rubbing direction

135°

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6 Sub sheet 50chips: Size and cut mark.

Cut ID

9000um

1900um

CF cut mark:

Array cut mark:

77.24

4.1

52.96

Unit: mm

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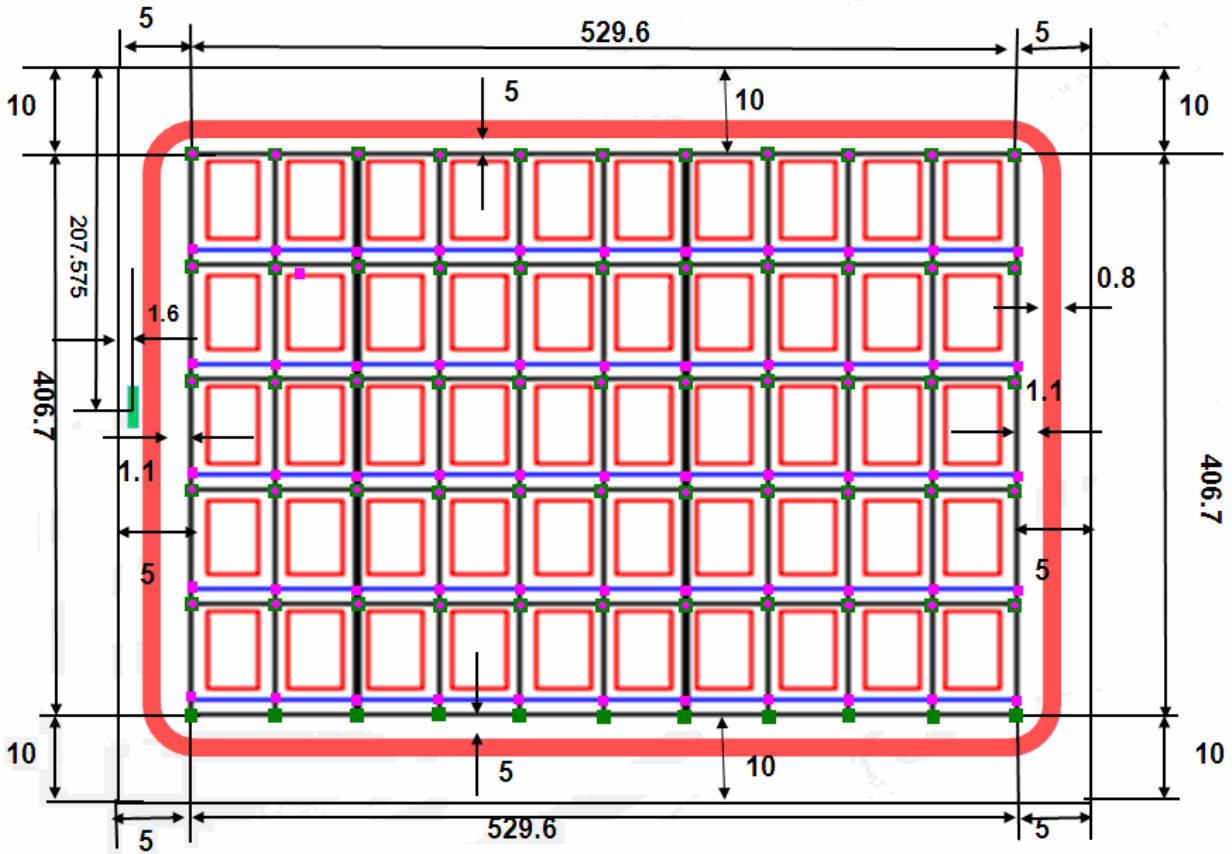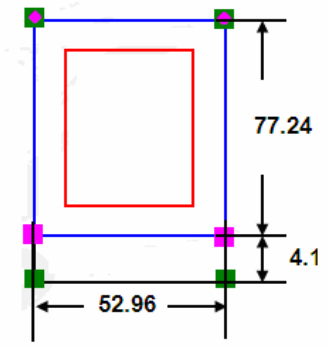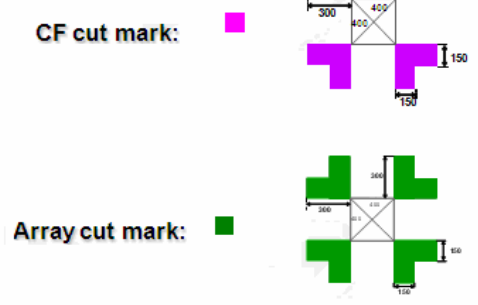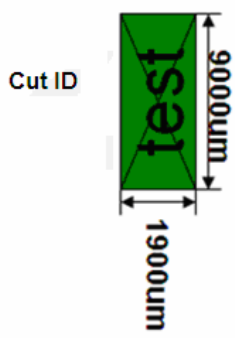
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6.1 Cell Light-On Test Pad Drawing (Shorting bar)
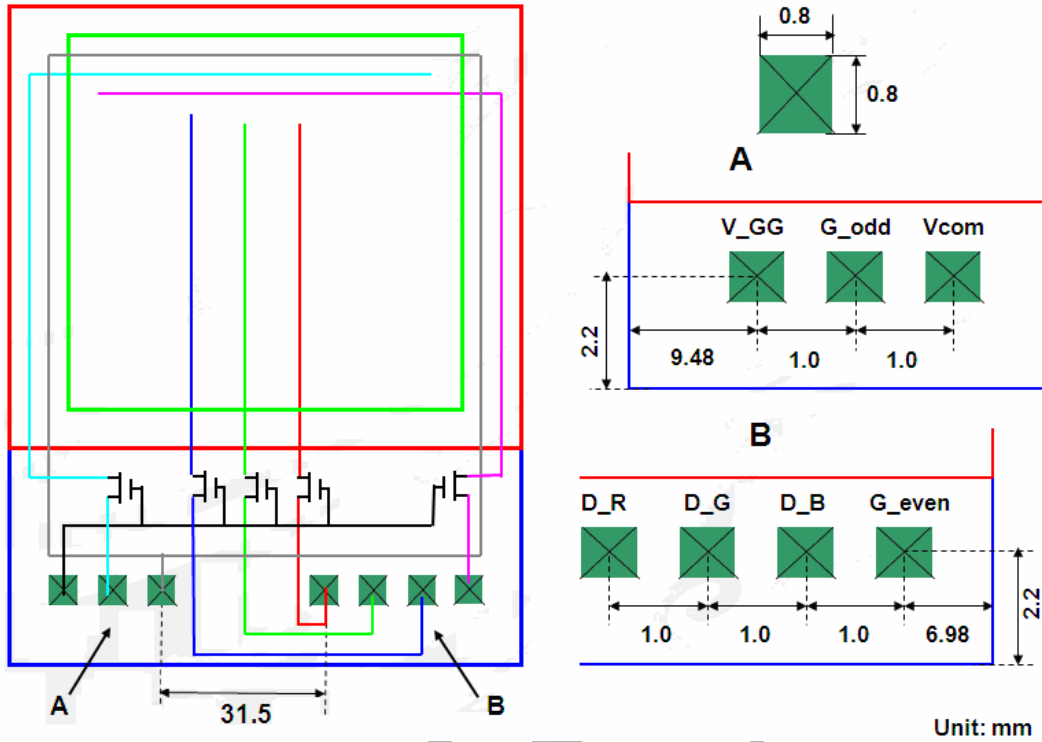
6.2 Gamma Reference Voltage: (HX8357-C)

No	Level	Positive	Negative	Unit
1	L0	3.52988	-3.52988	V
2	L1	3.43512	-3.43512	V
3	L2	3.45881	-3.45881	V
4	L3	3.22190	-3.22190	V
5	L4	2.98500	-2.98500	V
6	L6	2.25060	-2.25060	V
7	L13	2.10845	-2.10845	V
8	L20	1.87155	-1.87155	V
9	L27	2.46381	-2.46381	V
10	L36	1.49250	-1.49250	V
11	L43	1.39774	-1.39774	V
12	L50	1.06607	-1.06607	V
13	L57	1.01869	-1.01869	V
14	L59	0.78179	-0.78179	V
15	L61	0.75810	-0.75810	V
16	L63	0.14214	-0.14214	V

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6.3 Cell Light-On Test Waveform
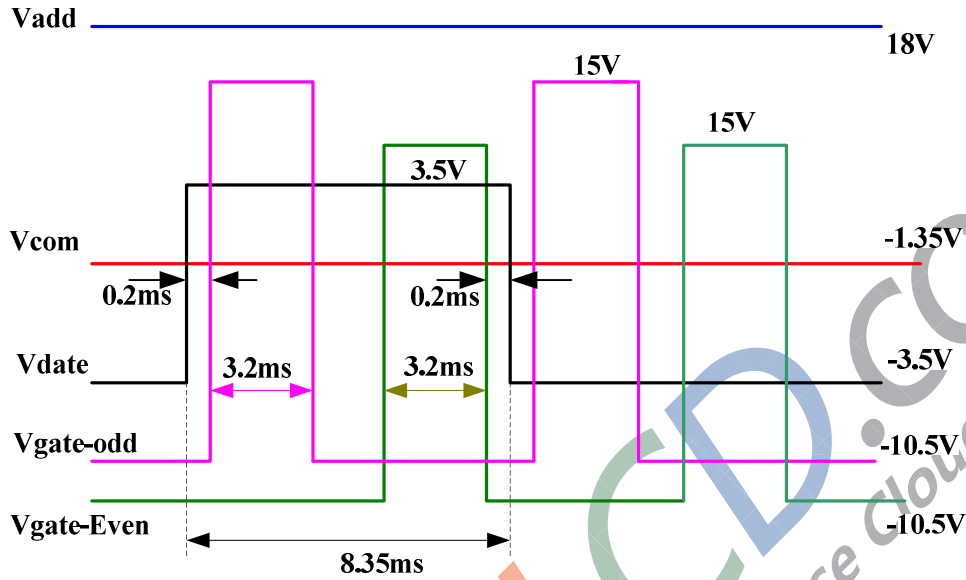
6.4 Vdata Voltage Table

Display	Vdata
Black	Vsig=+3.5V and -3.5V
Gray	Vsig=+1.9V and -1.9V
White	Vsig=+0.2V and -0.2V
Red	VR=+0.2Vand-0.2V
	VG=+3.5V and -3.5V
	VB=+3.5V and -3.5V
Green	VR=+3.5V and -3.5V
	VG=+0.2Vand-0.2V
	VB=+3.5V and -3.5V
Blue	VR=+3.5V and -3.5V
	VG=+3.5V and -3.5V
	VB=+0.2Vand-0.2V

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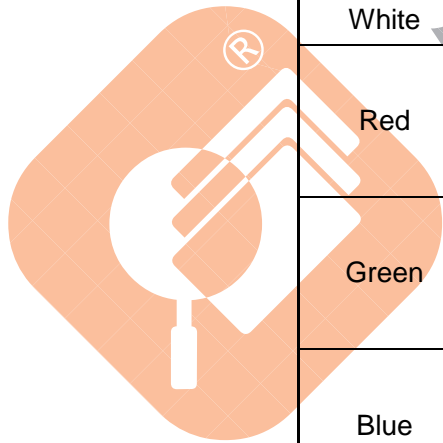
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7 COG+FPC Position On Panel

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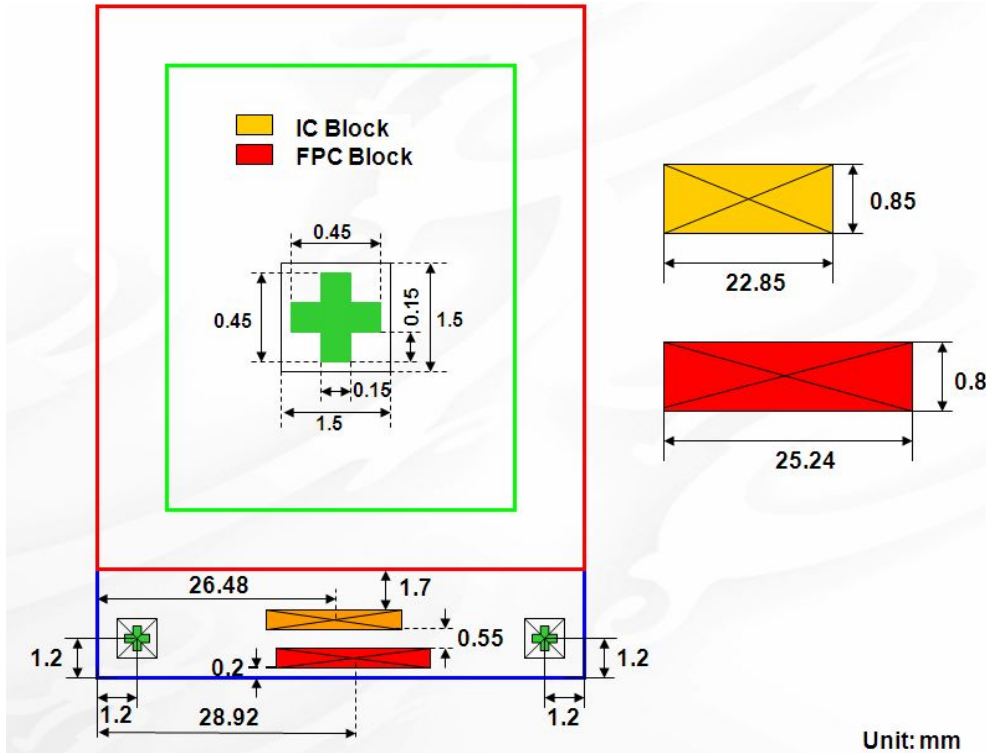
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8 X- FPC Pad Information
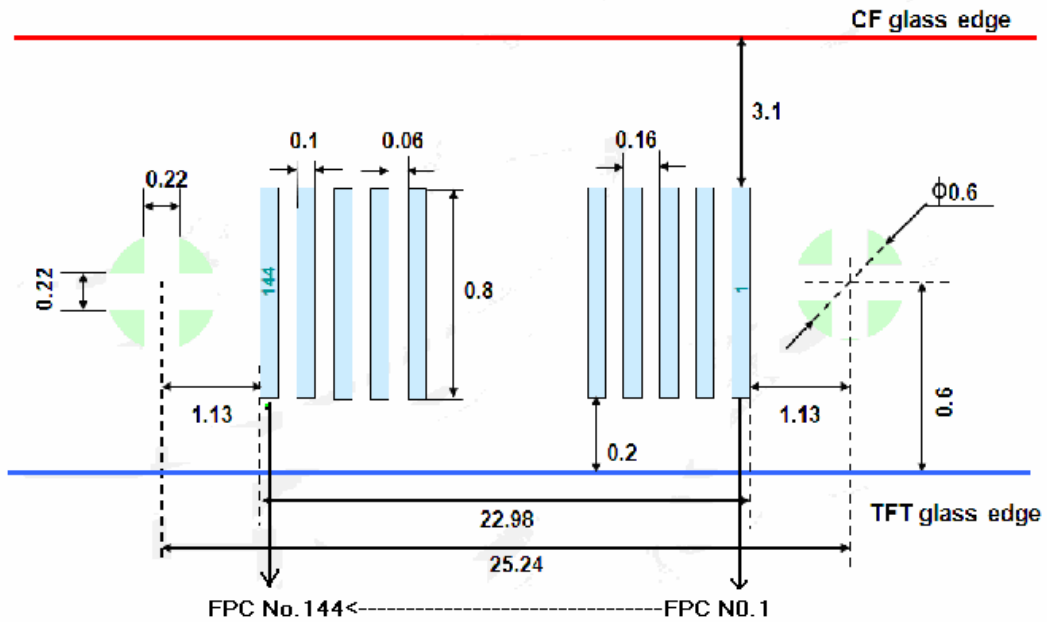
9 Cell Electrode Pin Assignment

IVO InfoVision Optoelectronics (Kunshan)Co., Ltd.
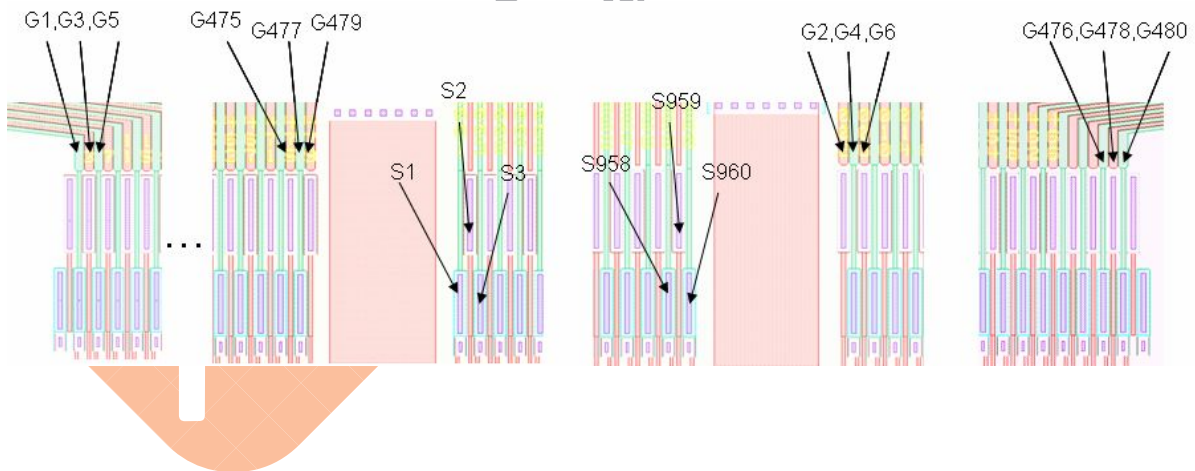
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9.1 FPC Pin assignment (HX8357-C)

Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name
1	VCOM	25	TS3_DB22	49	DB7	73	VSSD	97	C11A	121	C12B
2	VCOM	26	TS2_DB21	50	DB6	74	VSSD	98	C11A	122	C12B
3	VCOM	27	TS1_DB20	51	DB5	75	VCOM	99	C11A	123	C12A
4	VPG	28	TS0_DB19	52	DB4	76	VCOM	100	C11A	124	C12A
5	VPG	29	SD_DB18	53	DB3	77	VCOM	101	CX11B	125	C12A
6	VSSD	30	CM	54	DB2	78	VCOMH	102	CX11B	126	C21B
7	VSSD	31	IM0	55	DB1	79	VCOMH	103	CX11B	127	C21B
8	CABC_ON	32	IM1	56	DB0	80	VCOML	104	CX11B	128	C21B
9	CABC_PWM1	33	IM2	57	DOUT	81	VCOML	105	CX11A	129	C21B
10	TESTO3	34	RESX	58	DIN_SDA	82	VREG1OUT	106	CX11A	130	C21A
11	TESTO4	35	VSYNC	59	RDX	83	VREG1OUT	107	CX11A	131	C21A
12	TESTO5	36	HSYNC	60	WRX_SCL	84	VCL	108	CX11A	132	C21A
13	HSI_LDO	37	PCLK	61	DCX	85	VCL	109	VGL	133	C21A
14	HSI_LDO	38	DE	62	CSX	86	DDVDH	110	VGL	134	C22B
15	HSI_LDO	39	DB17	63	TE	87	DDVDH	111	VGL	135	C22B
16	HSI_CP	40	DB16	64	IOVCC	88	VCI1	112	VGL	136	C22B
17	HSI_CP	41	DB15	65	IOVCC	89	VCI1	113	VSSD	137	C22B
18	HSI_CN	42	DB14	66	VDD	90	VCI	114	VSSD	138	C22A
19	HSI_CN	43	DB13	67	VDD	91	VCI	115	VSSD	139	C22A
20	HSI_DP	44	DB12	68	VSSA	92	VCI	116	VGH	140	C22A
21	HSI_DP	45	DB11	69	VSSA	93	C11B	117	VGH	141	C22A
22	HSI_DN	46	DB10	70	VSSA	94	C11B	118	VGH	142	VCOM
23	HSI_DN	47	DB9	71	VGS	95	C11B	119	VGH	143	VCOM
24	TS4_DB23	48	DB8	72	VSSD	96	C11B	120	C12B	144	VCOM

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9.2 FPC Pin description (HX8357-C)

Pad No	Pad Name	Description
1	VCOM	The power supply of common voltage in TFT driving. Conncet the pin to the common electrode in TFT panel.
2	VCOM	
3	VCOM	
4	VPG	Power supply pin used in OTP program mode and operates at 7.5V ± 0.2. If not in OTP program mode, please let it open.
5	VPG	
6	VSSD	Digital ground.
7	VSSD	
8	CABC_ON	Connected with B/L circuit.LED Driver Enable signal.If not use, please open the pin.
9	CABC_PWM1	Connect to B/L cricuit/MPU. H_TE=0:CABC B/L control PWM signal output. H_TE=1: Horizontal sync output.
10	TESTO3	Test pin input(internal pull low) If not use, open or connected it to VSSA.
11	TESTO4	
12	TESTO5	
13	HSI_LDO	Connect to stabilizing Capacitor beween HIS_VSS and HSL_VSSLDD. High speed interface regulator output pin. If not use,open the pins.
14	HSI_LDO	
15	HSI_LDO	
16	HSI_CP	DSI Host,High speed interface clock differential signal input/output pins. If not use,open the pins or connect to VSSA.
17	HSI_CP	
18	HSI_CN	MDDI Host,High speed interface clcok differential signal input/output pins. If not use,open the pins or connect to VSSA.
19	HSI_CN	
20	HSI_DP	DSI Host,High speed interface data differential signal input/output pins. If not use,open the pins or connect to VSSA.
21	HSI_DP	
22	HSI_DN	MDDI Host,High speed interface data differential signal input/output pins. If not use,open the pins or connect to VSSA.
23	HSI_DN	

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Pad No	Pad Name	Description
24	TS4_DB23	24-bit bi-directional data bus. The unused pins let to open or connected to VSSD.
25	TS3_DB22	24-bit bi-directional data bus. The unused pins let to open or connected to VSSD.
26	TS2_DB21	
27	TS1_DB20	
28	TS0_DB19	
29	SD_DB18	
30	CM	Change the displayed number of colors
31	IM0	System internal select.If not use, fix the pin to IOVCC or VSSD level.
32	IM1	
33	IM2	
34	RESX	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
35	VSYNC	Vertical synchronizing signal in DPI interface. Let to open or connected to VSSD.
36	HSYNC	Horizontal synchronizing signal in DPI interface. Let to open or connected to VSSD.
37	PCLK	Pixel clock
38	DE	Data Enable
39~56	DB0~DB17	24-bit bi-directional data bus. The unused pins let to open or connected to VSSD.
57	DOUT	Serial data output.
58	DIN_SDA	Serial data input
59	RDX	DBI Type-B:mode:Servers as a read signal and read data at the low level.If not use ,Fix it to IOVCC or GND level
60	WRX_SCL	the low level.DBI Type-C:mode:it servers as SCL (Serial clock)If not use,fix it to IOVCC or VSSD.
61	DCX	DBI Type-B,Type-C Option 3: Data/Command selection pin.If not use,fix it to IOVCC or VSSD.

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| Pad No	Pad Name	Description
62	CSX	Low: chip can be accessed High:Chip can not be accessed If not use,fix it to IOVCC.
63	TE	Tearing effect output.If not use,Open the pin.
64	IOVCC	Digital IO Pad power supply.
65	IOVCC	
66	VDD	For internal logic voltage. Connect to a stabilizing capacitor.
67	VDD	
68	VSSA	Analog ground.
69	VSSA	
70	VSSA	
71	VGS	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
72	VSSD	Digital ground.
73	VSSD	
74	VSSD	
75	VCOM	The power supply of common voltage in TFT driving. Conncet the pin to the common electrode in TFT panel
76	VCOM	
77	VCOM	
78	VCOMH	The power supply of common voltage in TFT driving. Conncet the pin to the common electrode in TFT panel.
79	VCOMH	
80	VCOML	The power supply of common voltage in TFT driving. Conncet the pin to the common electrode in TFT panel.
81	VCOML	
82	VREG1OUT	Internal generated stable power for source driver unit.
83	VREG1OUT	
84	VCL	A negative voltage for VCOML circuit, VCL=-VCI
85	VCL	

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Pad No	Pad Name	Description
86~87	DDVDH	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH.
88~89	VCI1	Capacitor connection
90~92	VCI	Capacitor connection
93~96	C11B	Connceted to the Step-up capacitors for step up circuit 1 operation(VSP)
97~100	C11A	Connceted to the Step-up capacitors for step up circuit 1 operation(VSP)
101~104	CX11B	Connceted to the Step-up capacitors
105~108	CX11A	Connceted to the Step-up capacitors
109~112	VGL	A negative power output from the step-up circuit 2 for the gate line drive circuit. Conplct a schottkey barrier diode between VSSA and VGL.
113~115	VSSD	Digital ground.
116~119	VGH	A positive power output from the step-up circuit 2 for the gate line drive circuit.
120~122	C12B	Connceted to the Step-up capacitors for step up circuit 3 operation(VSN)
123~125	C12A	Connceted to the Step-up capacitors for step up circuit 3 operation(VSN)
126~129	C21B	Connceted to the Step-up capacitors
130~133	C21A	
134~141	C22B,C22A	Connceted to the Step-up capacitors for step up circuit 1 operation(VSN)
142~144	VCOM	The power supply of common voltage in TFT driving. Conncet the pin to the common electrode in TFT panel.

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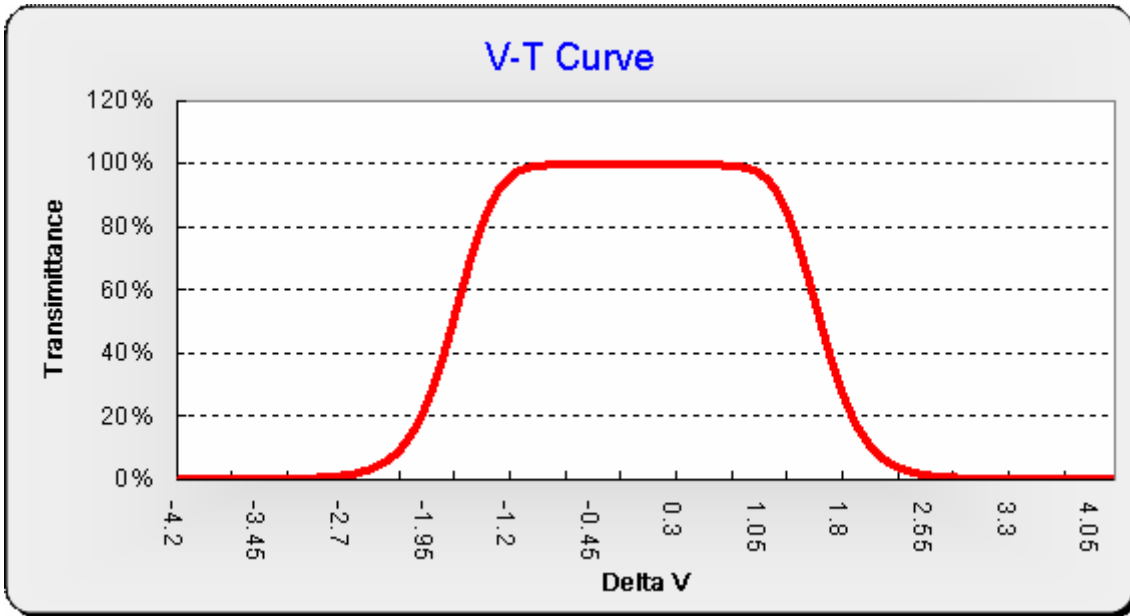| Document Title	C035SWN1-1 Product Information		Page No.	18/23
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9.3 Vcom connect to FPC .
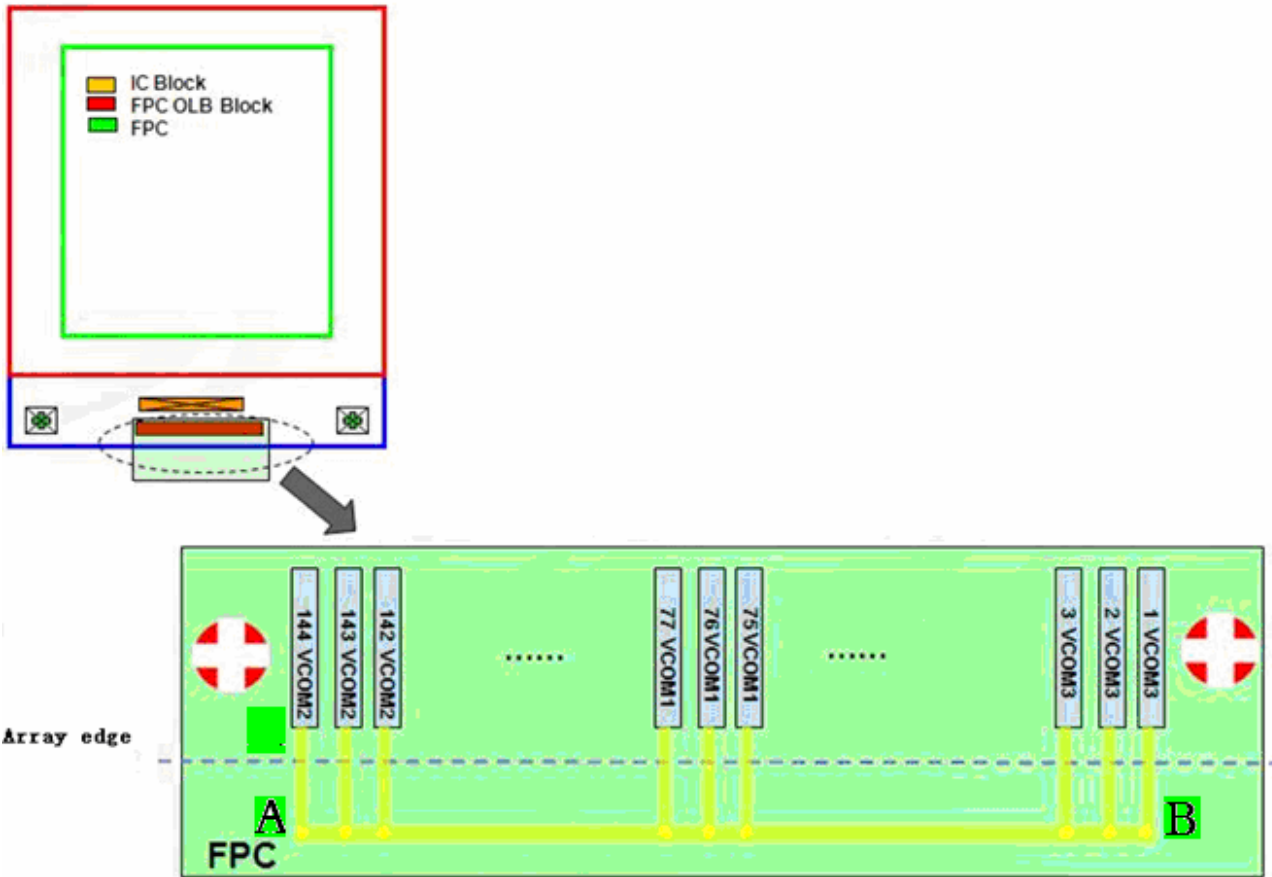
Note:

1. Vcom (NO.1~3,NO.75~77,NO.142~144) must link altogether in FPC, and suggest that from A to B 's resistance should less than 5 ohm.

2. IVO suggest that customer use waterproof material cover pad and the oblique wiring area after bonding ok.

_____
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10 V-T Curve

10.1 V-T Curve (Reference)

10.2 CF Spectrum (Reference)
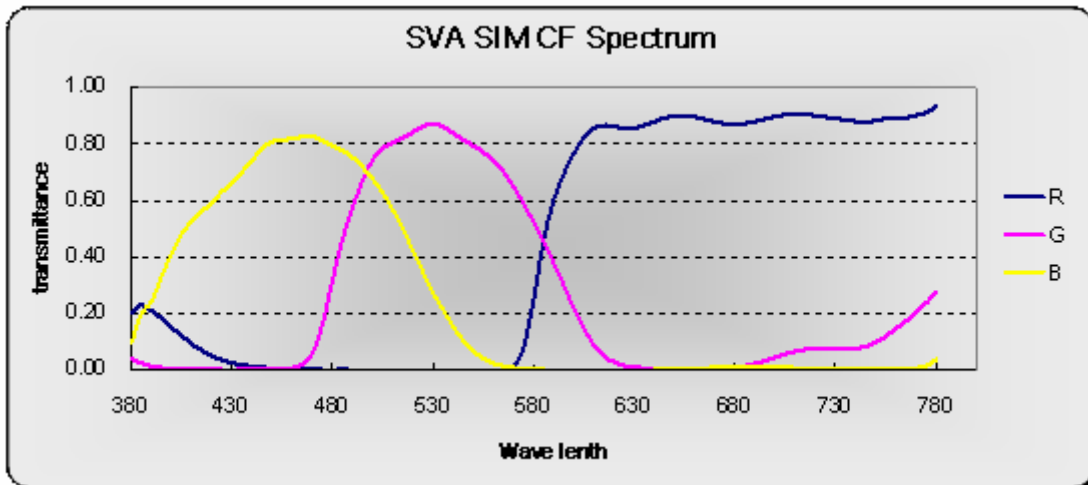
※ Measured at ambient temperature 25℃, under IVO requirement driving condition (refer to see section 11)

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11 IVO Requirement Driving Condition

11.1   Timing Range

Category	Parameter	Unit	Min	Typ	Max
Timings	Frame Rate	Hz	55	60	65
Scanning Method	Gate Scanning Method (single / double)	single			
Line Impedance	Capacitive Load of a Signal Line	pF	24.83	29.79	37.24
	Capacitive Load of a Gate Line	pF	242.76	291.31	364.14
	Resistance Load of Signal Line	KOhm	2.90	4.12	7.08
	Resistance Load of Gate Line	KOhm	2.51	2.99	3.74

11.2   Power Supply Voltage

| No.	Item	MIN	TYP	MAX
1	Vcom voltage(V)	-1.55	-1.35	-1.15
2	Vgl voltage(V)	-9.5	-10.5	-11.5
3	Vgh voltage(V)	14	15	16
4	Vdl voltage(V)	-4	-3.5	-3
5	Vdh voltage(V)	4	3.5	3
6	Vadd(V)	17	18	19
7	Gate line charging time(us)	--	28	--
8	Data line delay closing time(us)	--	3	--
9	Dummy gate line	VCOM	VCOM	VCOM

11.3   OLB Outline

Item \ Driver IC	Source/Gate Driver
Output Channels	960/480
Driver Amount	1
Component Type	COG
OLB Pad Pitch	15um/15um

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11.4 Driver Recommendation

Driver Supplier and Model No.	Driver IC
	ILI9486/HX8357B/HX8357C

12 Back light Spectrum (Reference)

S0351 BL spectrum

IVO

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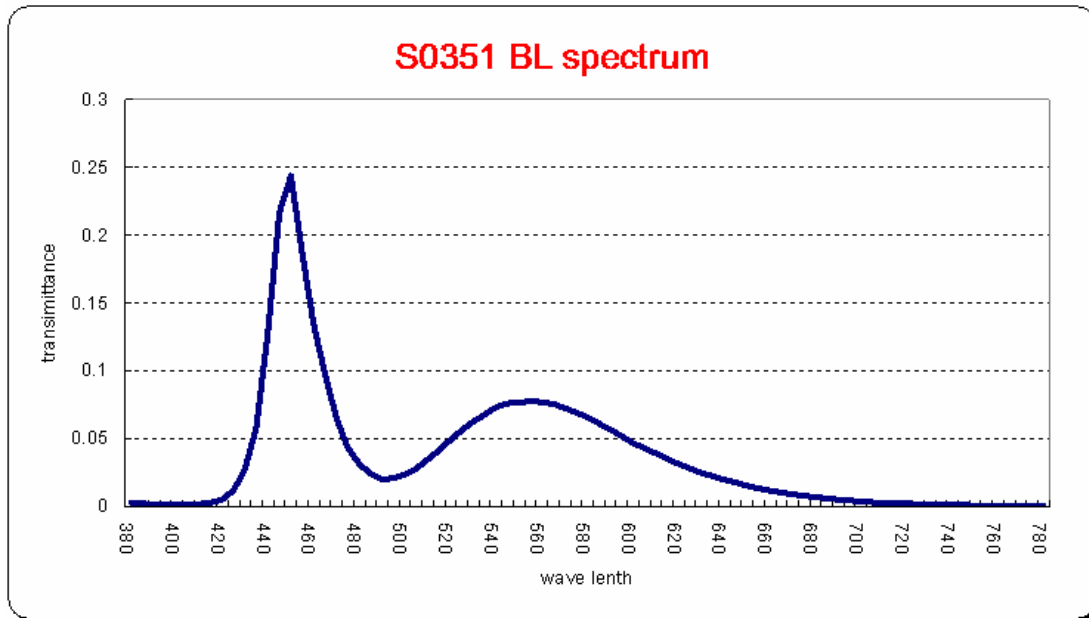
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13 IVO Recommended Cell Packaging

50chips cell packaging :

Cell :5Pcs
Pink EPE:6Pcs
Top PP-Board:1Pcs
Bottom PP-Board:1Pcs

1Pcs Bottom PP-Board

Cell :5Pcs
Pink EPE:6Pcs

Top PP-Board

Put Tape on the
Top PP-Board

Vacuum Bag

Put it in the
Vacuum Bag

Tape

Vacuum-Packed

Put the Vacuum Bag
in the carton

800

1100

IVO InfoVision Optoelectronics (Kunshan)Co., Ltd.
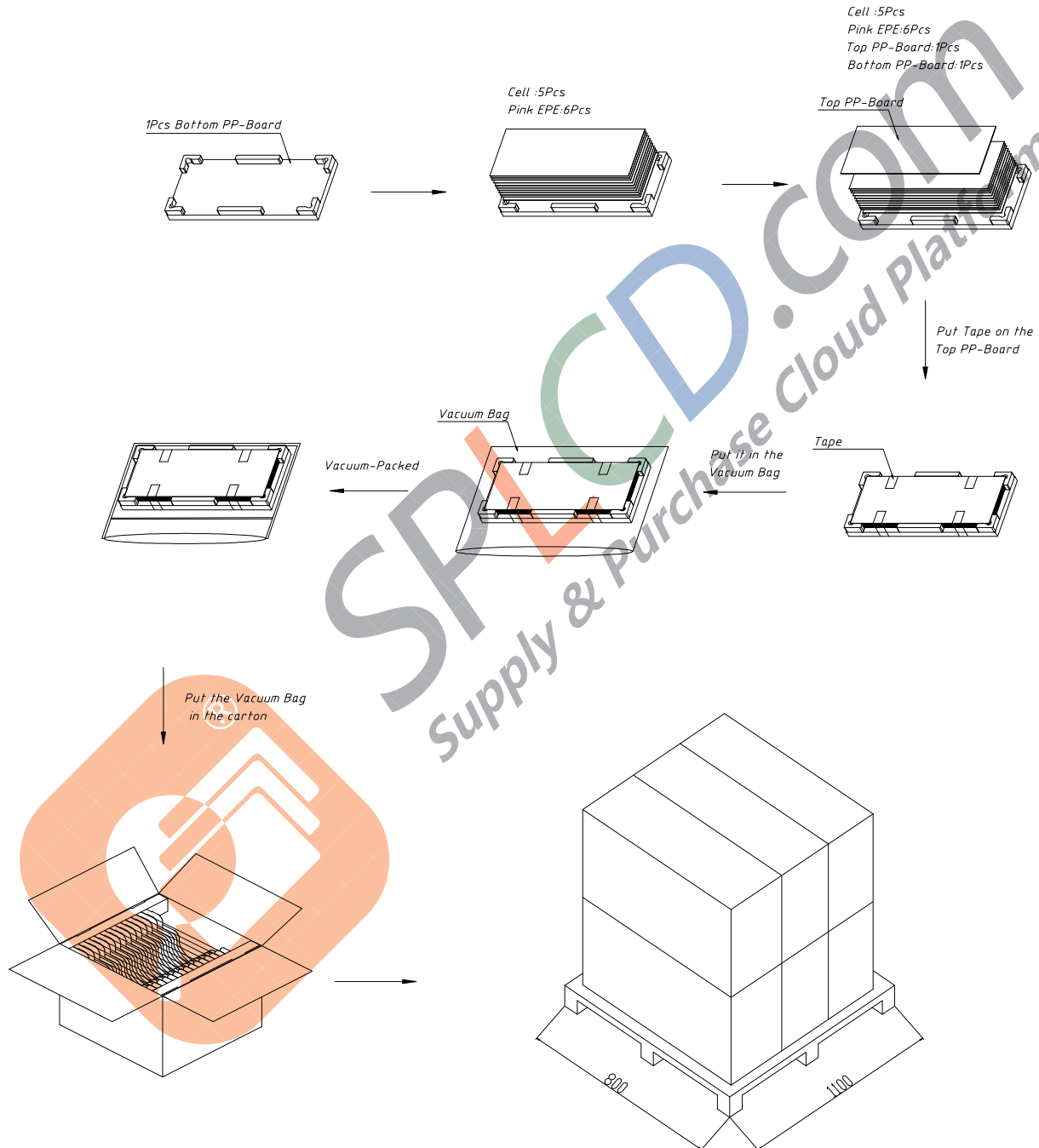
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14 Storage Precaution

(1) Please do not leave cell in the environment of high humididy and high temperature for long time.

(2) IVO suggests to assembly the cell to LCD module in one month after cut into single chip.

(3) The Cell should be stroed in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.