

Silicon NPN Power Transistors

2SC1030

DESCRIPTION

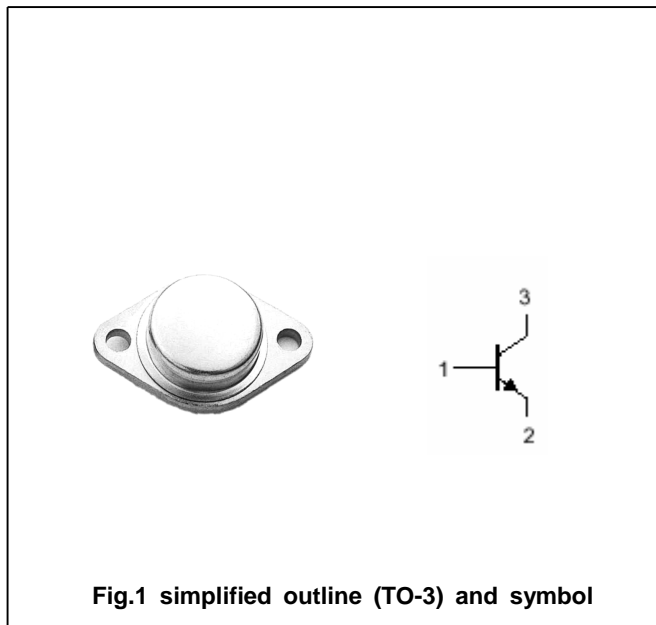
- With TO-3 package
- Wide area of safe operation

APPLICATIONS

- For low frequency power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

**Absolute maximum ratings(Ta=?)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	150	V
V_{CEO}	Collector-emitter voltage	Open base	80	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		6	A
P_C	Collector power dissipation	$T_C=25^\circ$	50	W
T_j	Junction temperature		150	?
T_{stg}	Storage temperature		-55~150	?

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CHARACTERISTICS

T_j=25° unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =0.1A ; I _B =0	80			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =1mA ; I _E =0	150			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =5A; I _B =1A			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =100V; I _E =0			0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			0.1	mA
h _{FE-1}	DC current gain	I _C =1A ; V _{CE} =5V	35		200	
h _{FE-2}	DC current gain	I _C =5A ; V _{CE} =5V	22			
f _T	Transition frequency	I _C =1A ; V _{CE} =5V		10		MHz

U h_{FE-1} classifications

A	B	C
35-70	60-120	100-200

PACKAGE OUTLINE

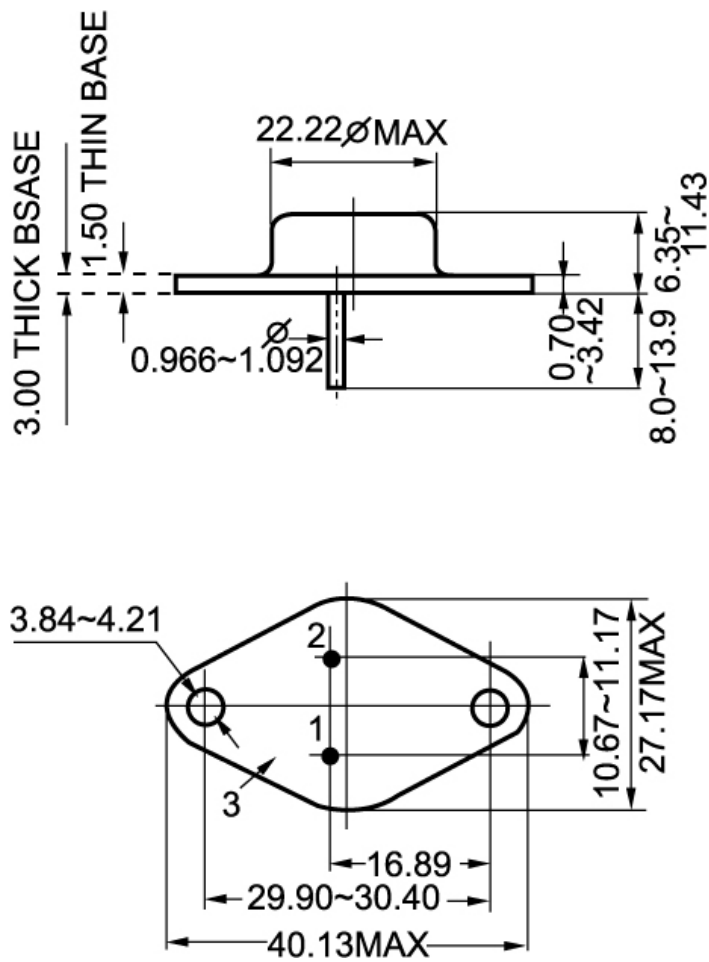


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)