C2163PX2 Datasheet

Primary Sensing SMPS Controller For Adapter Applications

C2163PX2
SOT23-6

ADVANTAGES

- Low cost bipolar primary switch driven in a cascode configuration by a LV n-channel MOSFET
- Tight tolerance CV/CC operation
- Low component count
- High efficiency (Energy Star 2.0 compliance with margin)
- Very low no-load power (<100mW for 16W designs)
- Programmable maximum switching frequency
- Programmable output cable compensation up to 10%

FEATURES

- Advanced primary sensing controller achieves true CV/CC output characteristic without opto-coupler
- Full featured protection for over-temperature, input over-voltage, input under-voltage, output short-circuit
- Advanced PFM/PWM control and quasi-resonant switching for increased efficiency
- Natural switching timing jitter spreads RF spectral emissions, eases EMC compliance
- SOT23-6 package

APPLICATIONS

- Adapters for network applications
- Universal standby and auxiliary power supplies
- Set top box power adapters
- Chargers for power tools

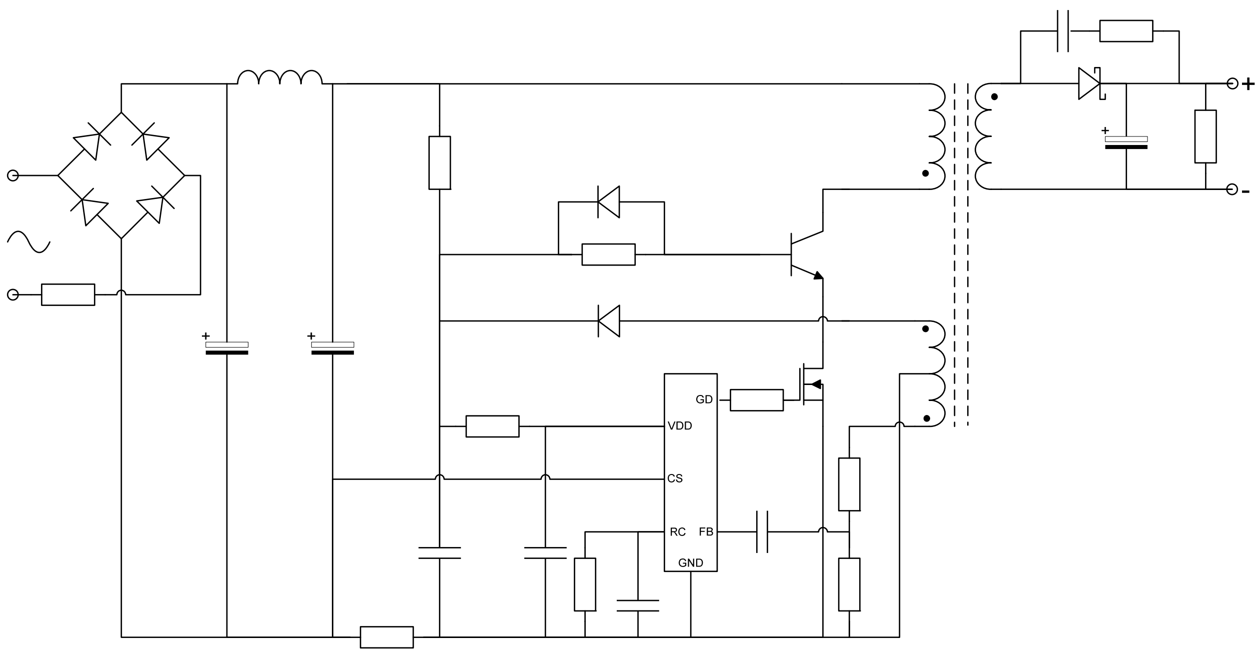

Figure 1: Typical Application Circuit

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BLOCK DIAGRAM

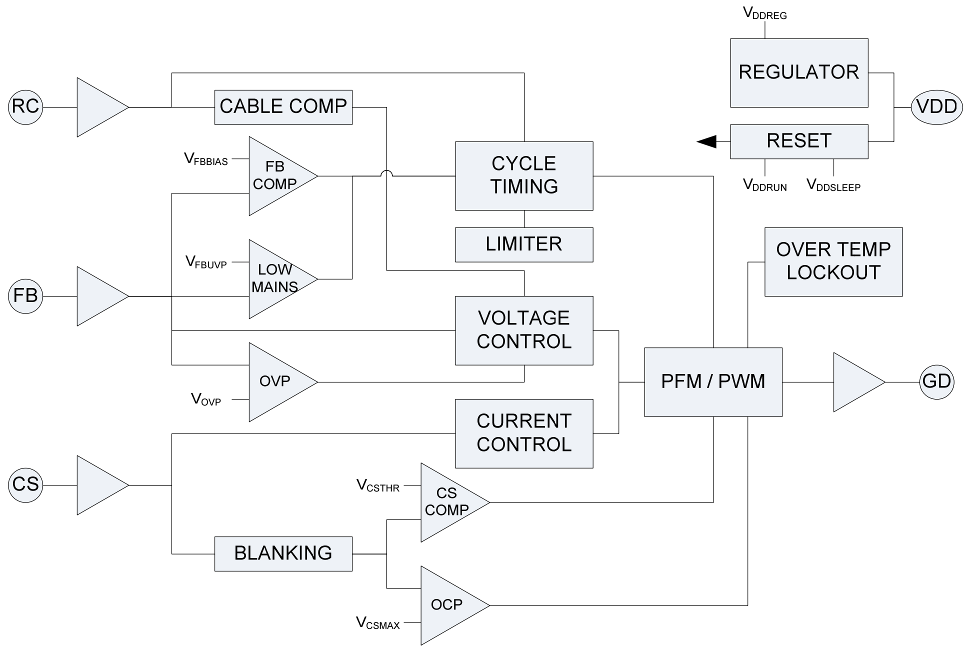

Figure 2: C2163PX2 Block Diagram

PIN DEFINITIONS

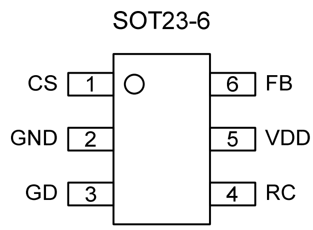

Figure 3: C2163PX2 Pin Assignment

VDD Pin

The VDD pin supplies power to the chip and dictates the operating mode (Run or Sleep).

FB Pin

The FB pin is used to sense the transformer winding voltage waveform, scaled and AC-coupled by an external RC network (Rfb1, Rfb2 and Cfb in Figure 4).

CS Pin

The CS pin senses the primary switch current via the current sensing resistor (Rcs in Figure 4).

RC Pin

The RC timing network connected to the RC pin (shown as Rosc, Cosc in Figure 4) defines both the required maximum switching frequency F_{MAX} and the cable compensation.

GD Pin

The GD pin is connected to the gate of the external MOSFET transistor (Qe in Figure 4).

GND Pin

The GND pin provides the ground reference.

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TYPICAL APPLICATION

The C2163PX2 controller is intended primarily for 12 V adapters, but is equally applicable to other off-line applications up to 16 W requiring low standby power and high efficiency. Higher power applications are possible, limited by component selection required to achieve the necessary power supply specifications. A high degree of configurability allows a wide range of applications to be met at minimum cost. A typical application circuit is shown below.

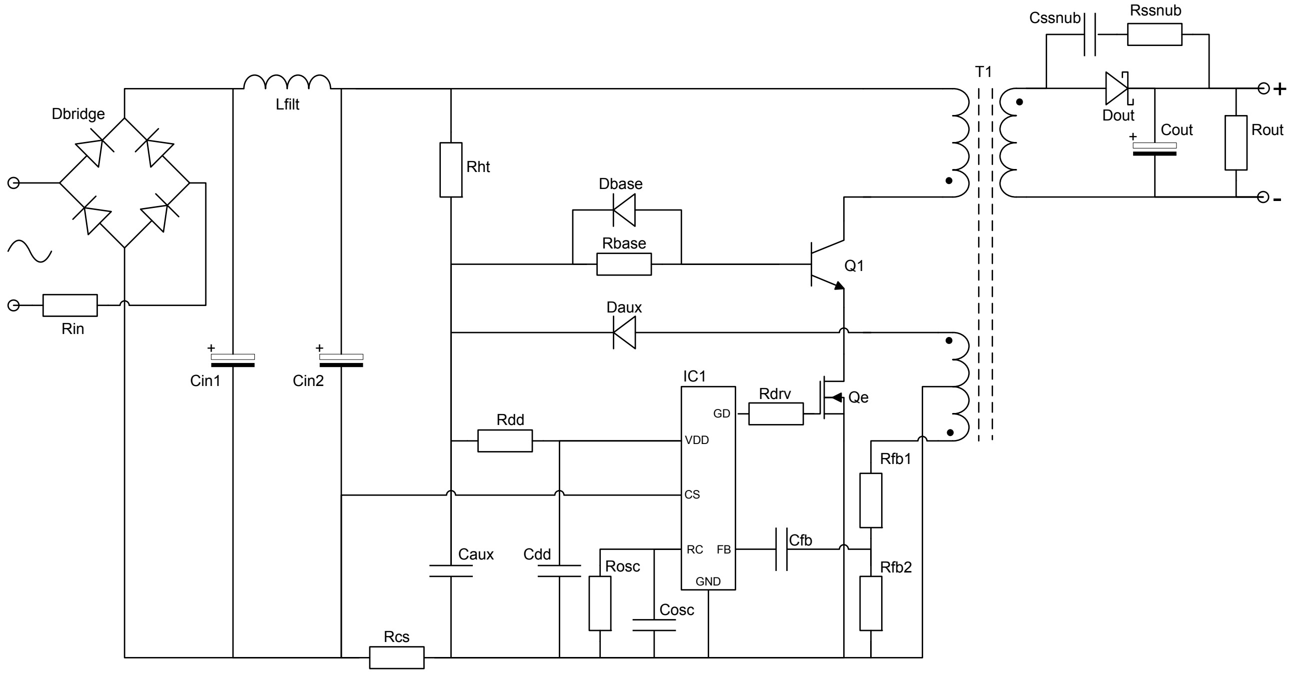

Figure 4: Universal Input 12 W Adapter

Typical 12 W Adapter Performance

Input	V_{IN}	85 - 265 V ac
Output	V_{OUTNOM}	12 V dc (± 5%)
	I_{OUTNOM}	1 A dc (-0/+20%)
Cable compensation	G_{CAB}	2 %
Average Typical Efficiency (including cable)	K_{EFF}	> 80%
No-load input power consumption	P_{NO_LOAD}	< 100 mW
Over-temperature protection (OTP)	T_{SH}	115 ºC
Start-up time	t_{START}	< 2 s

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PRINCIPLE OF OPERATION

Parameters used in equations are explained in the Electrical Characteristics section.

Power-Up/Power-Down Sequences

The C2163PX2 controller is powered via the VDD pin. When the line input is first applied, a small amount of current ($I_{DDSLEEP}$) is drawn from the rectified mains input via a high value start up resistor (Rht in Figure 4). When the voltage on the VDD pin (V_{DD}) reaches a level V_{DDRUN} the controller wakes up, demands more supply current (I_{DDREG}) and enters the Initialise mode (see Figure 5). The controller stays in Initialise for a short time during which internal circuits are enabled and then changes to Run mode. In Run mode, the controller uses an internal shunt regulator to regulate V_{DD} at V_{DDREG}.

If the VDD pin voltage drops $\Delta V_{DDSLEEP}$ below V_{DDREG} the controller goes back into Sleep mode, reducing the supply current demand. The system will restart when input power is restored and V_{DD} reaches V_{DDRUN} again. To achieve a smooth power up sequence the VDD reservoir capacitor (Cdd in Figure 4) needs to be large enough to sustain the supply over the Initialise period and the first few cycles of Run mode, until the auxiliary rail voltage supply is established.

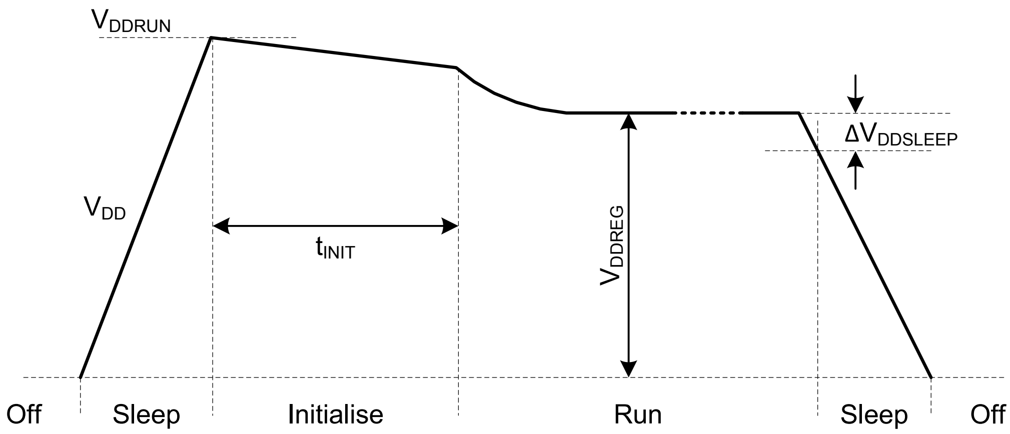

Figure 5: VDD Pin Waveform (V_{DD})

Mode	Description
Sleep	From initial application of power or from Run mode if V_{DD} falls below $\Delta V_{DDSLEEP}$ below V_{DDREG}, the controller changes to Sleep mode. Non-essential controller circuits are powered down and the external switching transistor (Q1) is held off. Exit from Sleep mode occurs when V_{DD} rises above V_{DDRUN} and the controller moves to the Initialise mode.
Initialise	When Initialise mode is entered, internal controller circuits are initialised and two clock cycles are issued, after which the controller changes from Initialise to Run mode.
Run	Converter operation continues. The shunt regulator controls V_{DD} to V_{DDREG}. If V_{DD} falls $\Delta V_{DDSLEEP}$ below V_{DDREG}, the controller ceases power conversion and reverts to Sleep mode.

Table 1: Summary of Controller Modes

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Constant Voltage and Constant Current (CV/CC) Operation

The C2163PX2 controller achieves constant voltage and constant current output within tight limits without the need for any secondary sensing components, by sensing the primary side waveforms of transformer voltage and primary switch current. Figure 6 shows the output characteristics of a typical adapter implemented with the C2163PX2.

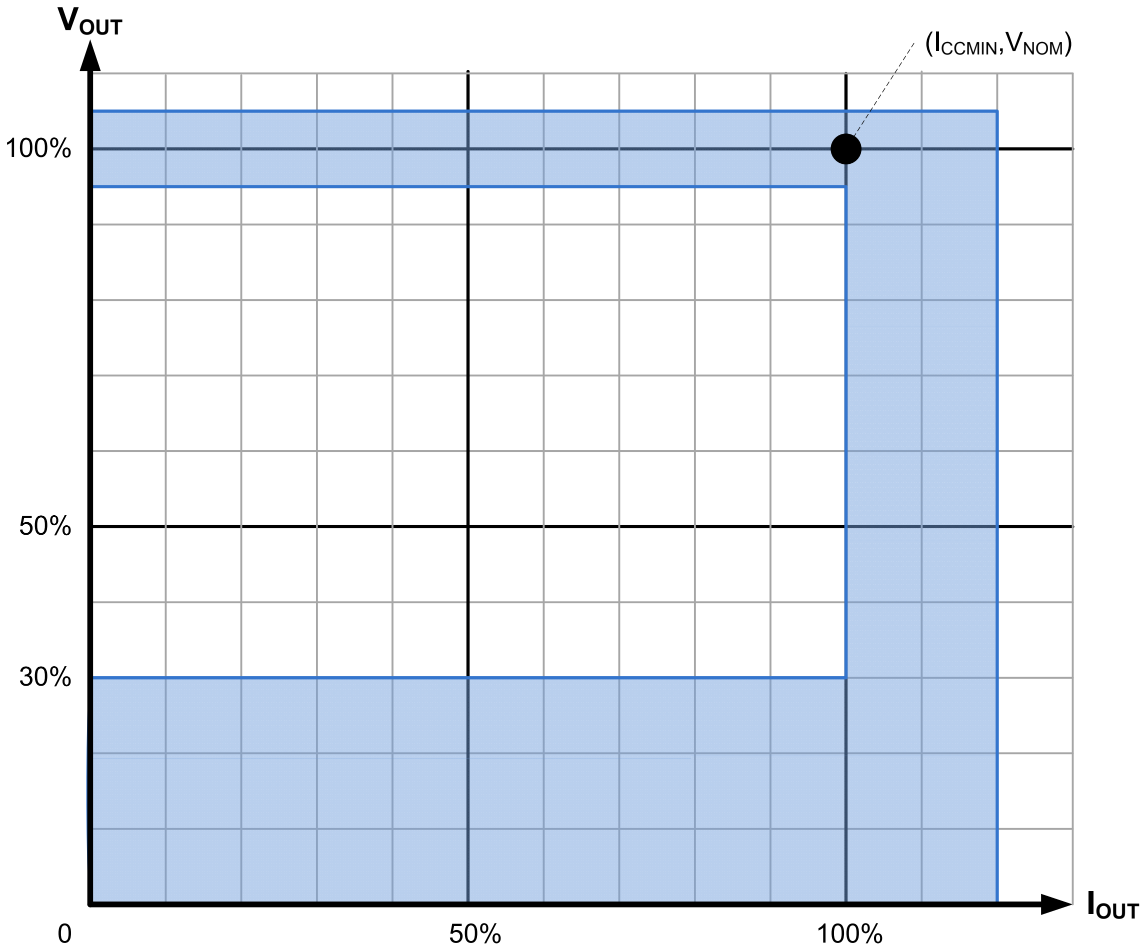

Figure 6: Achievable Adapter Output Characteristic Using C2163PX2

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Switching Waveforms

Typical switching waveforms for the FB, CS and RC inputs are shown with the GD output in Figure 7.

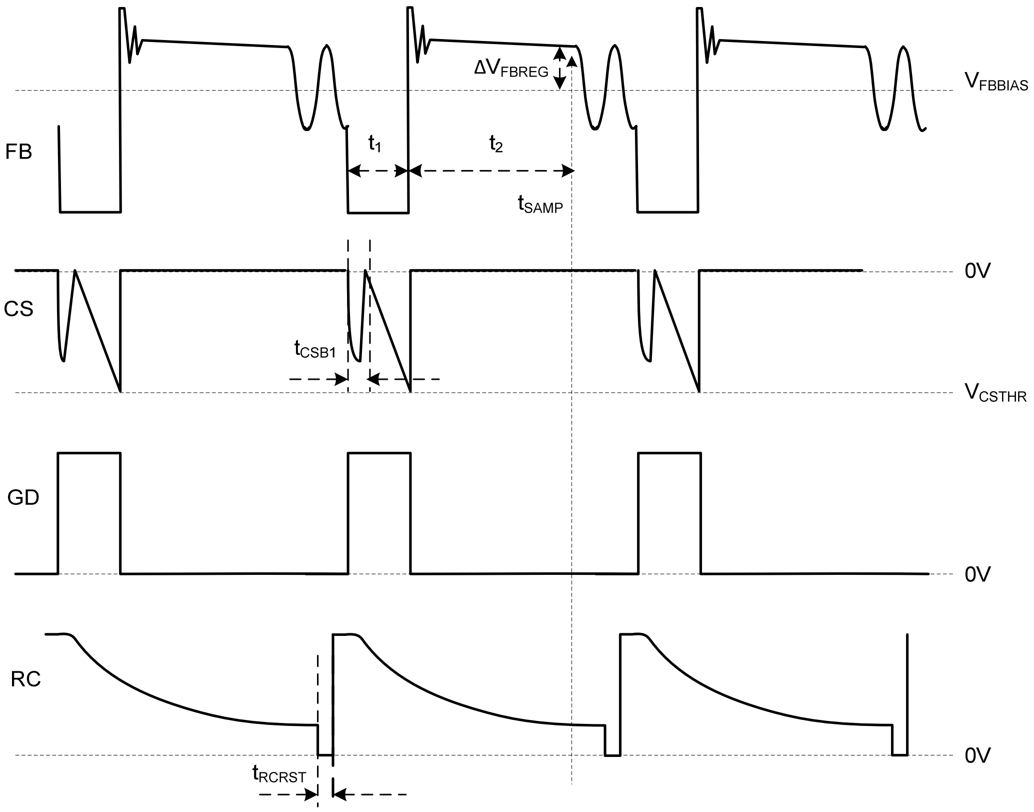

Figure 7: Typical Waveforms: GD, FB, CS, RC pins

Constant Voltage (CV) Regulation

Constant voltage regulation is achieved by sensing the FB input, which is AC coupled to the auxiliary winding of the transformer, as shown in Figure 4. The FB pin is internally biased to V_{FBBIAS}. A typical voltage waveform seen on this pin is shown in Figure 7.

The waveform is analysed and sampled at t_{SAMP} to derive an estimate of the reflected output voltage. The t_{SAMP} point is identified by the change in slope of the transformer auxiliary winding waveform (as sensed by the FB input) immediately prior to the zero crossing. The difference between the sampled voltage and the FB regulation voltage (ΔV_{FBREG}) is used to derive the system power demand and close the voltage control loop.

The regulated output voltage is determined by the selection of the potential divider resistors (Rfb1, Rfb2 in Figure 4) and the chosen transformer turns ratio. The total parallel combination of these resistors should be typically less than 120 Ω to prevent unwanted effects of stray capacitance. The tolerances of Rfb1 and Rfb2 affect output voltage regulation and would typically be chosen to be 1% or better. Values of Rfb1, Rfb2 and Cfb are given by the equations:

$$Rfb2 = 120\ \Omega$$

$$Cfb = 47nF \pm 20\%$$

$$Rfb1 = \frac{Rfb2\left(V_{OUTNOM}\frac{N_F}{N_S} - \Delta V_{FBREG}\right)}{\Delta V_{FBREG}}$$

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Constant Current (CC) Regulation

The current flowing through the transformer primary winding is sensed on the CS pin by the voltage generated across the current sensing resistor (Rcs in Figure 4). The voltage seen on the CS pin is a negative-going voltage waveform as shown in Figure 7. When the voltage on the CS pin exceeds a (negative) threshold V_{CSTHR}, the primary switching transistor is rapidly turned off. The internal loop controller regulates the CS voltage threshold (V_{CSTHR} in Figure 7) between V_{CSMIN} and V_{CSMAX}, based on the average CS input voltage and CC regulation set point (V_{CSCC}) to achieve constant output current regulation. Blanking is provided for a period of t_{CSB1} to prevent false triggering due to leading edge spikes in the waveform.

Constant Current regulation is determined by the transformer turns ratio and the value of Rcs. The value of Rcs is determined by the required output current (I_{OUT}) and transformer primary-secondary turns ratio (N_P/N_S) according to the approximation:

$$Rcs \approx \left(\frac{N_P}{N_S}\right)\left(\frac{V_{CSCC}}{I_{OUT}}\right)$$

The tolerance of Rcs has a direct relationship to the accuracy of the output current limit and is typically chosen to be 1%.

Cable Drop Compensation

The C2163PX2 controller adjusts the output voltage of the power supply to compensate for the voltage drop seen in the output cable. The amount of compensation applied (G_{CAB}) is programmed by the value of the capacitor connected to the RC pin, (Cosc in Figure 4) according to the equation:

$$Cosc = \frac{K_{CAB}}{G_{CAB}}$$

Drive Pulse and Frequency Modulation

The C2163PX2 controls both the primary switch peak current and the switching frequency in response to the power demanded by the application load. The controller ensures that power conversion is performed in discontinuous conduction mode (DCM) at all times. The switching frequency is varied depending on the actual power demand. The maximum switching frequency is set by F_{MAX}. The C2163PX2 controller does not have a minimum switching frequency. The full-load frequency F_{MAX} (chosen in the range 40 to 66 kHz) is set by the equations:

$$F_{MAX} = \frac{1}{K_{OSC}.\tau_{RCOSC} + t_{RCRST}}$$

The oscillator time constant τ_{RCOSC} is controlled by external components Cosc, Rosc so that:

$$\tau_{RCOSC} = R_{OSC}.C_{OSC}$$

Duty Cycle Control

The maximum duty cycle is set by the primary-secondary turns ratio (N_P/N_S) of the transformer (typically 6.7:1 for a 12 V output). For a typical universal input offline application, a maximum duty cycle of 50% is chosen for the minimum rectified supply voltage (typically 80 V_{DC}).

Soft Switching

Zero current (quasi-resonant) switching is used to minimise the switching losses in the primary switch, thereby increasing efficiency and introducing frequency jitter, to spread the RF emissions spectrum. The

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primary switching BJT is turned on when the voltage across it is a minimum (as detected by the FB input), minimising the capacitive switching losses and reducing the RF emissions.

Cascode Switching

The primary switch is connected in cascode configuration with a low voltage logic level MOSFET to ensure fast and efficient switching using low-cost high voltage bipolar transistors, e.g. STX13003, STBV42, TS13003, TS13005, MJE13003, MJE13005. The low voltage logic level MOSFET should have a maximum drain to source voltage, V_{DSS} of 15 - 30 V and low gate capacitance. Suitable MOSFETs include IRLML2402, SSS2202, NDS355.

Fast Load Step Response

When a drop in output voltage is detected due to a large load step from no-load, the controller quickly ramps up output power. This prevents the output voltage from dropping further, as shown in Figure 8. The total voltage drop is determined by the application circuit and the no-load switching frequency (f_{NLP}).

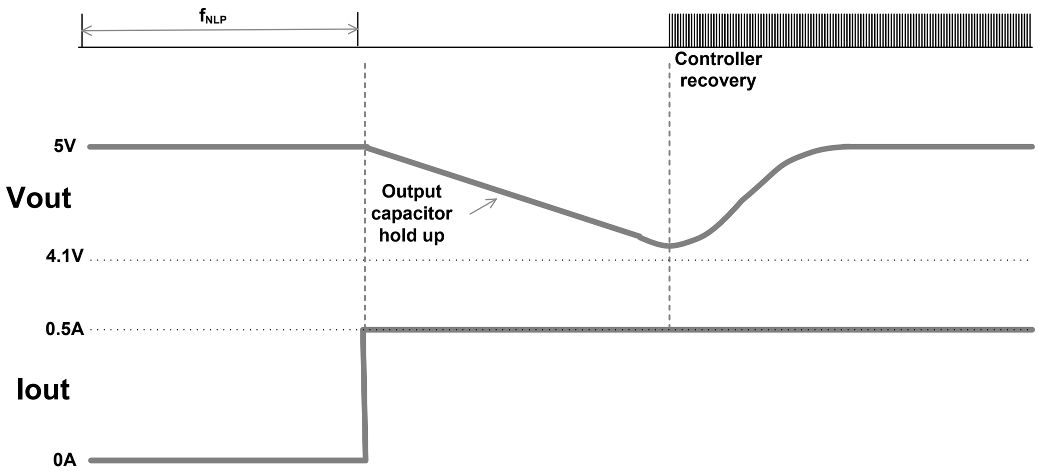

Figure 8: No-load to 0.5 A Load Step Recovery

Protection Features

Short Circuit Protection

In Short Circuit the output current is limited by the constant current regulation of the controller and will follow the adapter output characteristic as indicated in Figure 6.

Mains Under Voltage Protection (UVP) and Over Voltage Protection (OVP)

The regulated output voltage is reduced when the rectified input voltage falls outside the normal working voltage range, defined by V_{UVP} and V_{OVP}. The value is defined by the nominal output voltage (V_{OUTNOM}), the primary-secondary turns ratio (N_P/N_S) and other IC parameters by the equation:

$$V_{UVP} \approx V_{OUTNOM} \frac{N_P}{N_S} \frac{|\Delta V_{FBUVP}|}{\Delta V_{FBREG}} \qquad V_{OVP} \approx V_{OUTNOM} \frac{N_P}{N_S} \frac{V_{FBBIAS}}{\Delta V_{FBREG}}$$

Over Temperature Protection (OTP)

The on-chip OTP is triggered if the junction temperature exceeds the threshold T_{SH}, shutting down the controller. To prevent possible damage to the PCB, the OTP prevents restarting until the temperature has dropped to ($T_{SH} – T_{SHHYST}$).

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Primary Switch Over Current Protection (OCP)

The primary switch is turned off if the primary switch current exceeds a preset threshold V_{CSMAX}, as sensed by the CS input, subject to the minimum on-time T_{ONMIN}. This gives pulse by pulse over current protection.

Output Over Voltage Protection

The switching operation is inhibited when the output voltage is above the nominal range, defined by V_{OUTOVP}. The value is defined by the nominal output voltage (V_{OUTNOM}) and the feedback OVP to regulation level ratio:

$$V_{OUTOVP} = V_{OUTNOM} \cdot G_{FBOVP}$$

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ABSOLUTE MAXIMUM RATINGS

CAUTION: Permanent damage may result if a device is subjected to operating conditions at or in excess of absolute maximum ratings.

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{DD}		-0.5	4.5	V
Supply current	I_{DD}		-20	90	mA
FB input voltage	V_{FB}	DC condition	-0.5	V_{DD} + 0.5	V
CS input voltage	V_{CS}		-0.5	V_{DD} + 0.5	V
RC input voltage	V_{RC}		-0.5	V_{DD} + 0.5	V
GD pin voltage	V_{GD}		-0.5	V_{DD} + 0.5	V
FB input current	I_{FB}		-20	20	mA
CS input current	I_{CS}		-20	20	mA
RC input current	I_{RC}		-35	250	mA
GD pin current	I_{GD}		-150	150	mA
Junction temperature	T_J		-25	125	°C
Storage temperature	T_P		-40	150	°C
Lead temperature	T_L	Soldering, 10 s		260	°C
ESD withstand		Human body model, JESD22-A114		2	kV
		Charged device Model, ANSI-ESD-STM5.3.1		500	V

NORMAL OPERATING CONDITIONS

Unless otherwise stated, electrical characteristics are defined over the range of normal operating conditions. Functionality and performance is not defined when a device is subjected to conditions outside this range and device reliability may be compromised.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		3.1	3.45	3.6	V
Supply current	I_{DD}				30	mA
Full power switching frequency	F_{NOM}	Full-load, application dependent	36	40	66	kHz
Transformer resonance frequency (in-circuit)	F_{RES}		300			kHz
Junction temperature	T_J		-25	25	105	°C

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ELECTRICAL CHARACTERISTICS

Unless otherwise stated:

1. Min and Max electrical characteristics apply over normal operating conditions.
2. Typical electrical characteristics apply at $T_J = T_{J(TYP)}$ and $I_{DD} = I_{DDREG(TYP)}$.
3. The chip is operating in Run mode.
4. Voltages are specified relative to the GND pin.

VDD Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DDRUN}	To enter Initialise mode	3.6	4.0	4.45	V
	V_{DDREG}	In Run mode	3.3	3.45	3.6	V
	$\Delta V_{DDSLEEP}$	To enter Sleep mode (measured relative to V_{DDREG})		-600		mV
Supply current	I_{DDREG}	In Run mode			2.4	mA
	$I_{DDSLEEP}$	In Sleep mode			5.5	μA
Initialisation time	t_{INIT}			$3\tau_{RCOSC}$		s

FB Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FB bias voltage	V_{FBBIAS}	Internal DC bias voltage	1.66		1.84	V
FB regulation level	ΔV_{FBREG}	Measured relative to V_{FBBIAS} T=25°C	394.5	405	415.5	mV
FB slope detection threshold	$\Delta V_{FB}/\Delta t$		-280	-200	-120	mV/μs
FB input resistance	R_{FBIN}	Effective input resistance $0 < V_{FB} < V_{DD}$		50		kΩ
FB initialisation current	I_{FBINIT}	$V_{FB} = 0$ V		-1.8		mA
FB OVP ratio	G_{FBOVP}	Measured relative to V_{FBBIAS}	1.4		1.8	
FB UVP comparator threshold offset	ΔV_{FBUVP}			-135		mV

RC Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Maximum switching frequency	F_{MAX}	220 pF < Cosc < 2.2 nF	30		66	kHz
Maximum frequency control factor	K_{OSC}			0.31		
Cable compensation	G_{CAB}		1		10	%
Cable compensation factor	K_{CAB}			20		pF
Oscillator reset time	t_{RCRST}			2.7	3.8	μs

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CS Pin

Parameter	Symbol	Condition		Min	Typ	Max	Unit
CS input minimum threshold	V_{CSMIN}	Outside CS blanking time t_{CSB1}	Minimum load		-38		mV
CS input maximum threshold	V_{CSMAX}		Over-current protection		-182		mV
CS turn-off response time	t_{CSOFF}		Step ΔV_{CS}: V_{CSMAX} + 10 mV to V_{CSMAX} - 10 mV		175		ns
CS Input Offset	ΔV_{CSOFF}				0		µV
CS Input Leakage Current	I_{CSLEAK}	-0.2 V < V_{CS} < V_{DD}		-10		10	µA
CS input limit for CC operation (average)	V_{CSCC}	F = 40 kHz, $t_1 = t_2$ = 12.5 µs, T=25°C		-32.5	-31.4	-30.3	mV
Leading edge blanking time	t_{CSB1}	See Figure 7			400		ns

GD Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate drive rise time	T_{GDRISE}	C_{GATE} = 1 nF; 10% - 90%		30		ns
Gate drive fall time	T_{GDFALL}			30		ns
Gate sourcing current	I_{SOURCE}	V_{GD} = 2.0 V, V_{DD} = 3.3 V		65		mA
Gate sinking current	I_{SINK}	V_{GD} = 2.0 V, V_{DD} = 3.3 V		75		mA
Minimum on-time	t_{ONMIN}			575		ns

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THERMAL CIRCUIT PROTECTION

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal shutdown temperature	T_{SH}	At silicon junction	105	115	125	°C
Thermal shutdown hysteresis	T_{SHHYST}	At silicon junction		30		°C

PACKAGE THERMAL RESISTANCE CHARACTERISTICS

Conditions:

1. Controller IC mounted on typical PCB (1.6 mm thick, 35 µm copper, CEM1);
2. θ_{JB} measured to pin terminal of device at the surface of the PCB.

Package	Junction-to-board θ_{JB} (Typical)	Junction-to-ambient θ_{JA} (Typical)	Units
SOT23-6	60	170	°C / W

PACKAGING AND ORDERING INFORMATION

Package Marking

The SOT23-6 package is marked with a short code indicating type and production lot as shown in Figure 9.

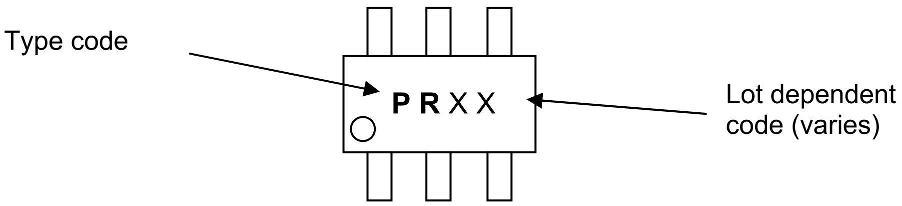

Figure 9: SOT23-6 Package Marking

Ordering

Type	Package	Marking	Packing Form	Shipping
C2163PX2	SOT23-6	PRxx	7" Tape & Reel	C2163PX2-TR7
			13" Tape & Reel	C2163PX2-TR13

For further package and ordering information, please contact CamSemi.

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DATASHEET STATUS

The status of this Datasheet is shown in the footer. Always refer to the most current version.

Datasheet Status	Product Status	Definition
Product preview	In development	The Datasheet contains target specifications relating to design and development of the described IC product. Application circuits are illustrative only. Specifications are subject to change without notice.
Preliminary	In qualification	The Datasheet contains preliminary specifications relating to functionality and performance of the described IC product. Application circuits are illustrative only. Specifications are subject to change without notice.
Product data	In production	The Datasheet contains specifications relating to functionality and performance of the described IC product which are supported by testing during development and production. Application circuits are illustrative only. Specifications are subject to change without notice.

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