C2183

Design Guide

DG-5479-1212

17-Dec-2012

Preliminary

Contents

1 INTRODUCTION

1.1 Purpose

The aim of this design guide is to assist the designer through the steps needed to complete a design using the C2183 power controller. The primary side sensing (PSS) controller is designed to drive an external power MOSFET switch in a Discontinuous Current Mode (DCM) quasi-resonant flyback converter. The block diagram for the IC is shown in Figure 1. A generic circuit diagram of a converter is shown in Figure 2 below. Use this document in conjunction with the C2183 datasheet, which lists the IC parametric values.

The C2183 is a primary sensing switching regulator. It is intended for applications where constant voltage and current operation is required. An example of such output characteristic is shown in Figure 3.

The guide shows the recommended design flow, with calculations for key components, transformer design, PCB design guidelines and other performance parameters considerations. MathCad models showing a design example are referenced to help assist with some calculations. Please consult your CamSemi representative for more information.

1.2 IC Block Diagram

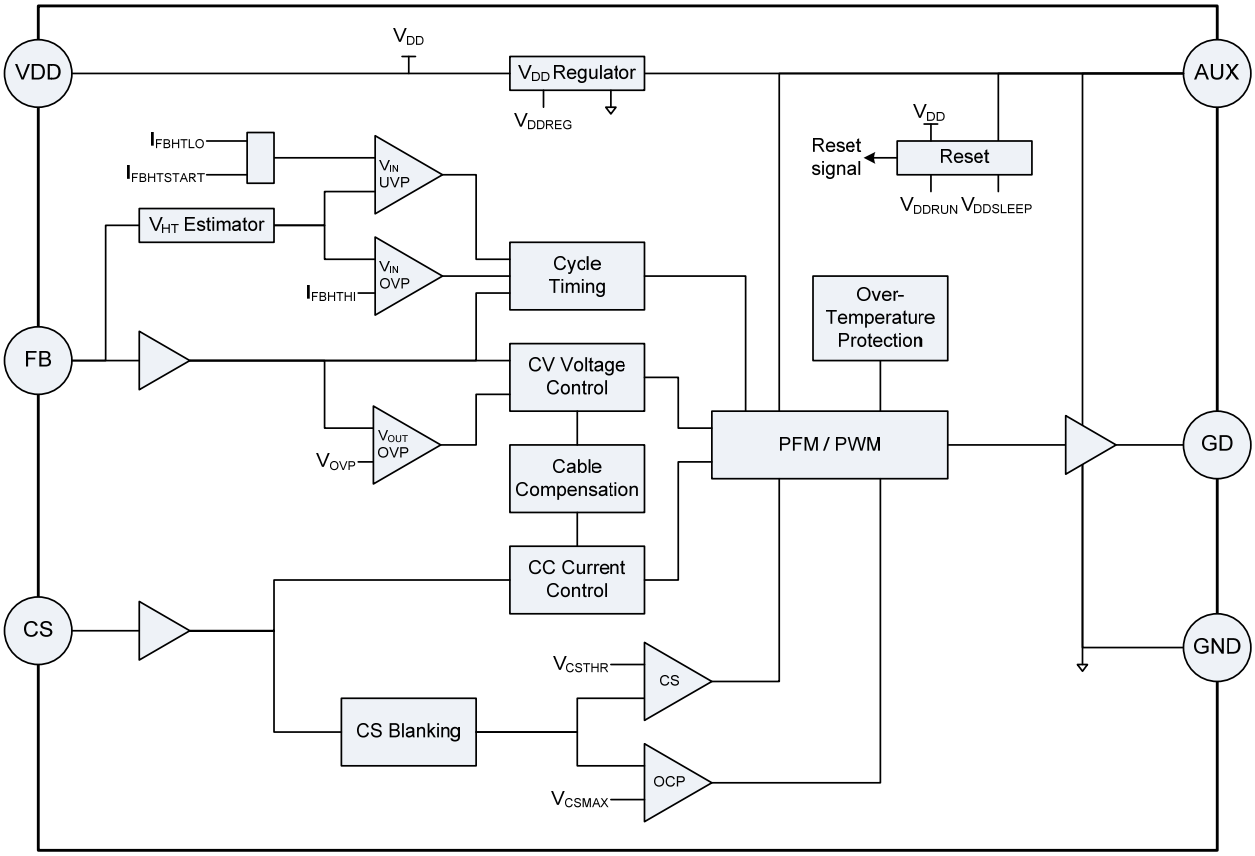

Figure 1: IC Block Diagram

Pin descriptions and IC parameters are included in the datasheet.

1.3 Application Circuit

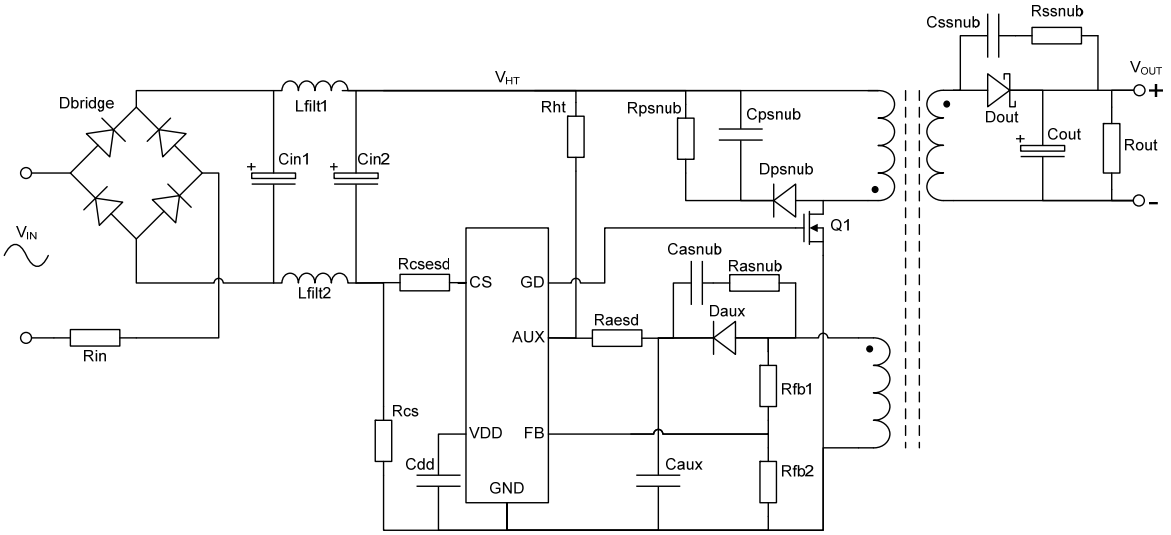

Figure 2: Typical Application Circuit

1.4 Typical Parameters

Parameter	Symbol	Range or Value	Units	Comment
Supply voltage	V_{IN}	85 - 264	Vac	Universal mains
Supply frequency	F_{IN}	47 - 63	Hz	
Output voltage	V_{OUTCV}	12 ± 5%	V	Constant voltage (CV) mode, at the load
Output current	I_{OUTCC}	1 ± 5%	A	Constant current (CC) mode
Switching frequency at full load	f_{MAX}	80	kHz	Determined by the chosen variant
Cable compensation	G_{CAB}	8.0	%	Determined by the chosen variant
No-load power	P_{NL}	< 150	mW	
Average efficiency	η	> 73	%	Energy Star test method
Turn-on delay	$T_{STARTUP}$	< 2	s	

Table 1: Typical Parameters

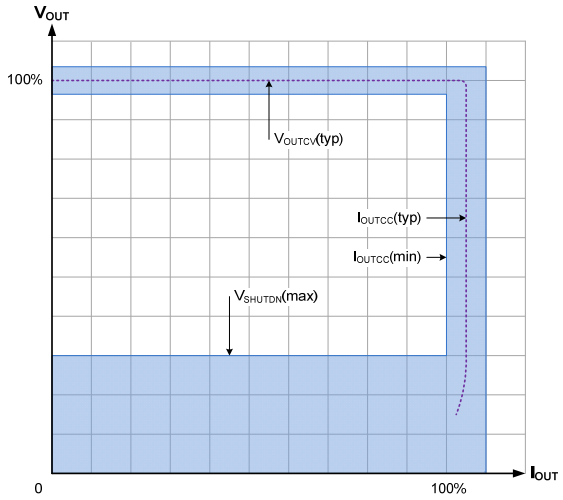

Figure 3: Output VI Characteristics

2 DESIGN FLOW

2.1 Overview

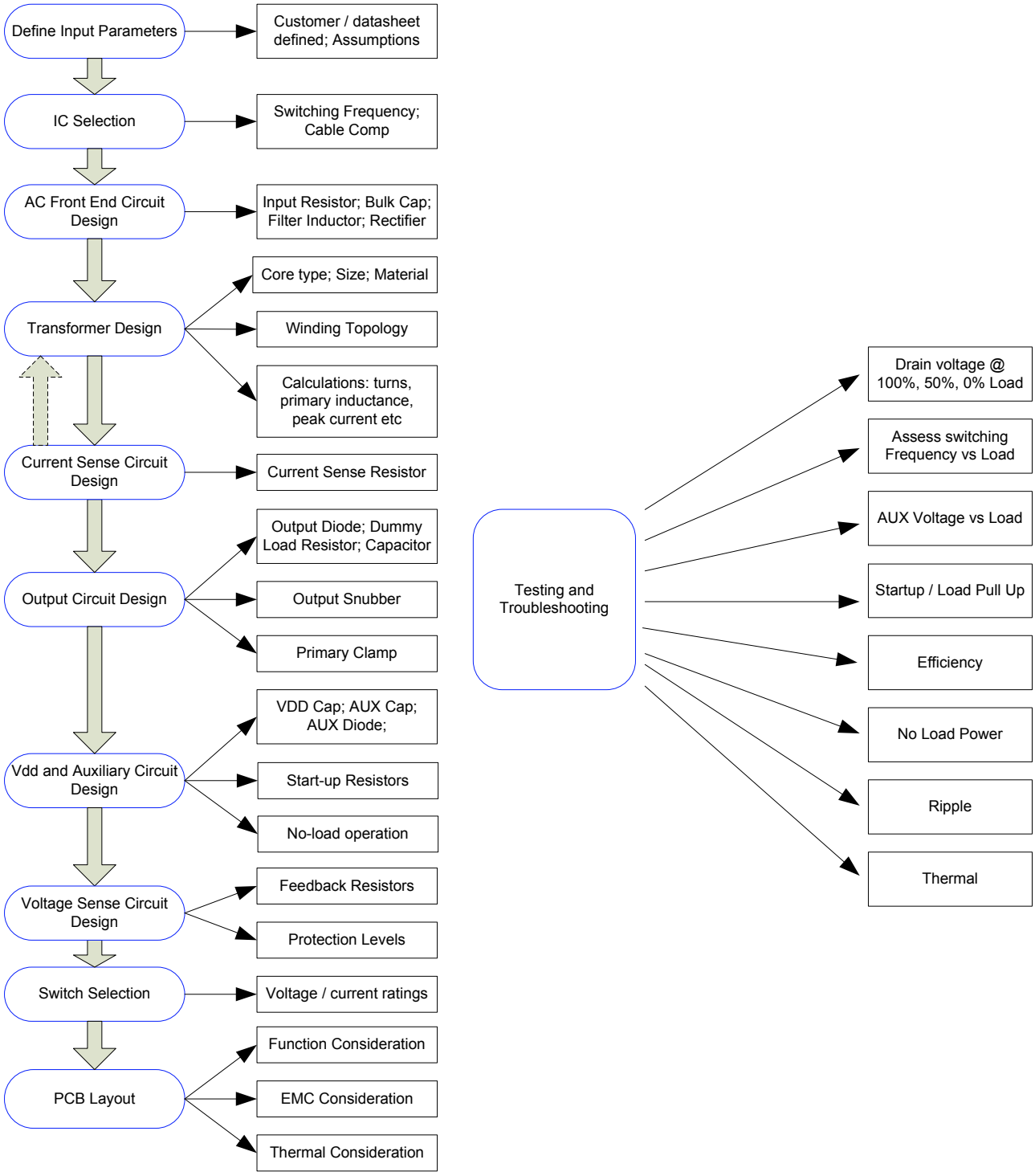

Figure 4: Design Flow Process

2.2 Input Parameters

The following parameters need to be defined for component values to be calculated and performance checks to be made. These are split into customer defined parameters and assumptions. Datasheet parameters are also required and can be found in the latest C2183 datasheet. Design example values are given.

Name	Symbol	Source	Design Example	Comments
Minimum Input AC Voltage	$V_{IN(MIN)}$	Customer defined	90 V	
Maximum Input AC Voltage	$V_{IN(MAX)}$	Customer defined	264 V	
Low Mains Input Voltage	$V_{MAINSLO}$	Customer defined	115 V	
High Mains Input Voltage	$V_{MAINSHI}$	Customer defined	230 V	
Minimum Line Frequency	$F_{IN(MIN)}$	Customer defined	47 Hz	
Output Voltage	V_{OUTCV}	Customer defined	12.0 V	
Output Current	I_{OUTCC}	Customer defined	1.1 A	I_{OUTCC} at least 5% greater than $I_{OUTCC(MIN)}$
	I_{OUTCC}(min)	Customer defined	1.0 A	
Converter Efficiency	η	Customer defined	0.73	
Cable Resistance	R_{CABLE}	Customer defined	0.134 Ω	
Primary Switch Voltage Rating	V_{DSMAX}	Customer defined	700 V	
Primary Switch Derating	ΔV_{FET}	Customer defined	0.1	10% de-rating
Min Core Cross-Sectional Area	Aemin	Customer defined	23 mm^2	
Load Step Voltage Undershoot	V_{USHOOT}	Customer defined	4.1 V	
Load Step Current Requirement	$I_{LOADSTEP}$	Customer defined	0.5 A	
Voltage Regulation Tolerance	K_{CVTOL}	Assumption	1.05	
Current Regulation Tolerance	K_{CCTOL}	Assumption	1.05	
CC Design Margin	$K_{CTRLTOL}$	Assumption	0.15	To account for K_{LPTOL} and K_{FTOL}
Primary Inductance Tolerance	K_{LPTOL}	Assumption	0.10	+/-10% estimated
Operating Frequency Tolerance	K_{FTOL}	Assumption	0.10	+/-10% estimated
Input Capacitance Tolerance	K_{CINTOL}	Assumption	0.10	+/-10% estimated
Transformer efficiency	η_{TX}	Assumption	0.96	
No-load efficieincy	η_{NL}	Assumption	0.80	
Transformer resonant frequency	f_{TX}	Assumption	800 kHz	
Minimum Input DC Voltage	V_{DCMIN}	Assumption	80 V	Determines $V_{INREGMIN}$
Output Diode Voltage	V_{Dout}	Assumption	0.3 V	
Auxiliary Diode Voltage	V_{Daux}	Assumption	0.7 V	
Full-load Core Flux Density	B_{FL}	Assumption	300 mT	Gives starting point
Current Regulation Accuracy	K_{CS}	Assumption	1	
Output Diode De-rating	ΔV_{Dout}	Assumption	0.25	25% de-rating
Switch Turn-off Overshoot	V_{OVER}	Assumption	120 V	
Maximum Switching Frequency	f_{MAX}	Datasheet variant	80 kHz	
Cable compensation	K_{GCAB}	Datasheet variant	1.08	8%

Table 2: Input Parameters

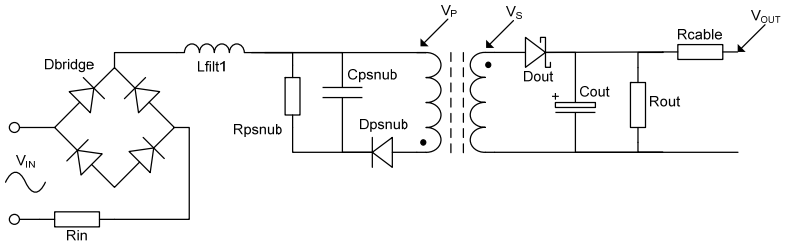

Figure 5: Calculated Voltage Points in Circuit

Based on these parameters the following calculations can be made, which are used in later stages.

Secondary voltage in CV mode: $V_{SCV} = (V_{OUTCV} \cdot K_{GCAB}) + V_{Dout}$

Secondary power during full-load: $P_{SFL} = (V_{OUTCV} \cdot K_{GCAB} \cdot I_{OUTCC}) + (V_{Dout} \cdot I_{OUTCC})$

Input power during full-load: $P_{INFL} = \frac{P_{OUTFL}}{\eta}$ Primary power during full-load: $P_{PFL} = \frac{P_{SFL}}{\eta_{TX}}$

NB power losses in the transformer secondary and primary, the input and output capacitor ESR, the auxiliary and primary clamp, and the MOSFET switching and conduction losses have not been considered.

2.3 IC Selection

Refer to the datasheet for the list of C2183 variants available.

2.3.1 Operating Switching Frequency (f_{MAX})

The maximum switching frequency is preset in each variant of C2183. For a chosen variant, the switching frequency is fixed. No external components are required to set the switching frequency.

In general, a lower f_{MAX} will ensure better efficiency, but will require a larger transformer size. If the transformer core size is known due to space or cost considerations then the lowest frequency of f_{MAX} achievable with the selected transformer should be used.

2.3.2 Cable Compensation (GCAB)

The cable compensation is preset for each variant of C2183. For a chosen variant, the cable compensation is fixed. No external components are required to set the compensation.

To determine the compensation requirement, the following formula may be used.

$$G_{CAB} = \frac{(R_{CABLE} - R_{FD}) * I_{OUTCC}}{V_{OUTCV}} \quad R_{FD} = 0.1$$

R_{FD} is an error term caused by the temperature of the output diode changing in sympathy with the output current. Cable compensation depends on the type of cable, cable length and rated output. From the calculated cable compensation, choose an IC with the nearest cable compensation.

2.4 Front End Circuit Design

2.4.1 Input Resistor (Rin)

The input resistor, Rin limits the current during power-up and surge. The value of Rin is best found empirically to keep inrush current < 25 A (peak). Typical Rin selection is 10R. However, the value may need to increase for surge test consideration.

To improve efficiency, a lower resistor value or thermistor may be used instead, but surge protection should be considered.

2.4.2 Input Capacitors (Cin1 and Cin2)

The input capacitors aim to hold the rectified supply voltage above the minimum level that, below which, would cause the system to go into boundary mode (critical mode).

Where the converter is not required to provide hold-up time, the input capacitance can be calculated from the equation below or picked from Figure 6. This ensures a minimum input voltage ($V_{IN(MIN)}$) at full load (P_{INFL}) and low mains (V_{DCMIN}). The following equation may be used to calculate the minimum capacitance required:

$$Cin1 + Cin2 \geq \frac{P_{INFL}}{(1 - K_{CINTOL}).\pi.F_{IN(MIN)}.(2.V_{IN(MIN)}{}^2 - V_{DCMIN}{}^2)}.\arccos\left(\frac{-V_{DCMIN}}{\sqrt{2}.V_{IN(MIN)}}\right)$$

Where K_{CINTOL} is the estimated tolerance of the input capacitor; V_{DCMIN} is the minimum DC level (after the rectifier) required to ensure the power supply does not go into boundary mode; P_{INFL} is calculated from the maximum output power based on the expected transformer efficiency. These parameters are specified in section 2.2.

Based on the capacitance chosen, the minimum DC regulation level needs to be chosen to calculate the transformer turns ratio. When no hold-up time is required, this can be chosen to equal the calculated V_{DCMIN}.

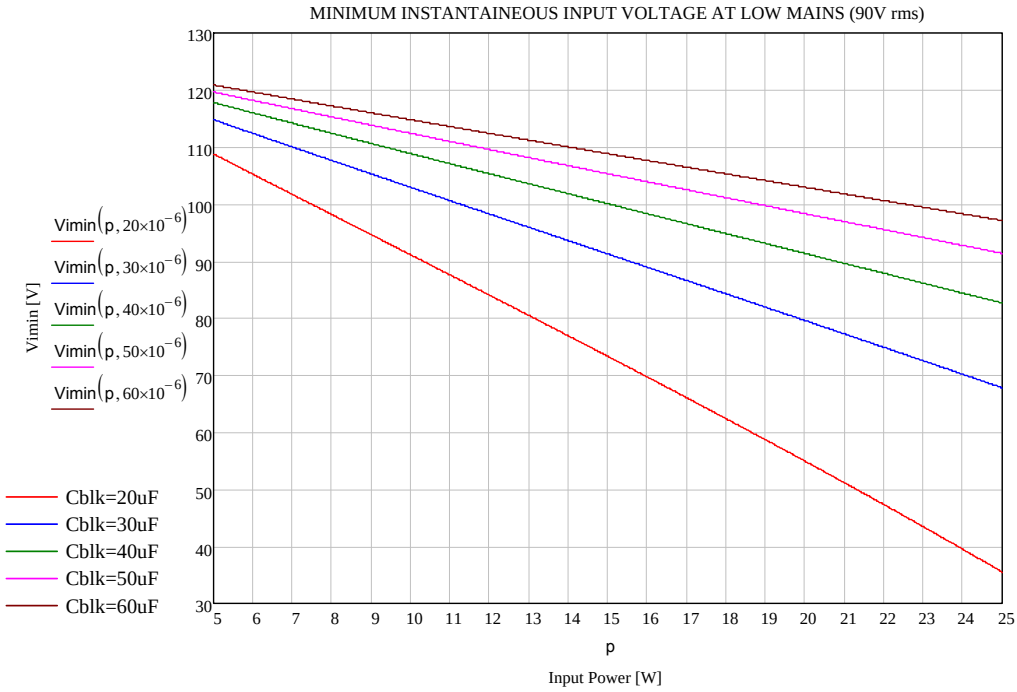

Figure 6: Input Capacitance Based on Input Power and Minimum Input Voltage

The capacitors require a minimum voltage rating of 400 V and at least Cin2 should be of low ESR type.

If the converter is required to provide hold-up time, the input capacitance must be significantly higher and/or the converter must switch at a much lower voltage. The graph in Figure 7 below could be used to choose the input filter capacitance so that T_{HOLD} = 10 ms is ensured at full-load and minimum mains. The hold-up time is checked using the following formula, where $V_{INREGMIN}$ is the minimum regulation voltage based on the total input capacitance, Cin, at full-load power. $V_{INREGMIN}$ must be less than V_{DCMIN} to ensure the hold-up time is met.

$$T_{HOLD} = \left(V_{DCMIN}{}^{2} - V_{INREGMIN}{}^{2}\right) \cdot \frac{Cin}{2 \cdot P_{INFL}}$$

The same graph could be used to determine the value of $V_{IN(MIN)}$, or if the capacitor size is too large or costly, could be used to find the necessary value of $V_{IN(MIN)}$.

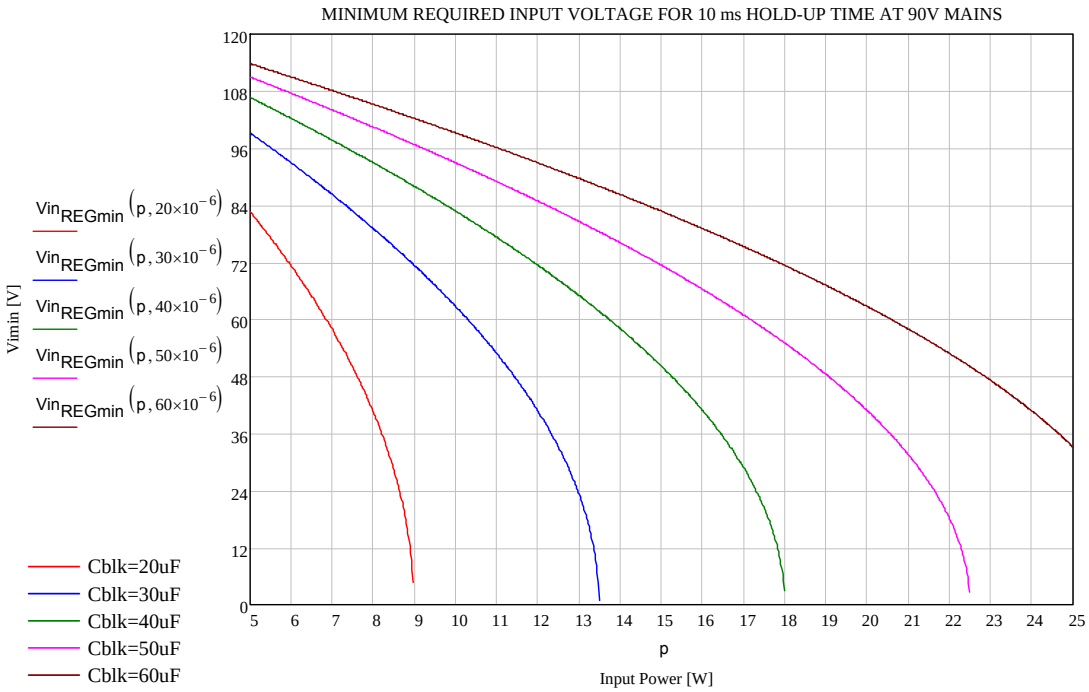

Figure 7: Input Capacitance Based on Input Power and Minimum Input Voltage for 10ms Hold-Up Time

The transformer design must always assume the lowest voltage on Cin for which full output power is required to meet hold up requirements, no matter what the hold-up input voltage requirement is.

2.4.3 Input Filter (Lfilt)

It is important to be aware of the current and temperature rating of the inductor used to improve differential mode noise, and ensure that the inductor does not saturate. Non-saturation of the inductor is particularly important if an LC filter is used (instead of a Pi filter), where high pulse current passes through the inductor at peak mains voltage. This high pulse current can cause the filter inductor to saturate if not adequately rated, and result in conducted EMC failures.

The resonant frequency of the inductor needs checked and, if necessary, a damping resistor (e.g. 10k) added in parallel with the inductor. For some cases, an additional Lfilt2 may be required to help with EMC, which needs to be found empirically.

2.4.4 Input Rectifier (Dbridge)

Implement the input line rectifier with four discrete diodes or an integrated bridge rectifier depending on the power requirement, cost and PCB area available for the application. A KBP206G bridge rectifier or four 1N4007 diodes are preferred but any other diodes are suitable with the following characteristics:

- Repetitive reverse maximum voltage rating, V_{RRM} > 600 V
- Average forward current rating, $I_{F(AV)}$ > = 1 A
- Surge forward current rating, $I_{F(SURGE)}$ > 25 A

2.5 Transformer Design

The transformer is a key component in the power supply design. The starting point for the transformer design is not always the same and is dependent on design constraints such as operating frequency or transformer size. The transformer interacts with nearly all other design considerations. It is therefore difficult to design the transformer in isolation. These interactions need constant consideration, and the transformer design needs iterated to accommodate an acceptable compromise throughout the design of the power supply.

2.5.1 Material Selection

The bobbin, core and wire to be used in the transformer affect the overall design so need to be well defined. They are often dependant on the power supply form factor so usually specified by the customer.

Select a transformer core and find the minimum cross sectional area of the core, Ae (other parameters, such as volume, may be needed if core loss is to be calculated).

2.5.2 Winding Topology

The preferred winding topology is shown below.

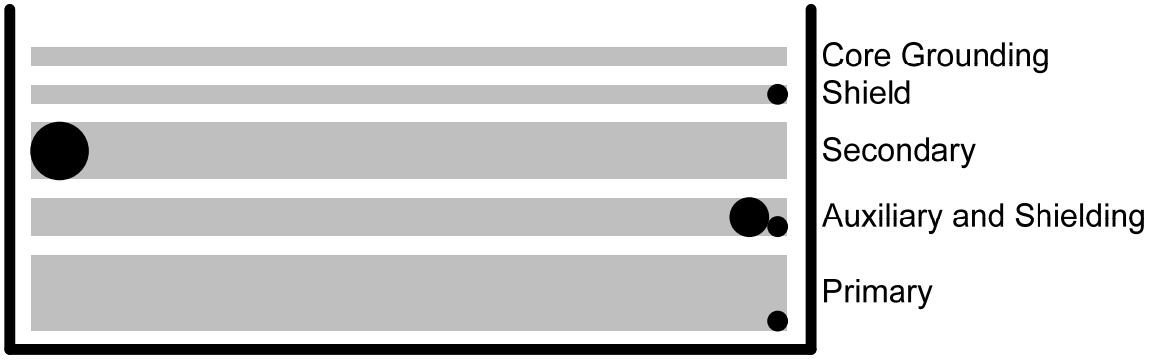

Figure 8: Winding Configuration

Placing a single strand wire AUX winding next to the primary winding as shown helps to reduce the leakage inductance between the primary and auxiliary. This helps to minimize the AUX voltage rise at full-load.

This winding arrangement also reduces the overall primary capacitance, which helps achieve higher efficiency.

A copper foil shield is used to isolate the primary and secondary windings and to help with EMC.

2.5.3 Transformer Turns Ratio (N)

Ideally, the converter operation should reach boundary mode at the minimum input voltage $V_{INREGMIN}$ while delivering full primary power, P_{PFL}. $V_{INREGMIN}$ is determined from the low mains allowed by the input capacitance (V_{DCMIN}), with some margin.

$$Nopt = \frac{I_{OUTCC} \cdot V_{SCV} \cdot V_{INREGMIN} \cdot V_{CSMAX} \cdot (1 - K_{CTRLTOL}) - 2 \cdot P_{PFL} \cdot V_{CSCC} \cdot V_{INREGMIN}}{2 \cdot P_{PFL} \cdot V_{SCV} \cdot V_{CSCC}}$$

P_{PFL} is the full-load power at the primary of the transformer; V_{SCV} is the voltage across the transformer secondary at full power and minimum output voltage, taking into account the voltage drop across Dout as calculated in section 2.2. V_{CSCC} and V_{CSMAX} are datasheet parameters. $K_{CTRLTOL}$ builds some design margin into the current regulation point to take into account tolerances of components and controller parameters.

The maximum transformer turns ratio is limited by the voltage rating of the primary switch Q1:

$$N\max = \frac{(1-\Delta V_{FET})\cdot V_{DSMAX} - V_{OVER} - \sqrt{2}\cdot V_{IN(MAX)}}{V_{SCV}}$$

V_{DSMAX} is the primary switch (FET) voltage rating; V_{OVER} is the switch voltage overshoot at turn off; $V_{MAINSHI}$ is the high mains RMS value; and ΔV_{FET} is the worst-case voltage margin dependent on the de-rating of the primary switch.

The lower of the two values (Nopt and Nmax) is chosen. If Nmax < Nopt then N = Nmax and the minimum input voltage at which the converter is still in regulation at full power is re-calculated. It is better to use Nopt where possible, but a higher rated MOSFET may be required.

$$V_{INREGMIN} = \frac{2\cdot N\cdot P_{PFL}\cdot V_{SCV}\cdot V_{CSCC}}{2\cdot P_{PFL}\cdot V_{CSCC} - I_{OUTCC}\cdot V_{SCV}\cdot V_{CSMAX}}$$

Note that if $V_{INREGMIN}$ is chosen to be greater than V_{DCMIN}, low mains ripple may be seen at full-load.

Current Sense Resistors (Rcs and Rcsesd)

Based on these calculations, the Rcs resistor can be calculated using the formula:

$$Rcs = \frac{N\cdot V_{CSCC}}{I_{OUTCC}}\cdot K_{CS}$$

Where N is the calculated turns ratio and K_{CS} is the current regulation accuracy factor. The CS input limit for CC operation, V_{CSCC} can be found in the datasheet. I_{OUTCC} is the constant current regulation point.

It may be necessary to use multiple resistors to get the required value. Alternatively, the number of primary turns can be adjusted to allow a standard resistor value to be used. Either way, the output current regulation point needs to be recalculated.

$$I_{OUTCC} = \frac{N\cdot V_{CSCC}}{Rcs}\cdot K_{CS}$$

For ESD protection, it may be necessary to add a 1k resistor adjacent to the CS pin as Rcsesd.

2.5.4 Transformer Peak Current and Inductance

Using the above values, the following parameters need to be checked. The primary peak current with the actual Rcs value needs to be calculated.

$$I_{PK} = \frac{V_{CSMAX}\cdot(1-K_{CTRLTOL})}{Rcs}$$

The primary inductance is calculated to provide full-load primary power, P_{PFL} at the maximum switching frequency, f_{MAX}.

$$L_P = \frac{2\cdot P_{PFL}}{I_{PK}^{\ 2}\cdot f_{MAX}}$$

In no-load operation, it is important that the minimum secondary conduction time, T_{SMIN} is longer than the feedback blanking time, T_{FBBL} of the controller as shown below. T_{FBBL} is given in datasheet.

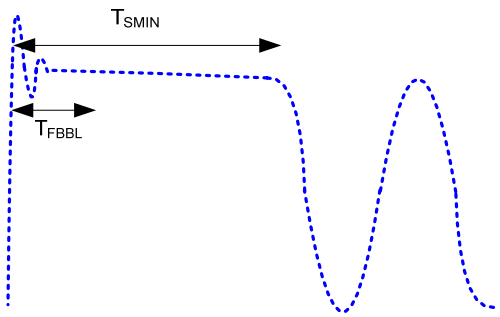

Figure 9: FB Blanking Time Waveform

This gives a requirement for the minimum primary inductance.

$$L_{PMIN} = \frac{N \cdot V_{SMAX} \cdot Rcs}{V_{CSMIN}} \cdot (T_{FBBL} - \frac{1}{4 \cdot f_{TX}})$$

f_{TX} is an estimate of the transformer resonant frequency given in section 2.2, and is a function of the transformer primary inductance, L_P, the power switch output capacitance, Coss, and the transformer equivalent parallel capacitance reflected to the primary, Ctx. For a good transformer design, Ctx is ideally an order of magnitude smaller than Coss. For example, using a Z-winding in the primary would reduce the transformer capacitance.

$$f_{TX} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_P \cdot (Coss + Ctx)}}$$

If $L_P < L_{PMIN}$ by a small margin, increasing Rcs a small amount would reduce the peak current, I_{PK} and allow an increase in L_P required for full power. Note however that this will result in higher $V_{INREGMIN}$, in a reduced hold-up time and the transformer turns ratio, N would need recalculated to ensure I_{OUTCC} does not move.

If a different value of L_P is chosen from that calculated, then this will affect the actual $K_{CTRLTOL}$ value used, resulting in a different margin allowance. This needs to be recalculated to check the current margin is sufficient.

2.5.5 Transformer Primary and Secondary Turns

The number of primary and secondary turns then need to be calculated based on the transformer material to be used. A starting point for the number of primary turns is calculated from the primary inductance so that at the primary peak current, the core flux density does not exceed the full-load requirement as a rule of thumb.

$$N_P = \frac{L_P \cdot I_{PK}}{B_{FL} \cdot Ae\min}$$

Aemin is the minimum transformer core cross-sectional area. The number of primary turns, N_P is increased to reduce the steady state peak flux density, B to ensure that the core does not saturate during normal operation.

$$B = \frac{L_P \cdot I_{PK}}{N_P \cdot Ae\min}$$

The number of secondary turns is then calculated to provide the required transformer turns ratio N. Ideally the number of secondary turns would fit into one layer on the bobbin.

$$N_S = \frac{N_P}{N}$$

The actual turns ratio must be re-calculated after N_P and N_S are rounded up to the next integer number.

Using these values, the following parameters need to be recalculated and checked:

- Rcs, L_P, actual V_{CSMAX} used by controller: $V_{CSMAXACT} = \frac{2 \cdot P_{PFL} \cdot V_{CSCC} \cdot N \cdot Rcs}{L_P \cdot f_{MAX} \cdot I_{OUTCC}}$
- I_{OUTCC}, $V_{INREGMIN}$ and I_{PK}
- $B_{MAX} = \frac{L_P \cdot V_{CSMAX}}{N_P \cdot Ae \min \cdot Rcs}$ during transient and start-up to check core does not saturate
- $T_{SMIN} > T_{FBBL}$ where $T_{SMIN} = \frac{1}{N} \cdot \frac{V_{INREGMIN}}{(V_{OUTCV} + V_{Dout})} \left(\frac{V_{CSMIN} \cdot I_{OUTCC} \cdot L_P}{N \cdot V_{INREGMIN} \cdot V_{CSCC}} + t_{CSOFF} \right)$

Based on the calculated results above and the known transformer material, the core gap is calculated.

2.5.6 Basic Tolerance Analysis

Many components within the circuit vary depending on manufacture, voltage and temperature. To consider all these would take a worst-case scenario that is unlikely to occur often, i.e. the sum of the worst tolerance of all components. However, it is important to consider some tolerance to ensure that the circuit will deliver the minimum required power.

A simple check is to take the expected tolerance of the primary inductance, $K_{LPTOL,}$ which is usually one of the worst spreads, and switching frequency tolerance, K_{FTOL}, and check the worst-case can deliver the required power.

Primary power available including L_P and f_{MAX} tolerances:

$$P_{PFL} = \frac{1}{2} \cdot (1 - K_{LPTOL}) \cdot (1 - K_{FTOL}) \cdot L_P \cdot f_{MAX} \cdot \left(\frac{V_{CSMAX}}{Rcs} \right)^2$$

Secondary power: $P_{SFL} = P_{PFL} \cdot \eta_{TX}$

Achievable output current: $I_{OUTCC}(\min) = \frac{P_{SFL}}{(V_{OUTCV} \cdot K_{GCAB} + V_{Dout})}$

2.5.7 Auxiliary Turns (N_A)

It is important to check that V_{AUX} does not go too high in no-load. If it goes too high, the no-load power and low load efficiency are affected. To determine the minimum number of auxiliary turns required, the voltage on the transformer, V_A needs calculated. NB it may be necessary to add an extra resistor in the AUX path as shown below and described in section 2.7. The resistor is to help prevent any issues due to ESD.

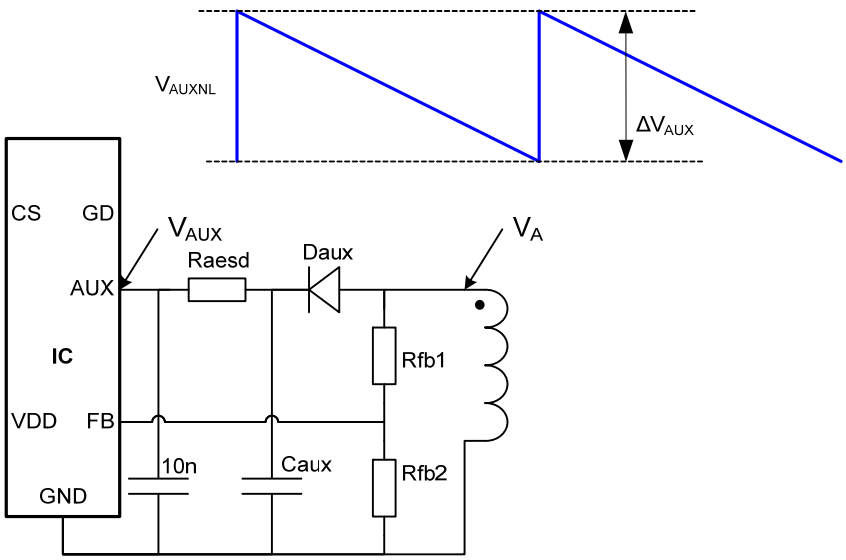

Figure 10: Auxiliary Circuit with Extra Components

The voltage drop across the diode and resistor is $V_{RaesdDaux}$. The minimum IC AUX pin voltage, V_{AUXLOW}, and the AUX pin voltage peak-to-peak amplitude (ΔV_{AUXPFM}) are from the datasheet. The maximum voltage seen during no-load by the transformer is $V_{ANL} = V_{AUXLOW} + \Delta V_{AUXPFM} + V_{RaesdDaux}$. So the minimum number of AUX turns is calculated.

$$N_{AMIN} = \frac{V_{ANL}}{V_{OUTCV} + V_{Dout}} \cdot N_S$$

Based on these calculations, N_A can be chosen. Once the number of auxiliary turns is chosen, the AUX voltage should be recalculated to confirm that the voltage drop, ΔV_{AUX} is still appropriate.

When the primary switch turns on, sufficient current is drawn to cause V_{AUX} to dip. A 10 nF capacitor added to the controller AUX pin prevents this. If the AUX pin reaches $V_{AUXSLEEP}$, the controller enters into a new cycle.

2.5.8 Feedback Winding

Typically, there are no constraints to the number of turns of the sense winding, N_F. Often for simplicity, the AUX winding could be used as the feedback winding.

2.5.9 Primary and Secondary RMS Currents

The maximum continuous RMS current through the primary and secondary winding can be calculated using the average value of the input voltage at minimum mains and full power $V_{INAVMIN}$.

$$I_{PRMSMAX} = I_{PK}^{3/2} \cdot \sqrt{\frac{f_{MAX} \cdot L_P}{3 \cdot V_{INAVMIN}}} \qquad I_{SRMSMAX} = I_{PK}^{3/2} \cdot \sqrt{\frac{N \cdot f_{MAX} \cdot L_P}{3 \cdot V_{SCV}}}$$

Alternatively, the maximum primary RMS current for 90V mains could be obtained from the graph below for known values of the input bulk capacitance and input power.

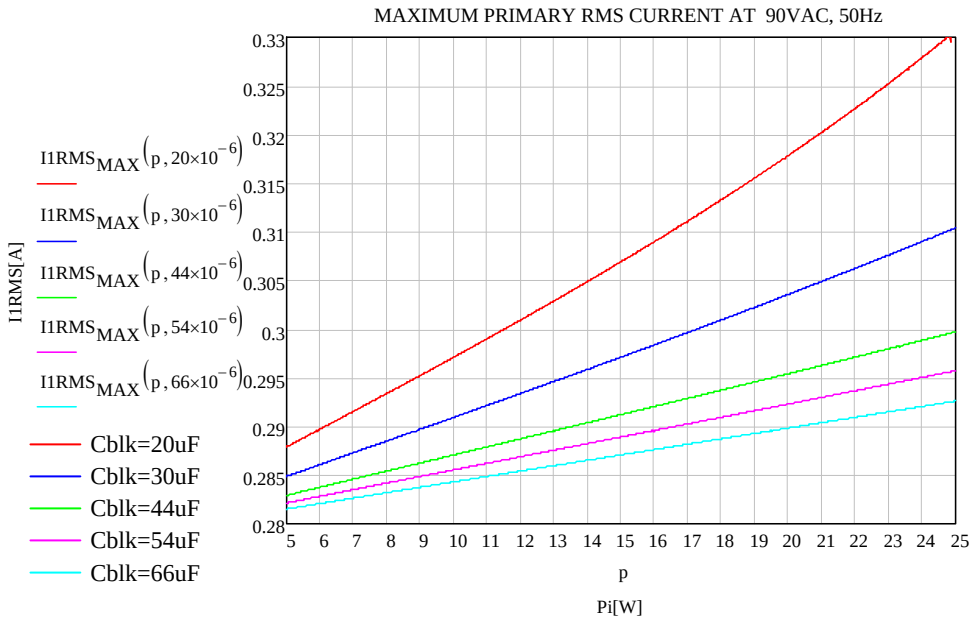

Figure 11: Maximum Primary RMS Current at 90 V 50 Hz

The values of $I_{PRMSMAX}$ and $I_{SRMSMAX}$ could be used to calculate the diameter of a single strand copper wire for the primary and the secondary winding based on the current density. If the calculated wire diameter is greater than three times the copper skin depth at f_{MAX}, then a larger diameter wire or multi-filar winding should be considered. The copper skin depth for a frequency f at 100ºC in mm is:

$$\delta = \frac{0.071}{\sqrt{f}}$$

In a comprehensive design, the skin effect and the proximity effect of all spectral components of the primary and secondary current should be considered when appointing the transformer windings.

In a typical case, the secondary will be a single layer winding made out of triple insulated wire and the proximity effect could be ignored when calculating the equivalent wire diameter. Often the size of transformer core (bobbin) is determined out of cost considerations. More over the required wire insulation often takes a significant part of the window allocated to the secondary winding. Consequently, the number of secondary turns calculated do not fit in a single layer. In such a case, if a larger core is not an option, then the above calculations must be redone using the number of secondary turns that can fit in a single layer.

2.6 Output Circuit

2.6.1 Output Diode (Dout)

The output diode must withstand continuous operation under overload conditions and reverse voltage at peak input voltage. For efficiency reasons, Schottky diodes are better for output voltages (V_{OUTCV}) up to 12 V. Above this, fast epitaxial diodes are more suitable.

To calculate the minimum recommended reverse voltage, V_{RRM} rating required for the diode, use the following formula. This includes a ΔV_{Dout} de-rating factor.

$$V_{RRM} = [V_{OUTCV} * (1 + G_{CAB}) + \left(\sqrt{2} * V_{IN(MAX)} * \frac{N_S}{N_P} \right)] / (1 - \Delta V_{Dout})$$

A diode with a larger maximum current is better for thermals and efficiency because it generally has a lower voltage drop. A rule of thumb is to use a current rating 2-5 times larger than the output current. Some diode

datasheets provide power loss information; otherwise, empirically the diode needs to be checked for power loss to ensure all performance requirements are met.

2.6.2 Output Resistor (Rout)

The dummy resistor value is calculated to ensure that the power transferred to the output each switching cycle is dissipated within that cycle, so that the output voltage does not lift. To ensure good regulation, sufficient power must be available to be sensed at the output, i.e. secondary current should conduct longer than the auxiliary current to ensure correct measurement. To ensure this, it is recommended that P_{DUMMY} = P_{ANL} + P_{MARGIN}, where P_{MARGIN} is approximately 1 - 3 mW.

$$Rout = \frac{V_{OUT}{}^2}{P_{DUMMY}}$$

P_{ANL} uses the average voltage on the AUX calculated when selecting the number of AUX turns (2.5.7), and the assumptions about margin stated in the section describing the AUX capacitor selection (2.7.2) along with various datasheet parameters.

$$P_{ANL} = \frac{(2 \cdot V_{ANL} - \Delta V_{AUXPFM} + 0.6)}{2} \cdot I_{AUXNL}$$

A larger value resistance can be used to reduce the no-load power, but will allow output voltage lift at no-load.

2.6.3 Output Capacitor (Cout)

Output capacitors are usually constrained by the following:

- Ensuring the capacitor value is big enough to limit the initial drop in output voltage before the controller circuit responds to meet the load step undershoot requirements.
- Ensuring that the ESR of the capacitor is suitable for ripple requirements.
- Ensuring that losses in the ESR of the output capacitor are low for better efficiency.

2.6.4 Output Snubber

A secondary snubber is recommended for applications ≥ 3 W, to achieve EMC compliance as shown in Figure 12 but will affect efficiency. The optimum values for Rssnub and Cssnub are found by experimentation. Increase the value of Cssnub to improve EMC margin. Decrease Cssnub to improve margin on no-load power and efficiency.

Starting point values for Rssnub and Cssnub are given by the equations:

$$Rssnub = \frac{V_{OUTCV}{}^2}{5} \qquad Cssnub = \frac{125}{V_{OUTCV}{}^2}\ \text{nF}$$

2.6.5 Primary Clamp

To reduce the peak drain voltage further, a primary snubber may be added as shown below. Rpsnub1, Dpsnub, Rpsunb2, and Cpsnub form a simple diode clamping snubber.

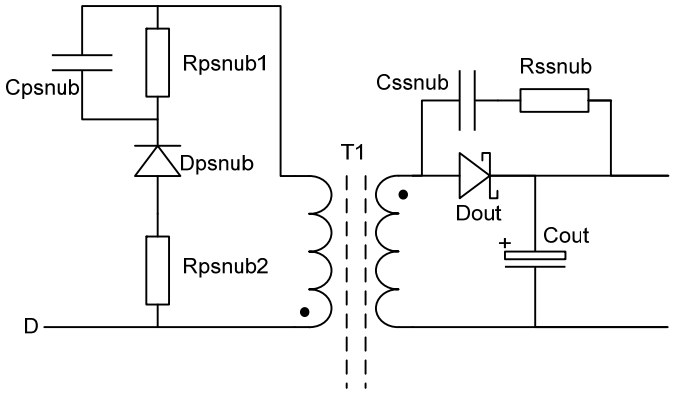

Figure 12: Primary Clamp and Secondary Snubber Components

Cpsnub can be in the range of 220 pF to 1000 pF with a 500 V rating.

A GF1M diode is recommended for Dpsnub; alternatively, faster diodes such as HER107, FR107, or S1ML may be used. Using a slower diode is good for radiated emissions, but can corrupt voltage regulation.

Rpsnub1 can be chosen in the range of 100 kΩ to 1 MΩ. The exact value chosen is a trade-off between efficiency and peak drain voltage.

Rpsnub2 can be chosen in the range of 22 Ω to 1 kΩ. The exact value chosen is a trade-off between peak collector voltage and RF emissions compliance.

No-load performance needs to be checked as these components affect performance.

2.7 VDD and Auxiliary Circuit Design

The C2183 is implemented in a technology that allows input voltages up to $V_{AUX(max)}$. The controller allows the AUX capacitor to be charged to V_{AUXRUN} before attempting to start, resulting in more energy being available to power the controller when starting up with a capacitive load.

2.7.1 VDD Capacitor (Cdd)

The C2183 uses a series regulator in order to provide the low voltage V_{DD} supply needed to power the low voltage section of the controller. This reduces power dissipated in the controller when it is operating at full power. The Cdd capacitor is present only to de-couple the V_{DD} supply and ensure a clean supply for the low voltage section of the chip as shown in Figure 13.

The minimum recommended value for Cdd is 0.47uF, type X7R and rated for 25V operation. This needs to be checked once Caux has been finalised. In addition, a 10nF capacitor in parallel with the Cdd may be required for minimizing noise generated by the on-chip clock and meeting radiated EMC.

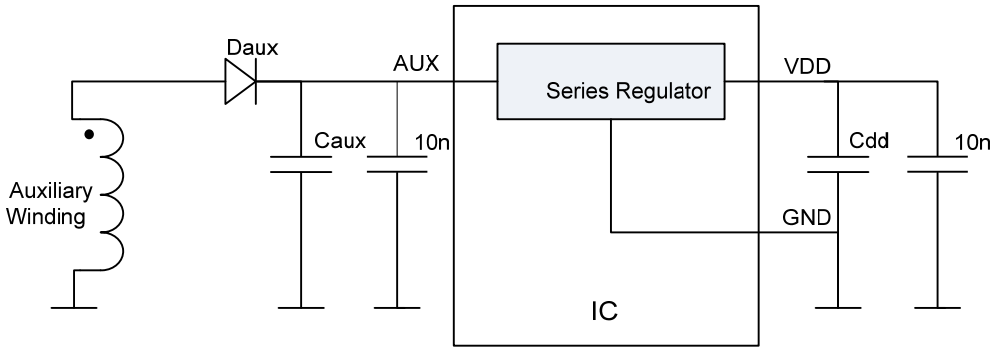

Figure 13: Series Regulator Arrangement

2.7.2 Auxiliary Capacitor (Caux)

The C2183 includes a pulse frequency modulator (PFM) stage that, in conjunction with the Caux, determines the switching frequency at no-load.

During no-load operation, the peak-to-peak voltage amplitude on the AUX pin must be less than ΔV_{AUXPFM}. So to make sure that under all conditions and due to all component tolerances, the datasheet limit is not exceeded Caux is calculated using $\Delta V_{AUXPFM} - 0.6 = 1$ V to allow margin. Based on the calculated Caux, round up to the nearest standard value.

$$Caux = \frac{I_{AUXNL}}{(\Delta V_{AUXPFM} - 0.6) \cdot f_{MIN}}$$

The energy per cycle needs to be calculated to determine the minimum frequency that will be seen at no-load operation. The peak primary current is known from the current sense resistor value so the energy per cycle delivered can be calculated. The energy used in the primary clamp can be approximated. So the energy delivered to the secondary side ($E_S + E_A$) is the difference between these.

$$I_{PK} = \frac{V_{CSMIN}}{Rcs} \qquad E_{CYCLE} = \frac{1}{2} \cdot L_P \cdot I_{PK}2 \qquad E_{CLAMP} = \frac{1}{2} \cdot Cpsnub \cdot \left[N \cdot (V_{OUTCV} + V_{Dout})\right]^2$$

$$E_S + E_A = E_{CYCLE} - E_{CLAMP}$$

The auxiliary and secondary power during no-load can be calculated to determine the total power during no-load. No-load efficiency is assumed in section 2.2.

$$P_{ANL} = \frac{(2 \cdot V_{AUXNL} - \Delta V_{AUXPFM} + 0.6)}{2} \cdot I_{AUXNL} \quad P_{SNL} = \frac{V_{OUTCV}{}^2}{Rout} \quad P_{SANL} = \frac{P_{SNL} + P_{ANL}}{\eta_{NL}}$$

From this, the minimum frequency can be calculated. With the required no-load frequency, f_{MIN}, the value of the capacitor is determined.

$$f_{MIN} = \frac{P_{SANL}}{E_S + E_A}$$

In the controller, the low voltage and high voltage parts have different start-up levels. V_{DD} tracks V_{AUX} as shown in the diagram below. The ramp rate of each voltage is dependent on the appropriate capacitor. So by changing the capacitance, the start-up points for AUX and VDD vary. Ideally, the relationship between Cdd and Caux values can be described by $0.5 < Cdd / Caux < 2$. If the ratio is too low, there could be start-up issues. If the ratio is too high, V_{AUX} could go above the specified maximum limit.

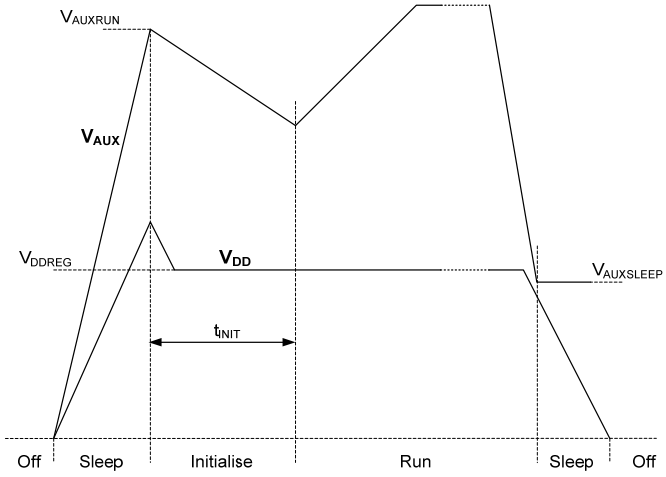

Figure 14: AUX and VDD Waveforms

A 25 V capacitor should be used to allow the AUX voltage its full range. X5R or X7R capacitors are good because the capacitance value is less variable over voltage.

Once Caux is chosen, the AUX voltage ramp needs to be checked to ensure it is within range over temperature and process tolerance as specified by ΔV_{AUXPFM}.

$$\Delta V_{AUX} = \frac{I_{AUXNL}}{Caux \cdot f_{MIN}}$$

2.7.3 Start-up Resistor (Rht)

The controller remains asleep until Caux is charged to V_{AUXRUN}. The start-up time for the circuit depends on the Rht current available to charge Caux and power the IC via the AUX pin. The IC current required is given by $I_{AUXSLEEP}$ in the datasheet. An approximation of the required circuit current can be given as below. In reality, I_{Rht} reduces with time because the voltage across the resistor decreases as V_{AUX} rises. Therefore, the capacitor charging current also reduces with time. So the answer is slightly higher than reality.

$$I_{Rht} = \frac{Caux \cdot V_{AUXRUN}}{T_{STARTUP}} + I_{AUXSLEEP}$$

The longest start-up time will be at minimum input mains, $V_{IN(MIN)}$. This allows an approxmate value for Rht to be calculated.

$$Rht = \frac{V_{IN(MIN)}}{I_{Rht}}$$

Once a standard resistor value is chosen, the actual IC start-up time can be recalculated. Note that this does not include the time taken for the output to reach its target level, which is only milliseconds, where the start-up time is usually in the order of seconds.

There is a trade-off between start-up time and no-load power, dependent on the Rht value; increase the resistor value to lower no-load power but increase start-up time. Enough current must be available for both the IC to power up and Caux to charge.

The voltage rating of the resistor(s) must be able to withstand the maximum input voltage. To reduce the BOM count, it is possible to use one resistor with a higher voltage rating.

2.7.4 No-load Power and Undershoot Considerations

The minimum frequency is critical to the no-load power and undershoot requirements so it is important to check that the AUX capacitor value chosen still allows these requirements to be met.

There is a compromise between switching losses and visibility of output voltage. To keep no-load power low, the no-load switching frequency should be kept low. For undershoot considerations, the switching frequency under no-load or light loads should be high so that when a load transient from no-load occurs, the controller will respond quickly. Worst case the controller will wait a whole switching cycle; the slower the frequency, the longer the switching cycle, the longer the response, the more the output voltage will drop as shown below.

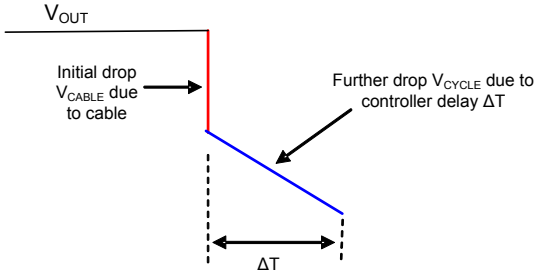

Figure 15: Voltage Drop During Load Step From No-load

The initial drop in the voltage due to the cable is calculated from $V_{CABLE} = R_{CABLE} \cdot I_{LOADSTEP}$ where $I_{LOADSTEP}$ is the load step requirement and R_{CABLE} is the cable resistance. This is then used to work out the voltage margin available when considering the allowed undershoot voltage V_{USHOOT}. To allow for component variations a tolerance of V_{TOL} is included. A reasonable value for V_{TOL} would be 0.2 V.

$$V_{MARGIN} = V_{OUTCV} - V_{CABLE} - V_{USHOOT} - V_{TOL}$$

The minimum frequency allowable to meet the undershoot requirement, $f_{MINUSHOOT}$ is then calculated. This should be less than the minimum frequency, f_{MIN} calculated above to ensure the voltage stays above V_{USHOOT}.

$$f_{MINUSHOOT} = \frac{I_{LOADSTEP}}{V_{MARGIN} \cdot Cout}$$

The total no-load power is calculated as follows, including a margin, $P_{NLMARGIN}$ to account for tolerances.

$$P_{NL} = P_{SNL} + P_{ANL} + P_{CLAMP} + P_{SWNL} + P_{NLMARGIN} + P_{NLHT}$$

The switching no-load power, P_{SWNL} is calculated from the estimated capacitances of the transformer, Ctx and primary switch, Coss as previously discussed in section 2.5.4.

$$P_{SWNL} = 1/2 \cdot (Coss + Ctx) \cdot (\sqrt{2}V_{MAINSHI})^2 \cdot f_{MIN}$$

The start-up resistor power loss, P_{NLHT}, is also calculated at high mains, $V_{MAINSHI}$, as this will be worst case.

$$P_{NLHT} = \frac{(\sqrt{2}V_{MAINSHI})^2}{Rht}$$

The above calculations assume the output capacitor has very low ESR (e.g. 20mΩ or so), therefore the voltage drop due to the ESR is negligible.

The delay in response by the controller could be longer than the switching period of no-load frequency because, typically, the controller needs to see a minimum of 0.4 V output voltage error before starting to correct. So if the initial voltage change is less than 0.4V, the controller may not notice until there is further voltage drop. Therefore it is possible, at the worst case, the overall undershoot is larger than that calculated above, hence it is important to allow extra margin.

2.7.5 Auxiliary Supply Diode (Daux)

The following table lists some recommended AUX diodes.

Type	T_{RR} (ns)	V_{RRM} (V)	V_{FD} (V) @	I_F (A)
1N4148	4	75	1.0	0.15
1N4933	50	50	1.0	1.0
SF11G	35	50	1.0	2.0
UF4001	50	50	1.0	2.0
BYV27-50	25	50	1.0	2.0
UG1A	25	50	1.0	3.0
ES1A	35	50	1.0	3.0
STTH1R02	15	200	1.0	3.0

Table 3: Recommended AUX Diodes

The voltage rating of the diode needs to be checked against the maximum auxiliary voltage based on the number of chosen auxiliary turns and the capability of the IC, so that $V_{RRM} > V_{Daux(MAX)}$.

$$V_{Daux(MAX)} = \sqrt{2} \cdot V_{IN(MAX)} \frac{N_A}{N_P} + V_{AUX(MAX)}$$

If considering a Schottky diode, some have large leakage at high temperature, so start-up across temperature should be checked if a Schottky diode is used. Remember that the voltage across the auxiliary diode will affect the calculation of the AUX capacitor.

2.7.6 Auxiliary ESD Resistor (Raesd)

To ensure that ESD events do not affect the controller circuit, it is recommended that a resistor be placed in the AUX pin path. This should not exceed 47R.

2.7.7 Auxiliary Snubber (Rasnub and Casnub)

The auxiliary snubber helps the circuit meet EMC requirements. The recommended range for Casnub is between 47 pF and 2.2 nF. The recommended starting value for Rasnub is 47R. The no-load performance should be checked once the values have been found empirically to meet EMC.

2.7.8 Capacitive Load Pull-Up Considerations

There is a trade-off between the capacitive load pull-up capability, start-up time, no-load power and the application circuit functioning correctly. This section considers the implications on the circuit required to accommodate these performance factors.

To ensure that the circuit can pull-up the capacitive load (Cload) at start-up we need to consider the capability of the application based on the Caux value. Caux controls the time allowed for Cload to be pulled up, based on the voltage drop allowable before the IC goes to sleep ($V_{AUXRUN} – V_{AUXSLEEP}$), see Figure 14, and the current drawn by the IC (I_{AUXRUN}).

$$t_{AUX} = \frac{Caux \cdot (V_{AUXRUN} - V_{AUXSLEEP})}{I_{AUXRUN}}$$

In this time, the output voltage should be pulled above V_{SHUTDN}, the hiccup point as shown in Figure 3 to ensure normal run operation is achieved.

$$t_{PULLUP} = \frac{Cload \cdot V_{SHUTDN}}{(I_{OUTCC} - I_{OUTCP})}$$

This gives a ratio of Cload to Caux for the known application and datasheet parameters as below, which gives the load capacitance pull-up possible based on the chosen Caux.

$$\text{Load pull-up: } \frac{Cload}{Caux} = \frac{(V_{AUXRUN} - V_{AUXSLEEP})}{I_{AUXRUN}} \cdot \frac{(I_{OUTCC} - I_{OUTCP})}{V_{SHUTDN}}$$

To accommodate the largest pull-up load, Caux can be increased, but other application parameters need to be accounted for. For example, Caux controls the minimum frequency, which is required to be low to ensure no-load power performance. This gives a maximum value for Caux, based on the current drawn by the IC during no-load (I_{AUXNL}) and the minimum AUX voltage drop achievable with some margin (ΔV_{AUXPFM}*2).

$$\text{No-load: } Caux(\max) = \frac{I_{AUXNL}}{f_{MIN} \cdot \Delta V_{AUX}} = \frac{I_{AUXNL}}{f_{MIN} \cdot (\Delta V_{AUXPFM(MIN)} \cdot 2)}$$

Caux also influences the start-up time of the application. The minimum current flowing through Rht will be at low input mains for the given Rht value.

$$I_{Rht(MIN)} = \frac{V_{IN(MIN)}}{Rht}$$

The charging current through the start-up resistor(s) will vary during start-up (as the capacitor charges) so to find the maximum capacitor which allows the start-up time ($T_{STARTUP}$) to be achieved, the minimum start-up current ($I_{Rht(MIN)} - I_{AUXSLEEP}$) is considered to charge the capacitor to the voltage required to enter normal operation (V_{AUXRUN}). This takes into account the current required by the IC. Note that there will be variations due to process, temperature and voltage on these parameters, so it is advisable to allow some margin on the start-up time to ensure it is achieved across production.

$$\text{Start-Up: } Caux(\max) = \frac{\left(I_{Rht(MIN)} - I_{AUXSLEEP}\right) \cdot T_{STARTUP}}{V_{AUXRUN}}$$

It can be seen that the value of Caux needs to be a trade-off to achieve load pull-up, no-load power and start-up while ensuring the application circuit conforms to the IC datasheet. If sufficient no-load power margin is available, it may be possible to adjust Rht to give more start-up headroom. Any changes made to Rht or Caux need to be checked with previous calculations made.

To help pull-up a larger load, it is possible to move the hiccup point (V_{SHUTDN}) further down the CC chimney. This would allow a larger capacitive load to be pulled up for a given Caux. This may be achievable by one of the following, although these have side effects that need to be monitored.

- Ensuring good coupling between the primary and auxiliary windings in the transformer
- Or increasing the auxiliary snubber

Increasing the AUX snubber will affect the no-load and light load efficiency.

Improving the primary-auxiliary coupling will result in V_{AUX} going higher at full-load and transients. To ensure correct operation of the IC, this must be kept below $V_{AUXRUN(MAX)}$. This could be achieved by making the primary clamp circuit weaker (e.g. Cpsnub = 220 pF and Rpsnub1 = 470 kΩ) and placing a Zener diode in the auxiliary circuit as shown below. The extra diode (or diode and capacitor) are required to ensure that a leakage path is not created by the Zener, which could prevent the circuit from starting up.

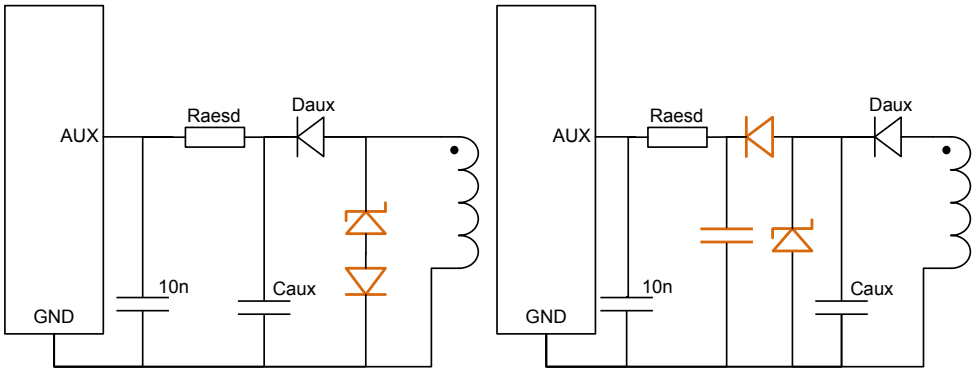

Figure 16: Zener Diode in Auxiliary Clamp Circuit

The chosen Zener must have the correct voltage and power rating for the circuit. The energy generated by the Zener should be checked, particularly over temperature. The effect of these changes needs to be checked across other performance factors, particularly radiated and conducted emissions.

2.8 Voltage Sense Circuits

2.8.1 Voltage Feedback

The C2183 has the voltage feedback signal (scaled via resistors divider) fed to the FB pin directly. When the sense winding voltage is negative, the controller drives sufficient current out of the FB pin to keep the pin voltage at ground (GND) potential. The current will depend on the value of Rfb1 and the amplitude of the negative voltage on the sense winding. The resulting FB pin voltage and current waveforms are shown in blue and green respectively below.

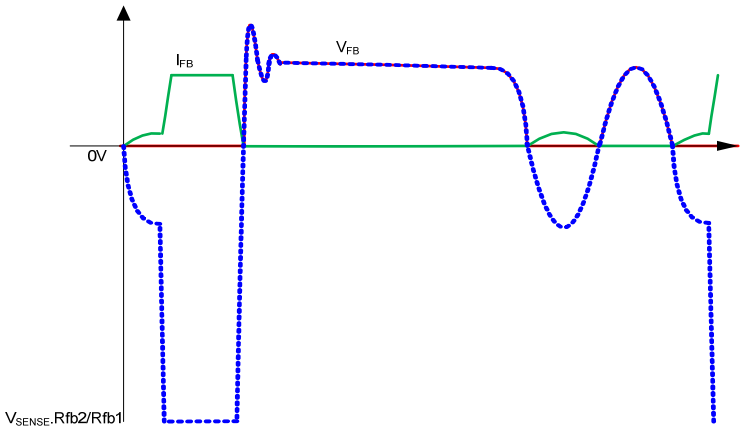

Figure 17: FB Pin Waveforms

The controller determines the sense voltage level by measuring the FB pin current sourced during the primary switch on-time. The relationship between the current and the input capacitor voltage depends on the primary to sense turns ratio and the value of Rfb1. The controller applies three different thresholds to the FB pin source current during CHARGE. These thresholds are defined in the datasheet.

The highest level, I_{FBHTHI}, alerts the controller to excessive bulk capacitor voltage, for example during a surge event. The controller responds by reducing the power delivered to the output in an attempt to limit the peak voltage across the primary switch.

The lowest level, I_{FBHTLO}, alerts the controller to the bulk capacitor voltage being too low to sustain normal operation. (Or it may indicate that the FB pin is not connected to the sense winding due to a fault.) When the threshold is triggered, drive to the primary switch is disabled so V_{AUX} decreases. When it falls to V_{AUXLOW}, the controller requests a new switching cycle but this is negated by the low mains condition. Therefore, the voltage continues to fall to $V_{AUXSLEEP}$, the controller goes to sleep and the start-up switch is turned on to initiate a restart cycle.

If the input bulk capacitors are sufficiently charged, the AUX voltage rises. If the AUX voltage rises to V_{AUXRUN}, the controller wakes up, turns the start-up switch off and issues one probe pulse to measure the bulk capacitor voltage and determine if it is high enough to start. If it is above the minimum start-up mains voltage ($I_{FB} > I_{FBHTSTART}$), then the controller restarts. If the bulk capacitor voltage is below the minimum voltage, the drive to the primary switch is disabled and the process repeats.

2.8.2 Feedback Resistor 1 (Rfb1) – Input Over Voltage Protection

In most charger applications, the maximum bulk capacitor voltage will provide the most important limitation. Therefore, the value of Rfb1 (top resistor) should be calculated to ensure that the controller operates in over voltage protection (OVP) mode when the bulk capacitor voltage exceeds $V_{BULKMAX}$. Mains input OVP is triggered if the current sourced from the FB pin, during the on-time exceeds I_{FBHTHI}.

$$Rfb1 = \left(\frac{V_{BULKMAX}}{I_{FBHTHI}} \cdot \frac{N_F}{Np} \right)$$

Where N_P is the number of primary turns and N_F is sense winding turns. For most universal mains charger applications, $V_{BULKMAX} = \sqrt{2}.V_{IN(MAX)}$ + 15% margin (50V), around 425 V.

The tolerances of Rfb1 and Rfb2 affect output voltage regulation and mains estimation so should typically be chosen to be 1% or better.

2.8.3 Input Voltage Start Threshold (Brown-in)

Once Rfb1 is decided, the input voltage start threshold can be calculated.

In Initialise mode, the controller issues a single low energy switching cycle in order to measure the applied mains voltage level. If the level detected by this low energy probe cycle, is below $V_{MAINSSTART}$ then the IC will not start. It will pause, while V_{AUX} discharges below $V_{AUXSLEEP}$, then it will begin a new power-up cycle and repeat the process. Once the mains voltage exceeds $V_{MAINSSTART}$, the converter will power-up normally. $V_{MAINSSTART}$ can be determined from the Rfb1 resistor value using:

$$V_{MAINSSTART} = \frac{-1}{\sqrt{2}} \cdot I_{FBHTSTART} \cdot Rfb1 \cdot \frac{N_P}{N_F}$$

2.8.4 Input Under-Voltage Protection ((Brown-out)

From Rfb1 value, the input under voltage protection threshold can be calculated. In Run mode, if the input rectified DC voltage reduces to V_{DCBRN}, the control circuitry will stop driving the primary switch, V_{AUX} will reduce to $V_{AUXSLEEP}$ and the IC will enter sleep mode.

$$V_{DCBRN} = I_{FBHTLO} \cdot Rfb1 \cdot \frac{N_P}{N_F}$$

2.8.5 Feedback Resistor 2 (Rfb2) - To Set Output Voltage

With the value of Rfb1 selected, the value of Rfb2 (bottom resistor) can be selected to set the output voltage as below:

$$Rfb2 = \frac{Rfb1 \cdot V_{FBREG}}{V_{OUTCV} \cdot \frac{N_F}{N_S} - V_{FBREG}}$$

Where N_S is the secondary winding turns, N_F is sense winding turns (auxiliary winding turns if it is combined). The FB regulation level V_{FBREG} can be found in the datasheet.

2.9 Switch Selection

The chosen primary switch (MOSFET) must have a gate threshold of less than 4 V and be rated as follows:

Voltage Rating: $V_{DS(MAX)} \geq N \cdot V_{SCV} + \sqrt{2} \cdot V_{IN(MAX)} + V_{OVER}$

Current Rating: $I_D \geq I_{PK}$

The gate capacitance needs to be low enough to ensure the switch turns on properly. In the order of < 1 nF.

The power switch output capacitance, Coss, needs to be considered as discussed in the calculation of L_P (2.5.4). The higher the Coss, the more impact it will have on low load efficiency, so should be minimised if possible.

2.10 PCB Layout

Good layout practice helps with:

- Achieving low EMI
- Thermal optimization
- Design for manufacture

Some simple, good practices and guidelines for routing are:

- Make track widths appropriate for current to be carried
- Space tracks according to voltage difference between them
- Keep tracks as short as possible.
- Prioritize critical paths: highest first (high current, high frequency, high voltage)
- Keep thin tracks away from board edge
- Route tracks to centre of a connecting pad

2.10.1 Functional Considerations

Current loops (signal paths and ground returns) that carry fast edges are a potential source of radiated EMI. The faster and larger the current fluctuations, the higher the radiated EMI power will be. Also the larger the area enclosed by the loop, the higher the level of EMI. The latter is where good PCB design can help, and poor design can cause a real problem. The key is to keep current loops small and run out/return tracks close together. Doing so keeps the loop area and radiated emissions down.

The following are the critical current loops in a CamSemi primary side sensing application.

2.10.1.1 Critical Connections

The tracks between the VDD and GND pins of the IC, and the decoupling capacitor must be as short as possible to avoid poor performance; shown in pink below.

The tracks between the FB resistors and GND pins must be as short as possible to avoid poor performance; shown in red below. The impedance driving the FB pin is quite high. As a result, the FB pin waveform can easily be distorted by parasitic capacitive coupling from the primary switch. When laying out the PCB, it is important to minimise stray capacitance between the switch and FB node. This can be achieved by placing the Rfb1 and Rfb2 resistors adjacent to the FB pin.

The tracks between the MOSFET gate and the GD pin of the IC must be as short as possible to avoid poor performance; shown in orange below.

The tracks between the transformer and MOSEFT drain must be as short as possible and the total area as small as possible to avoid poor performance; shown in green below.

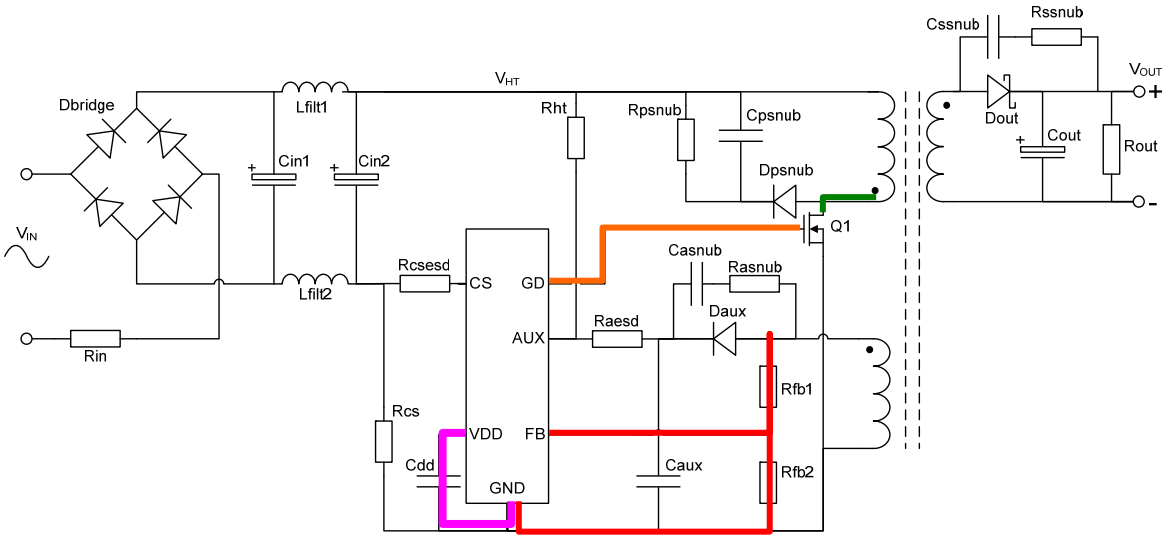

Figure 18: Critical Functional Layout Connections

2.10.1.2 Current Sense Resistor

The current sense resistor programs the power supply giving it the required rated current. The connection should be as small as possible and the track width as thick as possible. The current sense resistance is small and any track resistance will affect the operation of the power supply. The current sense path and resistors are marked in pink below.

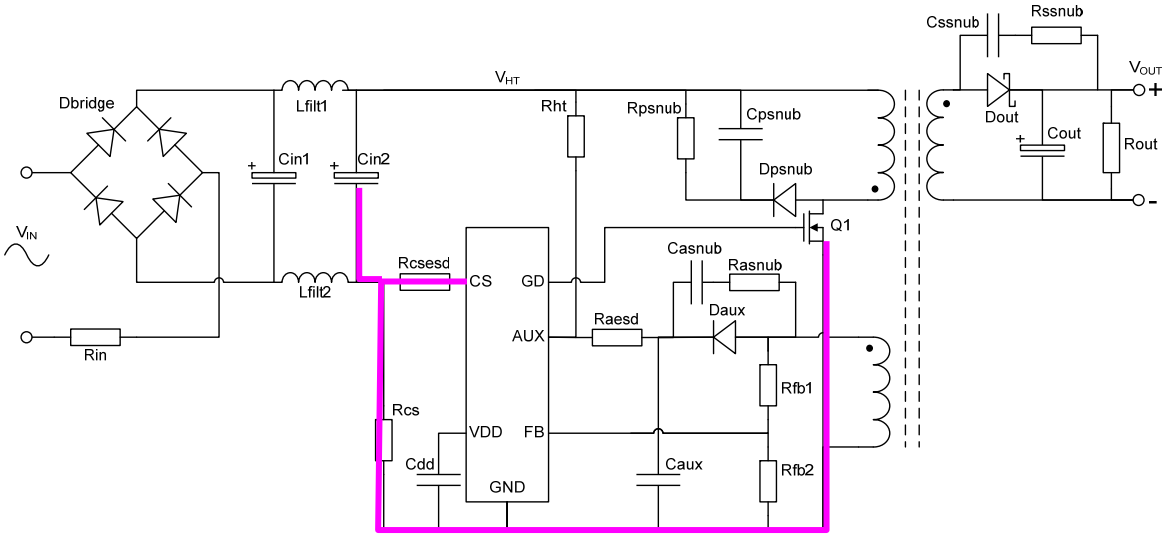

Figure 19: Current Sense Path Layout

2.10.2 EMC Considerations

2.10.2.1 Primary Current Path

The primary current loop must be kept as small as possible; shown in pink below.

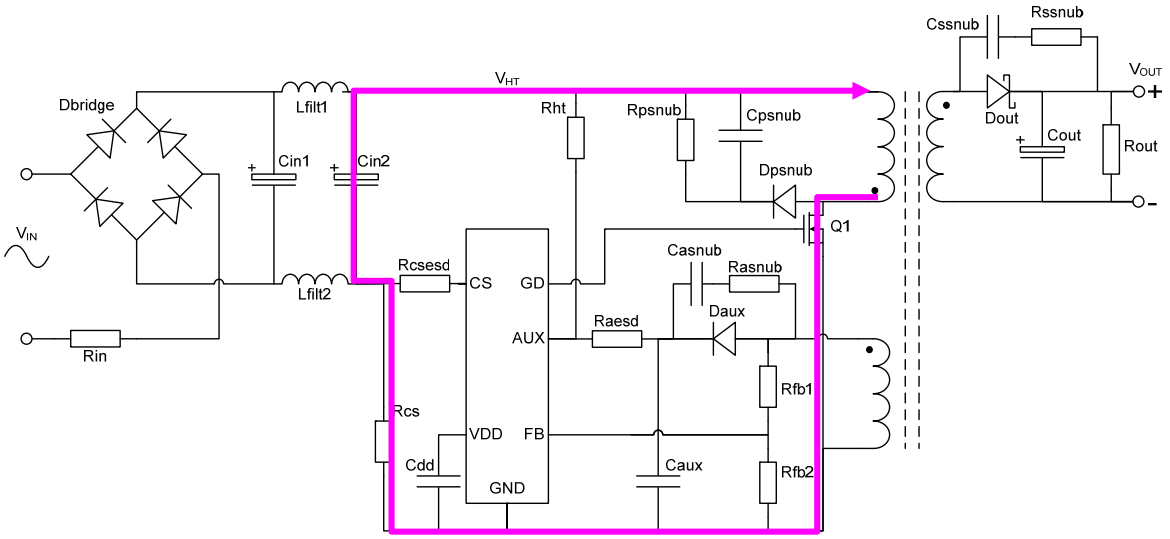

Figure 20: Primary Current Path Layout

2.10.2.2 Auxiliary Decoupling Path

The auxiliary power rail needs tightly decoupled to reduce any EMI resulting from the switching action of the MOSFET; shown in pink below.

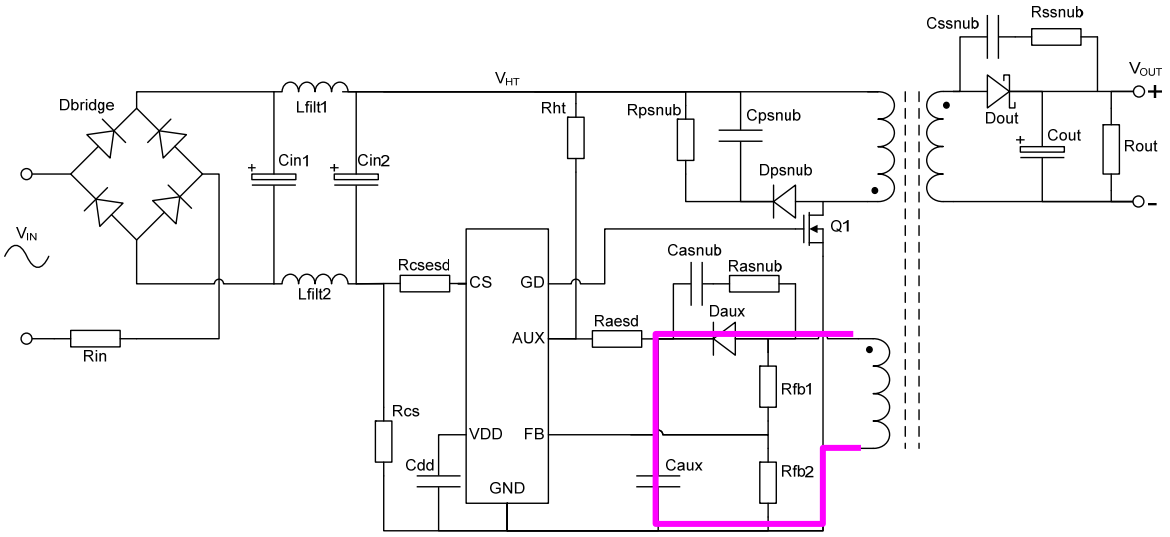

Figure 21: Auxiliary Decoupling Path Layout

2.10.2.3 Output Current Path

The output current path is where current from the output diode is smoothed by an output electrolytic capacitor to make a DC output and to reduce EMI. It is important that the path from diode to capacitor is as short as possible; shown in pink below.

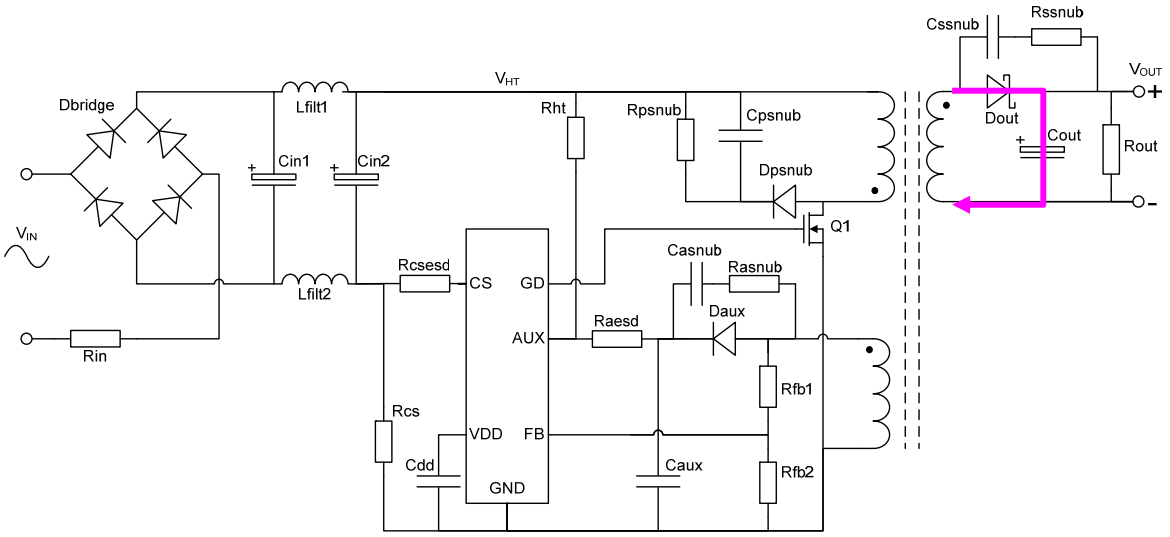

Figure 22: Output Current Path Layout

2.10.3 Thermal Considerations

Thermal management in enclosed power supplies can be very challenging, particularly in low-cost plug-top adapters/chargers. PCBs are generally single sided and do not have much copper to conduct heat away from hot spots. In a sealed plastic enclosure, there is no airflow so poor air circulation. The limited options for dispersing heat from particularly hot components are:

- Add all available PCB copper
- Keep components that get hot away from other components
- Use of 2oz copper boards and if possible double sided boards.

Thermal controls for two components in the C2183 design that can get particularly hot are covered in the following sections.

2.10.3.1 Primary Switch

The switching MOSFET switches through the primary winding of the transformer. To help keep the temperature down:

- Make pads as large as possible
- Make connections to pads as wide as possible to conduct heat away

These methods have little or no cost penalties. Another way to increase the copper at the MOSFET is by increasing the copper thickness, but this will carry a cost penalty. The switch is close to the transformer because of EMC and space requirements, but it is also a source of heat. This means a balance is required between having it further away for thermal reasons and close for EMC reasons.

It is also good practice to have some distance between the switching transistor and the nearest electrolytic bulk capacitor(s) to prevent the MOSFET from heating up the capacitor and hence shortening its life.

Note, using an IPAK MOSFET as the switching device is acceptable for applications up to about 4 W, above this:

- Use a larger MOSFET package (e.g. TO220) or
- Use a heat sink

2.10.3.2 Output Diode

The output diode can dissipate significant power due to the forward voltage drop and conducted output current, so consider the following when placing the diode:

1. Mounting the diode flat on the board:
    a. Keep the copper area of the cathode connection to transformer small
    b. Make the copper area of the anode connection as large as possible
2. Mounting the diode vertically:
    a. Put the diode body on the transformer side of the connection
    b. Keep the copper area small
    c. Make the opposite connection as large as possible in terms of copper area.
3. Using a surface mount diode:
    a. Provide a large copper area below and around the diode

2.10.4 Surge / ESD / EFT Considerations

The following components can be considered to help support surge / ESD / EFT requirements:

- Include spark gaps in the design to allow the events to bypass critical components and check ESD event takes place in the spark gap rather than any other place as shown below.

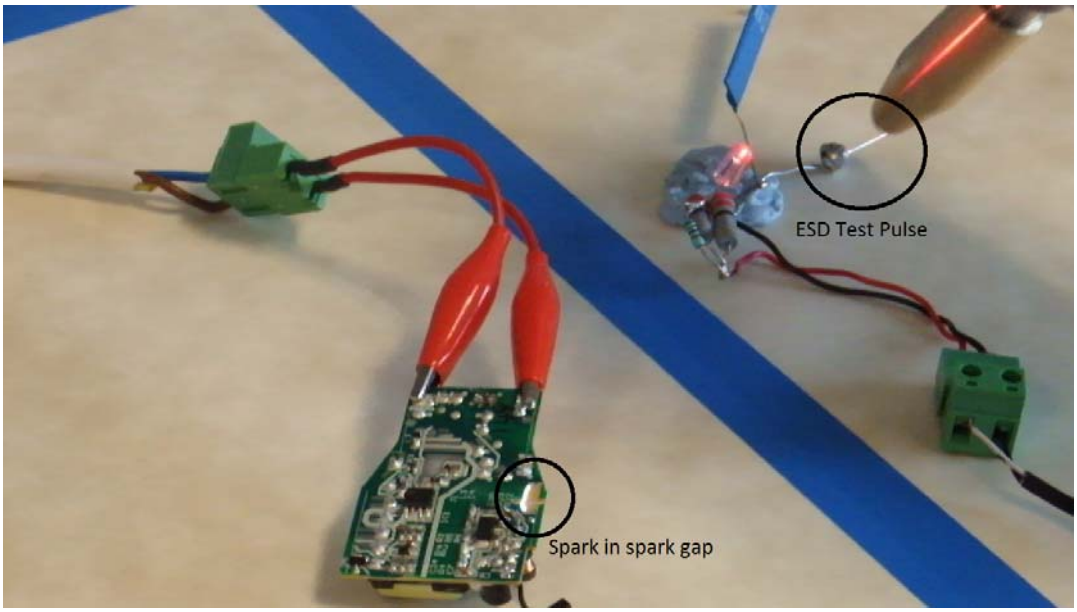

Figure 23: Check ESD Event Causes Spark in Spark Gap

- FB: Use a 0805 size for the top FB resistor component
- AUX: use a 47R resistor in series with the auxiliary circuit
- CS: place a 1k resistor between the CS resistor and CS pin
- Rin: use the recommended value 10R surge resistor for 2kV SURGE
- TX: Place two layers of tape around the flux band, if a flux band wire is used to ground the core

3 TROUBLESHOOTING

Here are a few steps to troubleshoot if the PSU does not work:

1. Ensure all winding directions in the transformer are correct
2. Measure the resistance between the following IC nodes. If the resistances measured are lower than expected, please resolve any issue before continuing to the next step.
    - Pin 1 to ground: Very high resistance should be seen
    - Pin 2 to Ground: Very high resistance should be seen
    - Pin 3 to Ground: Approximate resistance equal to parallel combination of feedback resistors
    - Pin 4 to Ground: Very high resistance should be seen.
    - Pin 5 to Ground: Approximate resistor value connected at CS pin (1k + Cs Resistor)
    - Pin 8 to Ground: Very high resistance should be seen
3. Apply 40 – 50 V at the input, and monitor the AUX and FB pin waveforms. The waveforms should behave as shown in Figure 24.

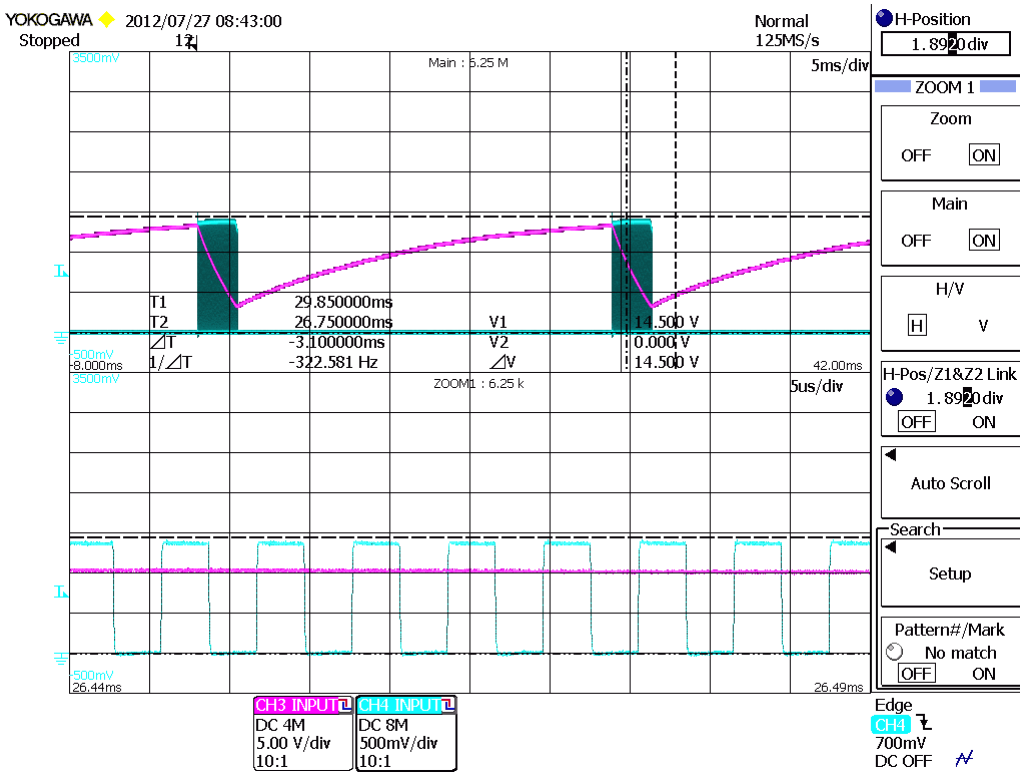

Figure 24: FB (blue) and AUX (pink) Pins When Input Mains = 40 - 50 V

4. Apply 120 – 150 V at the input and measure the FB signal. The controller provides a signal to indicate the cause of any shutdown event by driving the FB pin with a pulsed waveform of a particular duty cycle. The table below provides a list of the possible causes of a shutdown event and the resulting FB waveform duty cycle. If multiple faults occur at the same time then the duty cycle codes are added together. For example, if both Low Mains and OVP are detected as the causes of a shutdown event, then the FB signal duty cycle will be 0.5 + 0.25 = 0.75. Note the 50% duty cycle signal in Figure 24 as the controller detected a low input mains during the first switching pulse.

Shutdown Cause	FB Duty Cycle
Mains voltage low or missing fb signal	0.5
Output Over-Voltage Detected (>1.2xV_{FBREG})	0.25
LIGBT De-saturated so LIGBT has turned OFF before peak current detected, or missing CS pin signal	0.125
Controller maximum junction temperature exceeded (OTL)	0.06125

4 DESIGN EXAMPLE

Name	Symbol	Source	Design Example	Comments
CamSemi IC	IC	Calculated	C2183PX2-C	
Input Resistor	Rin	Assumption	3R3	
Input Capacitors	Cin1 + Cin2	Calculated	12 + 4.7 uF	Cin1+ Cin2 > Cin VDCMIN checked
Input Inductors	Lfilt1	Assumption	220u	
	Lfilt2	Assumption	NF	
Input Rectifier	Dbridge	Assumption	MBS6	
Current Sense Resistor	Rcs	Calculated	0.46	Common resistor value
CS ESD Protection	Rcsesd	Assumption	1k	
Primary Turns	N_P	Calculated	64	
Secondary Turns	N_S	Calculated	4	
Primary Inductance	L_P	Calculated	700 uH	
Auxiliary Turns	N_A	Calculated	7	= N_F
Output Circuit	Dout	Assumption	HSR5100	
	Rout	Calculated	18k	
	Cout	Assumption	1000 uF 25 V	
Output Snubber	Cssnub	Calculated	NF	
	Rssnub	Calculated	NF	
Primary Snubber	Rpsnub1	Assumption	100k	
	Cpsnub	Assumption	470 pF	
	Dpsnub	Assumption	GF1M	
	Rpsnub2	Assumption	100R	
VDD Capacitor	Cdd	Assumption	470 nF	
AUX Capacitor	Caux	Calculated	4.7 uF	
AUX Diode	Daux	Calculated	1N4148	
Auxiliary Snubber	Casnub	Assumption	NF	
	Rasnub	Assumption	NF	
AUX ESD Proteection	Raesd	Assumption	10R	
Start-up Resistors	Rht	Calculated	1.5M	
Feedback Resistors	Rfb1	Calculated	560R + 8k2	
	Rfb2	Calculated	2k4	
Primary Switch	Q1	Calculated	UTC4N60L	

5 IC DESCRIPTION

5.1 Flyback Topology

The following diagrams show the flyback topology circuit and typical waveforms.

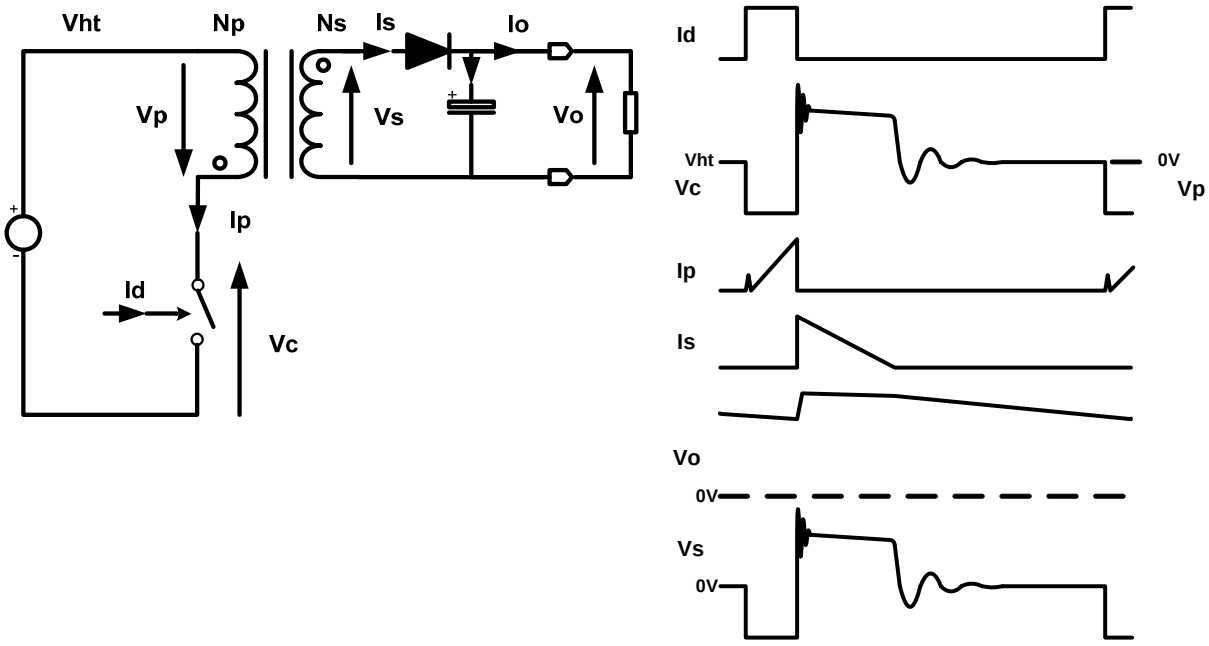

Figure 25: Flyback Topology and Waveforms

When using primary side sensing, the auxiliary winding contains output voltage information. A voltage divider placed directly across the AUX winding provides visibility of critical waveform features to allow accurate voltage measurement, including V_{HT}, the flyback voltage, period and resonant valleys.

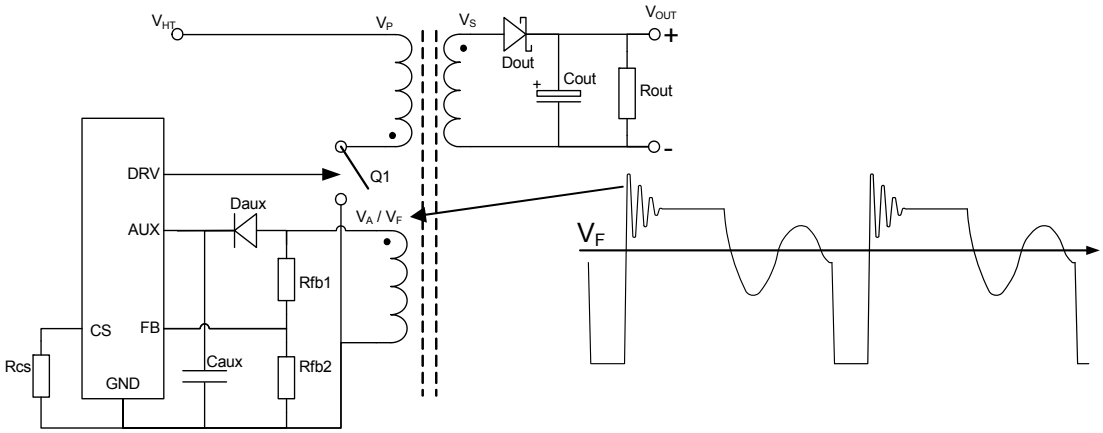

Figure 26: CamSemi Primary Side Sensing Topology and Waveform

5.2 Current and Voltage Regulation

The CamSemi controller regulation is peak current and switching frequency controlled, rather than duty cycle controlled. This allows a faster control loop, makes it independent of mains, ensures discontinuous mode operation and by limiting the peak current, avoids transformer saturation.

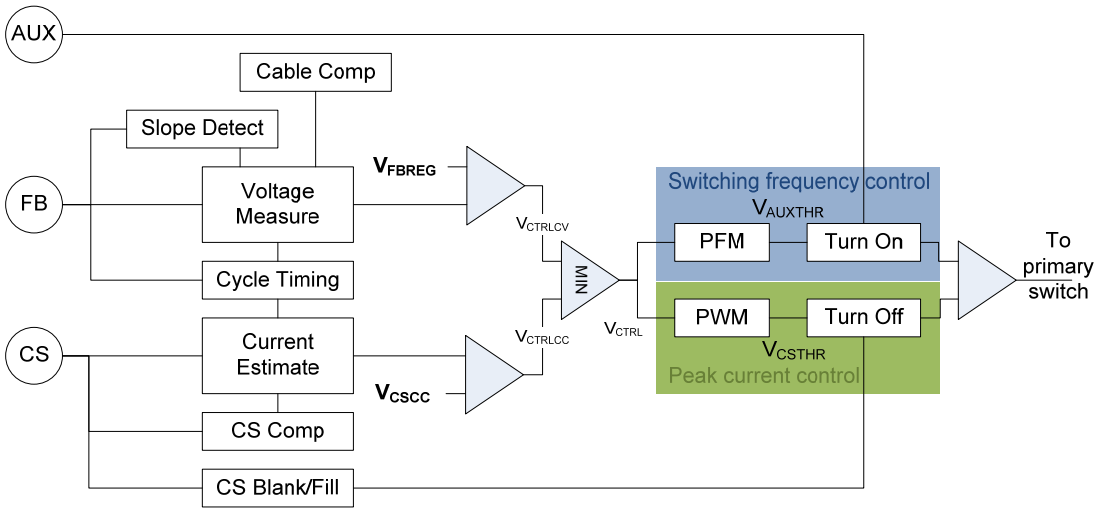

Figure 27: Current and Voltage Regulation Block Diagram

5.2.1 Output Voltage Measurement

Constant voltage regulation is achieved by sensing the voltage at the FB input, which is connected to the auxiliary or feedback winding. The waveform on the transformer feedback and secondary windings are identical, except for scaling by the turns ratio, N_F/N_S. The output voltage is only observable on the feedback winding during the flyback time, $t_{DCHARGE}$. When secondary current, I_S flows, the voltage drops across the diode and winding resistance cause an inaccuracy. Accurate voltage is measured when the secondary current falls to zero, coincident with zero flux in the transformer, because the voltage drop over the secondary circuit diminishes. This occurs at the 'Knee Point' and is the optimum time to get an accurate measurement of output voltage.

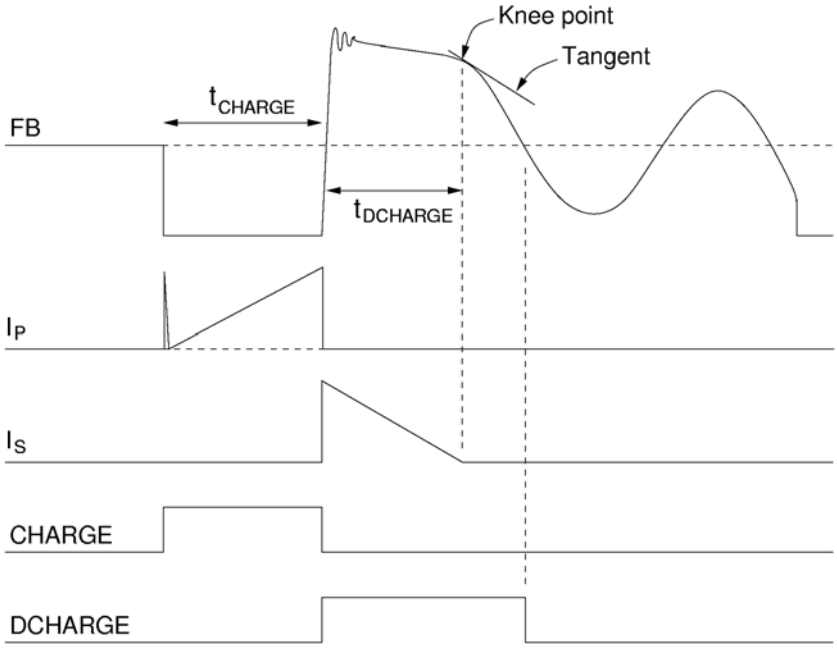

Figure 28: Voltage Detection Waveforms

To determine the knee point, various slope measurements are used as shown in Figure 29. In (a) the slope (dv/dt) is determined by the output current and circuit resistance, and is known based on given the power rating. In (b) the slope is determined by the resonant frequency of transformer, which is known and controlled

based on the transformer design. By selecting an on-chip reference slope (c) between these two slopes, it is possible to sample accurately the output voltage. The last slope detected before the FB waveform crosses 0 V will be the knee point.

The controller detects the slope and a sample and hold circuit is triggered at the knee point, t_{SAMP}. FB blanking is used to ignore the noise due to leakage inductance ringing.

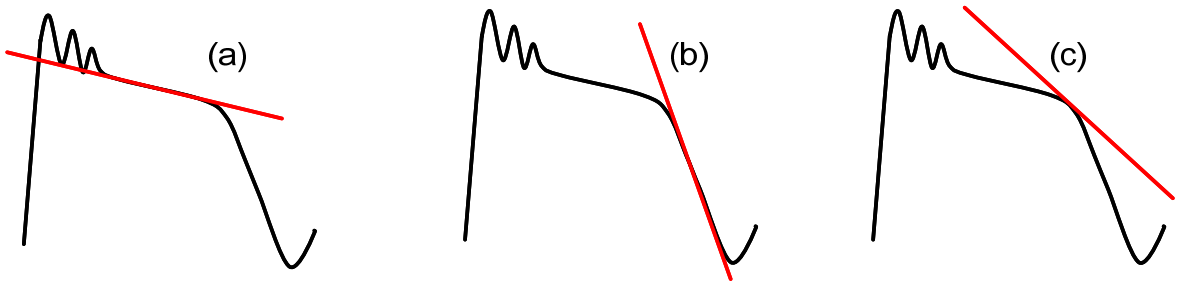

Figure 29: Tangent Detection Waveforms

The output voltage has the following relationship to the FB voltage based on the transformer and Rfb potential divider circuit (neglecting the output diode voltage).

$$V_{OUT} = V_F \cdot \frac{N_S}{N_F} = V_{FB} \cdot \frac{Rfb1 + Rfb2}{Rfb2} \cdot \frac{N_S}{N_F}$$

The application circuit is designed so that the FB resistors chosen allow the output voltage to be at its target value when the FB voltage is at V_{FBREG}.

$$V_{OUTCV} = V_{FBREG} \cdot \frac{Rfb1 + Rfb2}{Rfb2} \cdot \frac{N_S}{N_F}$$

Internally V_{FB} is compared to V_{FBREG} and a control voltage, V_{CTRLCV} is used to represent the power demand for the voltage loop.

5.2.1.1 FB Blanking

The oscillations due to the transformer at switch turn-off can cause false measurement triggers when the output voltage is low. The final slope detected before the FB signal crosses 0 V is taken as the knee point. When the output voltage is low, the transformer oscillations can cause the FB signal to cross 0 V before the full discharge phase is completed. This would result in a higher voltage knee point being detected.

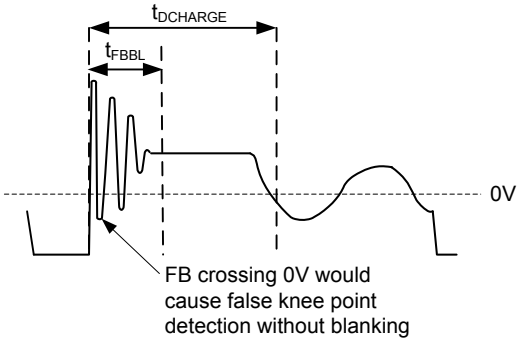

Figure 30: FB Blanking Time

To avoid false measurements, a blanking time is included to prevent any 0 V triggering. This time is set internally to the controller but takes into consideration the following:

- Maximum switching frequency, which determines the transformer design and hence transformer resonance oscillation profile
- CS input minimum threshold, V_{CSMIN}, which determines the minimum on-time, hence minimum DCHARGE time, $t_{DCHARGE}$.

The FB blanking time, t_{FBBL}, needs to be shorter than the minimum $t_{DCHARGE}$ to ensure good regulation, but needs to be long enough to ensure no false triggering due to transformer oscillations at turn-off.

5.2.2 Output Current Estimator

Current is monitored on the primary side via a current sense resistor, Rcs, providing a good measurement of the average primary current, $<I_P>$, and hence an estimate of the output current. The output current in terms of peak secondary side current, $I_{S(PK)}$, is given below; T is the switching period. The timings t_{CHARGE} and $t_{DCHARGE}$ are available from FB waveform as shown Figure 28.

$$I_{OUT} = \frac{1}{T} \cdot \frac{1}{2} \cdot I_{S(PK)} \cdot t_{DCHARGE} = \frac{t_{DCHARGE}}{2T} \cdot I_{S(PK)}$$

Since the flux and energy are conserved in the transformer, this can be transferred to the primary side; N is the transformer primary-to-secondary turns ratio; $I_{P(PK)}$ is the peak primary current during the CHARGE period.

$$I_{OUT} = \frac{t_{DCHARGE}}{2T} \cdot N \cdot I_{P(PK)}$$

The average primary current can be expressed in terms of the peak primary current:

$$\langle I_P \rangle = \frac{t_{CHARGE}}{2T} \cdot I_{P(PK)}$$

Giving a relationship between the output current and average primary current as:

$$I_{OUT} = N \frac{t_{DCHARGE}}{t_{CHARGE}} \langle I_P \rangle$$

Primary current generates a voltage across the current sense resistor, Rcs. The negative-going voltage is sensed by the CS input. The average primary current is equivalent to the average voltage seen on the CS pin, $<V_{CS}>$.

$$< I_P >= \frac{< V_{CS} >}{Rcs} \text{ so } I_{OUT} = N \frac{t_{DCHARGE}}{t_{CHARGE}} \frac{\langle V_{CS} \rangle}{Rcs}$$

The application circuit is designed so that the CS resistor chosen allows the output current to be at its target value when the primary side estimated output current is equal to Vcscc/Rcs.

$$I_{OUTCC} = \frac{N_P}{N_S} \frac{V_{CSCC}}{Rcs}$$

Internally the estimated output current, taken from $\frac{t_{DCHARGE}}{t_{CHARGE}} \cdot V_{CSCC}$, is compared to V_{CSCC} and a control voltage, V_{CTRLCC} is used to represent the power demand for the current loop.

5.2.3 Regulation

Both the current estimator and voltage measurement loops continuously determine whether more power is demanded. A minimum function on the control voltages is used to allow one of the loops to win.

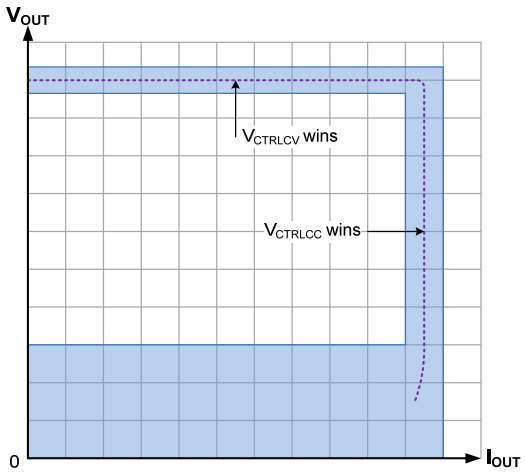

Figure 31: CV / CC Loop Minimum Function

For both voltage and current loops, the measured or estimated value is compared to the target and a control voltage is produced to indicate whether power is demanded. Depending on which loop wins, the associated control voltage, V_{CTRL} is used to determine the peak current (via PWM) and switching frequency (via PFM). They follow the characteristics of the plots shown below.

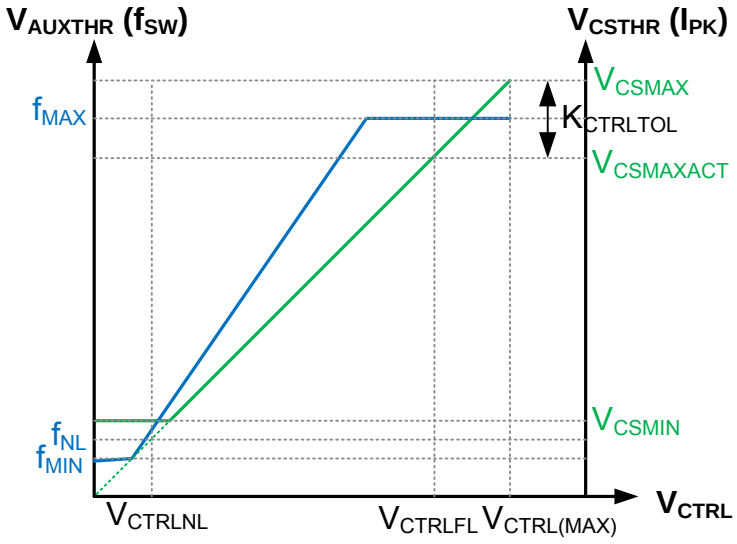

Figure 32: Switching Frequency and Peak Current Control

5.2.3.1 Peak Current Control

When the CS voltage exceeds a (negative) threshold (V_{CSTHR}) set by the control circuitry, the primary switch is turned off. The CS voltage threshold (V_{CSTHR}) varies from V_{CSMIN} to V_{CSMAX} during normal operation depending on the internal power demand signal V_{CTRL} from the CC or CV control loops.

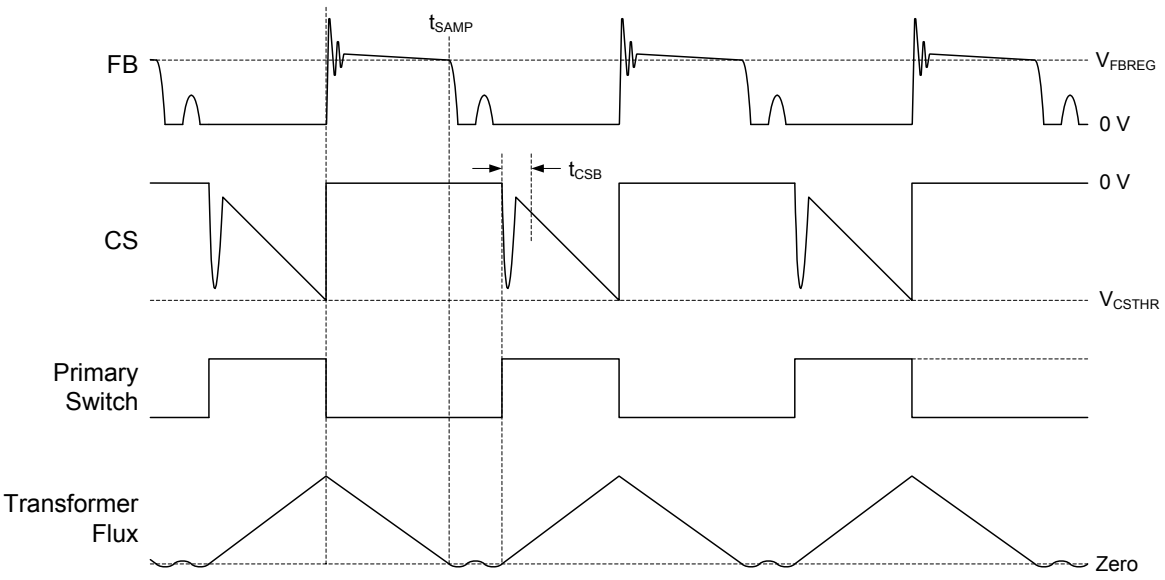

Figure 33: CS and FB Waveforms

During application design, the maximum CS threshold is chosen to run at a margin less than V_{CSMAX} by allowing a tolerance of $K_{CTRLTOL}$ to give $V_{CSMAXACT}$ as shown in Figure 32. This results in the maximum control voltage during full-load, V_{CTRLFL}, being lower than the maximum possible control voltage $V_{CTRL(MAX)}$. This headroom allows the peak current to be increased during transients to speed up recovery and to allow for component tolerances in production.

5.2.3.1.1 CS (Storage Time) Compensation

The switch does not turn off immediately so extra power would be delivered during the time that it takes the switch to turn off, t_{STORE}. The controller can see the difference between the requested turn off time and the actual turn off time using the CS pin voltage, so internally compensates by reducing V_{CSTHR} so that the peak current adjusts to the required value. The loop providing CS compensation is fast compared to the control loop.

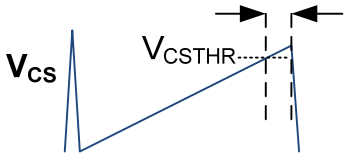

Figure 34: CS Compensation

5.2.3.1.2 CS Filler

The CS waveform is integrated to estimate the peak current, and is compared to the target threshold V_{CSTHR} to determine when the switch should be turned off. To avoid false triggering during the initial turn-on spike, this period is blanked for a fixed time of t_{CSB} as shown in Figure 35.

When running at low loads, a short on-time is required. To avoid missing the required turn-off point due to the blanking, the controller has a CS filler, which estimates the slope of the current during the blanking time as shown below. This prevents the peak current from being too high at low loads.

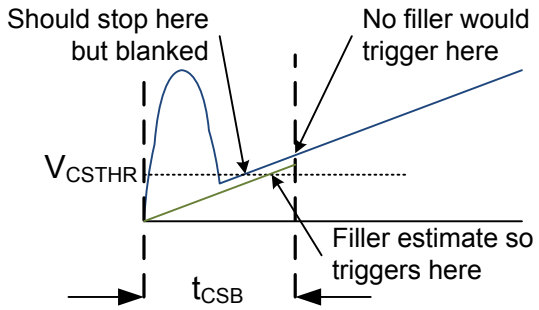

Figure 35: CS Filler

5.2.3.2 Switching Frequency Control

A pulse frequency modulator (PFM) using V_{AUX} determines the switching frequency based on the control voltage, V_{CTRL} signal as shown in Figure 36. During the idle period (after CHARGE and DISCHARGE are completed), V_{AUX} is allowed to fall a maximum of ΔV_{AUXPFM}. If the power demand is high, V_{CTRL} is high, so V_{AUX} triggers a new cycle before falling the full ΔV_{AUXPFM} range, hence the switching frequency is controlled. The maximum switching frequency is internally limited depending on the variant chosen.

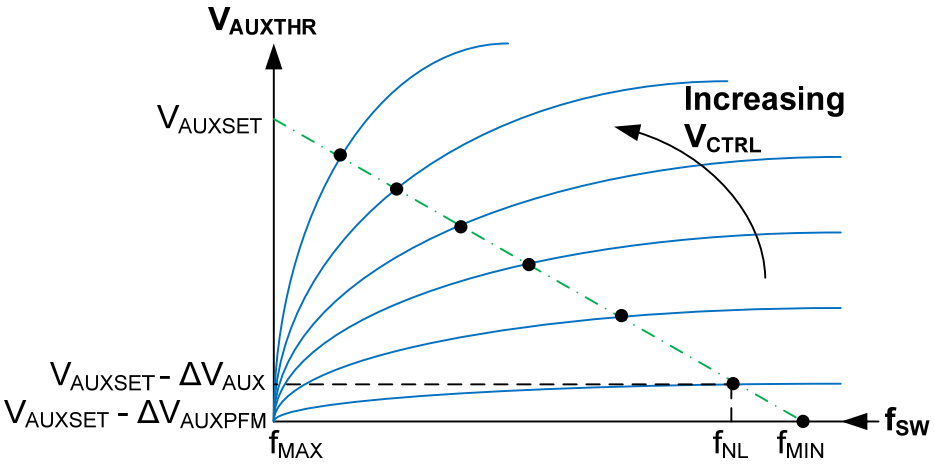

Figure 36: PFM Characteristics

The maximum V_{AUX} value is set by the transformer auxiliary-to-secondary turns ratio in the application circuit design to be V_{AUXSET} (ignoring output diode voltage drop). The maximum drop on V_{AUX} during no-load operation, ΔV_{AUX}, is determined by the value of Caux and the no-load operating frequency, f_{NL}. As the load is increased, the amplitude of the AUX voltage ripple reduces, hence increasing the switching frequency.

$$V_{AUXSET} = \frac{N_A}{N_S} V_{OUTCV} \qquad \Delta V_{AUX} = \frac{I_{AUXNL}}{Caux \cdot f_{NL}}$$

Note that the minimum switching frequency may not equal the no-load switching frequency. This allows headroom during a load step.

5.2.3.2.1 Auxiliary Control For No-Load

Using the PFM described above, the minimum frequency can be set by designing the application circuit using Caux, the auxiliary-to-secondary turns ratio and taking into account the current consumed by the control

circuitry. The design of the PFM ensures a gradual transition from the time dependent control voltage to a fixed minimum value required to maintain correct IC operation, which benefits no-load power behaviour.

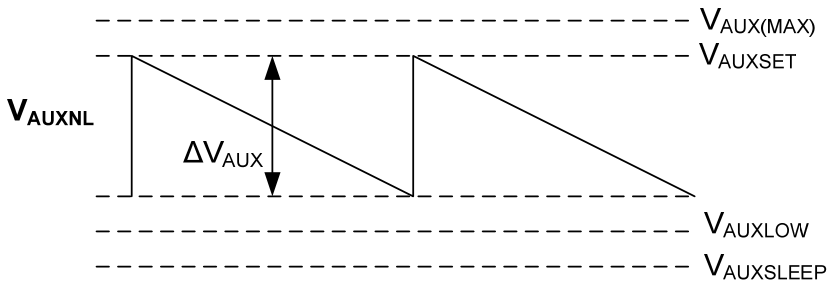

Figure 37: Auxiliary Voltage During No-Load

The PFM responds to relative movements in AUX voltage so the absolute level of V_{AUX} is not critical. Therefore, it should be possible to achieve low levels of no-load power over a wide range of V_{AUXSET} levels, which means the secondary-auxiliary turns ratio is less critical. Although it should be remembered that the level of no-load power will increase with AUX voltage because the power consumed by the IC rises linearly with AUX voltage, so it is still important to keep V_{AUX} low.

When V_{AUX} falls below V_{AUXLOW}, the controller requests a new cycle. This feature is for precaution and should not occur during steady-state operation. The controller will go to sleep if V_{AUX} falls below $V_{AUXSLEEP}$. The maximum AUX voltage, $V_{AUX(MAX)}$ is defined by the maximum voltage that the controller can handle on the AUX pin.

5.2.3.2.2 Cable Compensation

Cable compensation is fixed per variant. Based on the chosen level of cable compensation, the controller alters the voltage control signal produced during the comparison of V_{FB} to V_{FBREG}, thus making the necessary adjustment to compensate for the output voltage drop across the cable.

5.2.3.2.3 Quasi-Resonant Switching

The primary switch is only turned on when the voltage across it rings down to a minimum (voltage-valley, quasi-resonant switching). The effect of this is to reduce losses in the switch at turn-on. It also helps reduce EMI.

5.2.3.2.4 Duty Cycle Control

The full-load duty cycle is set by the primary-to-secondary turns ratio of the transformer. For a universal mains input power supply, full-load duty cycle is typically chosen to be 50% at the minimum (including ripple) of the rectified mains voltage (typically 80 V).

5.2.3.2.5 Frequency Dither and Edge Rate Control

The controller includes two additional features to reduce emissions and ease EMC compliance:

- Deliberate modulation of the switching frequency reduces measured levels of both quasi peak and average conducted emissions;
- Transition (edge) rate control of the primary switch driver reduces the rate of change of voltage on the primary switch during turn-on and hence reduces emissions.

5.3 Start-up

The controller begins in Sleep mode. When mains input voltage (V_{IN}) is applied, current flows through to the AUX node. Some of this current is consumed by the IC circuits as $I_{AUXSLEEP}$; the remainder charges capacitors Caux and Cdd.

Although the datasheet shows the IC starting based on the V_{AUX}, the internal circuits actually start based on the V_{DD} supply. V_{DD} is a level shifted version of V_{AUX} suitable for powering the lower power internal circuits. This makes the ratio of Caux to Cdd important. These should be scaled so that V_{DD} waking up the IC at V_{DDOVD} is around the time V_{AUX} reaches V_{AUXRUN}. At this point, the IC changes to Initialise mode. Current consumption increases to I_{AUXRUN} while internal circuits are enabled.

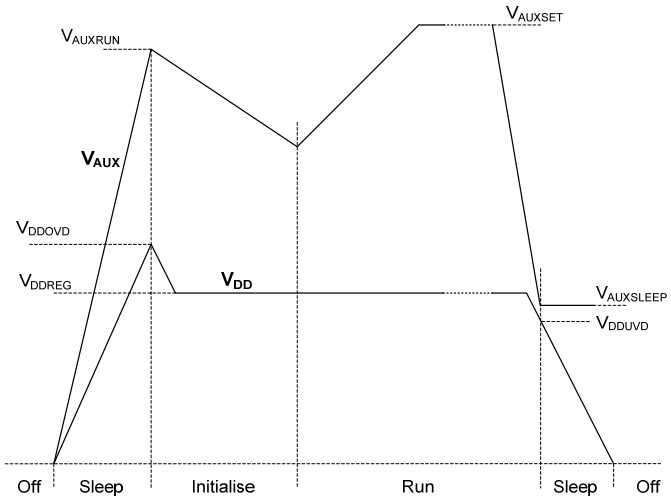

Figure 38: VDD and AUX During Start-up

When V_{DD} reaches V_{DDOVD}, a short drive pulse is output, during which time the voltage at FB is held at GND potential by current sourced from the FB pin. The current required to clamp the FB waveform to GND potential during the on-time of the primary switch depends on the rectified mains input voltage, the primary to feedback (or auxiliary if used for feedback) turns ratio, and resistor Rfb1. Analysis of this current enables the IC control circuit to compare the rectified mains input voltage with thresholds for allowing or preventing the next stage of power-up. The current flowing through (or voltage dropped across) Rfb1 is compared to internal thresholds to determine if the circuit is good to start.

If the input voltage is too low ($I_{FB} < I_{FBHTSTART}$), the IC will not issue further drive pulses, the AUX voltage will discharge to $V_{AUXSLEEP}$, at the same time V_{DD} discharges to V_{DDUVD}, and the power-up sequence will repeat.

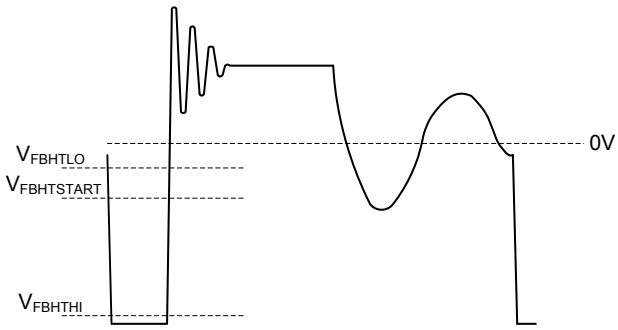

Figure 39: FB HT Reference Points

If the mains input voltage is high enough ($I_{FB} > I_{FBHTSTART}$), the IC will enter Run mode, further drive pulses will be output and V_{DD} will be regulated to V_{DDREG}. To achieve smooth power-up (monotonic rise in V_{OUT}), Caux

and Cdd must be large enough to power the control circuitry (during Initialise mode and the first few cycles of Run mode), until sufficient power is provided by the transformer auxiliary winding.

5.4 Protection Features

5.4.1 Input Under-Voltage Protection

Mains input under-voltage protection is triggered if the current sourced from the FB pin during the on-time is less than I_{FBHTLO} (shown as V_{FBHTLO} in Figure 39). This causes the control circuitry to stop issuing primary switch drive pulses, V_{AUX} reduces to $V_{AUXSLEEP}$ and the controller enters Sleep mode.

As described in the Troubleshooting section, this fault can be confirmed by monitoring the FB pin.

5.4.2 Input Over-Voltage Protection

Mains input over-voltage protection (OVP) is triggered if the current sourced from the FB pin during the on-time exceeds I_{FBHTHI} (shown as V_{FBHTHI} in Figure 39). The value of Rfb1 is chosen to ensure the mains input over-voltage protection is triggered when the mains rises above the desired threshold voltage ($V_{MAINSHI}$).

When triggered, the input OVP circuit reduces the target CV output voltage by 40%. This results in the reflected voltage on the primary being reduced and protecting the primary switch. In most applications, this will result in the output power being reduced too which also reduces the stress on the switch.

5.4.3 Output Over-Voltage Protection

The on-time of the primary switch is reduced if the output voltage tends to V_{OUTOVP}. The value depends on the set output voltage (V_{OUTCV}) and the FB OVP ratio:

$$V_{OUTOVP} = V_{OUTCV} \cdot G_{FBOVP}$$

As described in the Troubleshooting section, this fault can be confirmed by monitoring the FB pin.

5.4.4 Primary Switch Over Current Protection

The primary switch is turned off if the switch current as sensed by the CS input exceeds the effective threshold $V_{CSOCPEFF}$, subject to the minimum on-time T_{ONMIN}. The effective threshold $V_{CSOCPEFF}$ depends on a threshold V_{CSOCP} predefined by the controller, the CS signal rate of rise (dV_{CS}/dt), which is dependant on the application design, and the CS pin turn-off response time t_{CSOFF}. This gives pulse by pulse over current protection of the primary switch.

$$V_{CSOCPEFF} = V_{CSOCP}(\min) + \left(\frac{dV_{cs}}{dt} . t_{CSOFF} \right)$$

Also, if the controller sees the FB signal cross 0 V before the CS signal has reached V_{CSTHR}, as shown in Figure 40, the primary switch will be turned off early. This protects the switch if the cause is switch (de-)saturation or another type of single fault on the PCB.

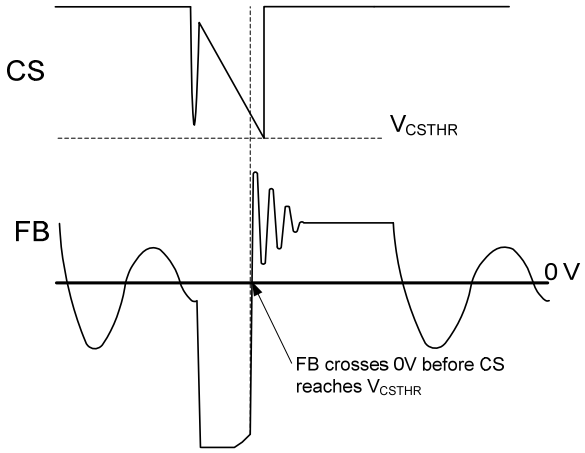

Figure 40: Switch Turn-off Before CS Threshold Reached

As described in the Troubleshooting section, this fault can be confirmed by monitoring the FB pin.

5.4.5 Over-Temperature Protection

The on-chip over-temperature protection (sometimes referred to as over-temperature lockout, OTL) is triggered if the junction temperature exceeds the threshold, T_{SH}. This causes the controller to shut down. To prevent possible damage to the PCB, there is hysteresis to prevent restart until the temperature reduces to ($T_{SH} – T_{SHHYST}$).

As described in the Troubleshooting section, this fault can be confirmed by monitoring the FB pin.

DESIGN GUIDE STATUS

Application design information and specifications provided in this Design Guide (e.g., circuit schematics, board layouts and custom wound component drawings) have not been fully developed for production and have not been subjected to safety or EMC approvals testing. Hence, design information contained herein should not be used for production without further development, verification, validation, approvals and certification appropriate for the intended application.

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