

C2M0045170D

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology
N-Channel Enhancement Mode

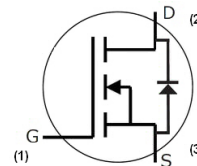


TO-247-3L



Features

- 2nd generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Resistant to latch-up
- Halogen free, RoHS compliant



Package Types: TO-247-3L
PN's: C2M0045170D

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Typical Applications

- Solar inverters
- Switch mode power supplies
- High voltage DC/DC converters
- Motor drive
- Pulsed power applications

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1700	v	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-10		+25		Transient	
Operational Gate-Source Voltage	V_{GSop}		-5/20			Static	Note 1
DC Continuous Drain Current	I_D			75	A	$V_{GS} = 20\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Fig. 19
				48		$V_{GS} = 20\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Note 2
Pulsed Drain Current	I_{DM}			160		t_{Pmax} limited by T_{Jmax} $V_{GS} = 20\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			338	W	$T_c = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +150	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 20V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


Electrical Characteristics ($T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700				$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4	V	$V_{DS} = V_{GS}, I_D = 18\text{ mA}$	Fig. 11
			2.5			$V_{DS} = V_{GS}, I_D = 18\text{ mA}, T_J = 150\text{ }^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		2	100	μA	$V_{DS} = 1700\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	I_{GSS}			600	nA	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$		40	70	m Ω	$V_{GS} = 20\text{ V}, I_D = 50\text{ A}$	Fig. 4,5,6
			80			$V_{GS} = 20\text{ V}, I_D = 50\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Transconductance	g_{fs}		24.7		S	$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}$	Fig. 7
			23.4			$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Input Capacitance	C_{iss}		3455		pF	$V_{GS} = 0\text{ V}$ $V_{DS} = 1200\text{ V}$ $f = 1\text{ MHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17,18
Output Capacitance	C_{oss}		171				
Reverse Transfer Capacitance	C_{rss}		6.7				
C_{oss} Stored Energy	E_{oss}		139		μJ		Fig. 16
Effective Output Capacitance (Energy Related)	$C_{o(er)}$		188		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0 \dots 1200\text{ V}$	Note: 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$		255		pF		
Turn-On Switching Energy (SiC Diode FWD)	E_{ON}		2.5		mJ	$V_{DS} = 1200\text{ V}, V_{GS} = -5/20\text{ V},$ $I_D = 50\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 99\text{ }\mu\text{H},$ $T_J = 150\text{ }^\circ\text{C},$ Using SiC Diode as FWD	Fig. 26, 29b Note 2
Turn Off Switching Energy (SiC Diode FWD)	E_{OFF}		1.4				
Turn-On Switching Energy (Body Diode FWD)	E_{ON}		4.9		mJ	$V_{DS} = 1200\text{ V}, V_{GS} = -5/20\text{ V},$ $I_D = 50\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 99\text{ }\mu\text{H},$ $T_J = 150\text{ }^\circ\text{C},$ Using MOSFET as FWD	Fig. 26, 29a Note 2
Turn Off Switching Energy (Body Diode FWD)	E_{OFF}		1.1				
Turn-On Delay Time	$t_{d(on)}$		68		ns	$V_{DD} = 1200\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 50\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega,$ Timing Relative to V_{DS} Inductive Load	Fig. 27, 29 Note 2
Rise Time	t_r		19				
Turn-Off Delay Time	$t_{d(off)}$		35				
Fall Time	t_f		19				
Internal Gate Resistance	$R_{G(int)}$		1.3		Ω	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	Q_{gs}		43		nC	$V_{DS} = 1200\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 50\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}		74				
Total Gate Charge	Q_g		200				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 1200 V.

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 1200 V.



Reverse Diode Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	3.8		V	$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}$	Fig. 8, 9, 10 Note 1
		3.4			$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Continuous Diode Forward Current	I_S		76	A	$V_{GS} = -5\text{ V}, T_C = 25\text{ }^\circ\text{C}$	Note 1
Diode Pulse Current	I_{SM}		160		$V_{GS} = -5\text{ V}$, Pulse Width t_p Limited by T_{Jmax}	Note 1
Reverse Recovery Time	t_{rr}	53		ns	$V_{GS} = -5\text{ V}, I_{SD} = 50\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 1000\text{ A}/\mu\text{s}, T_J = 150\text{ }^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	461		μC		
Peak Reverse Recovery Current	I_{rrm}	14		A		
Reverse Recovery Time	t_{rr}	40		ns	$V_{GS} = -5\text{ V}, I_{SD} = 50\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 3040\text{ A}/\mu\text{s}, T_J = 150\text{ }^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	481		μC		
Peak Reverse Recovery Current	I_{rrm}	22		A		

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.25	0.37	$^\circ\text{C}/\text{W}$		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$		40			



Typical Performance

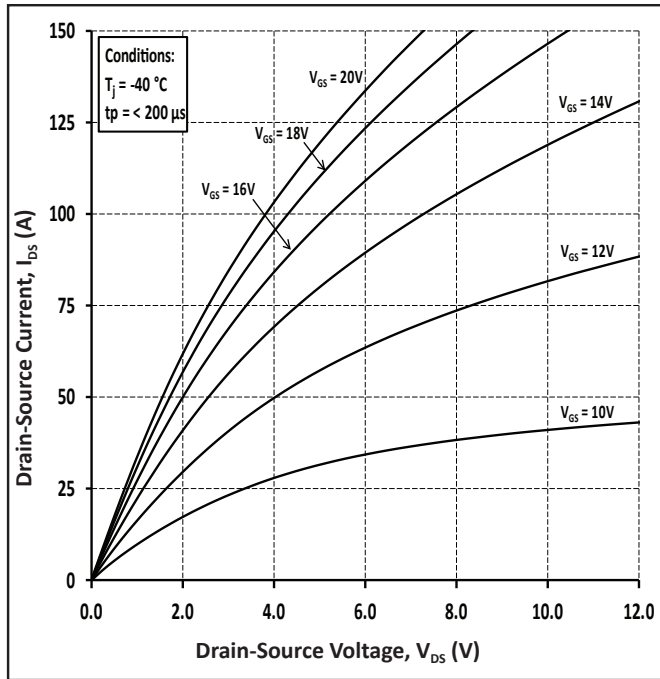


Figure 1. Output Characteristics $T_j = -40\text{ }^\circ\text{C}$

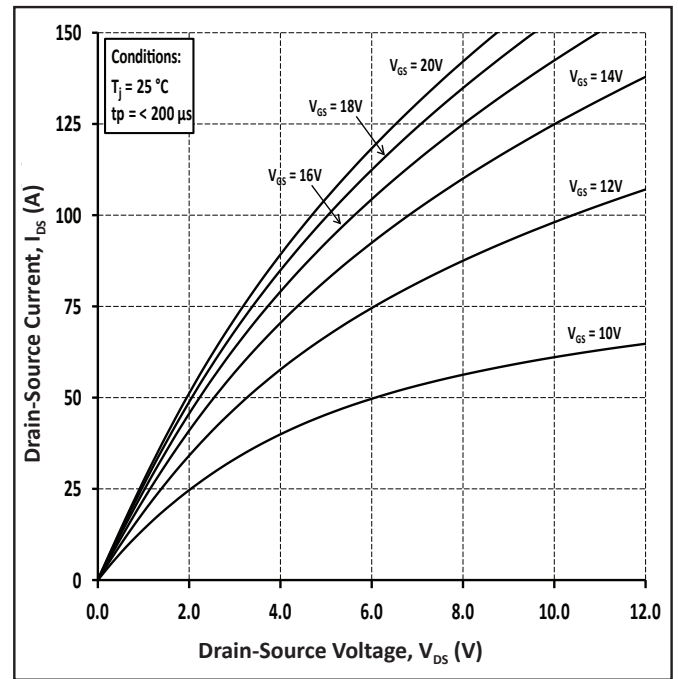


Figure 2. Output Characteristics $T_j = 25\text{ }^\circ\text{C}$

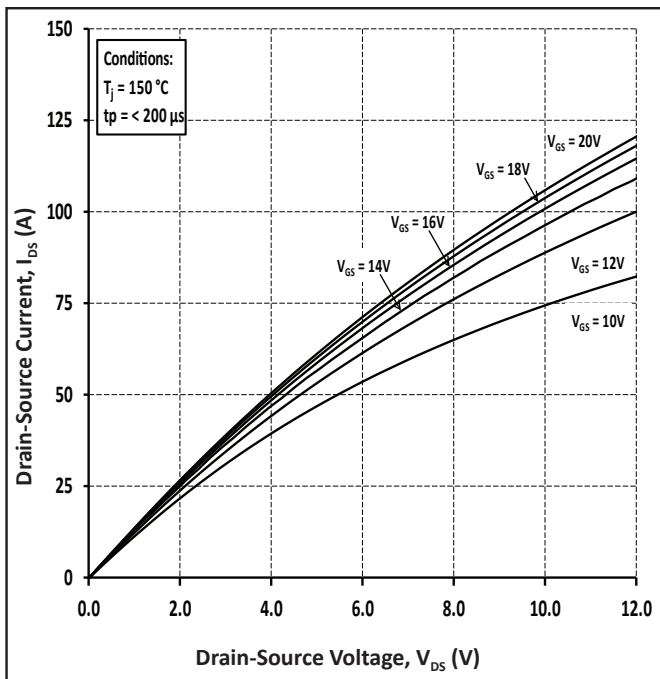


Figure 3. Output Characteristics $T_j = 150\text{ }^\circ\text{C}$

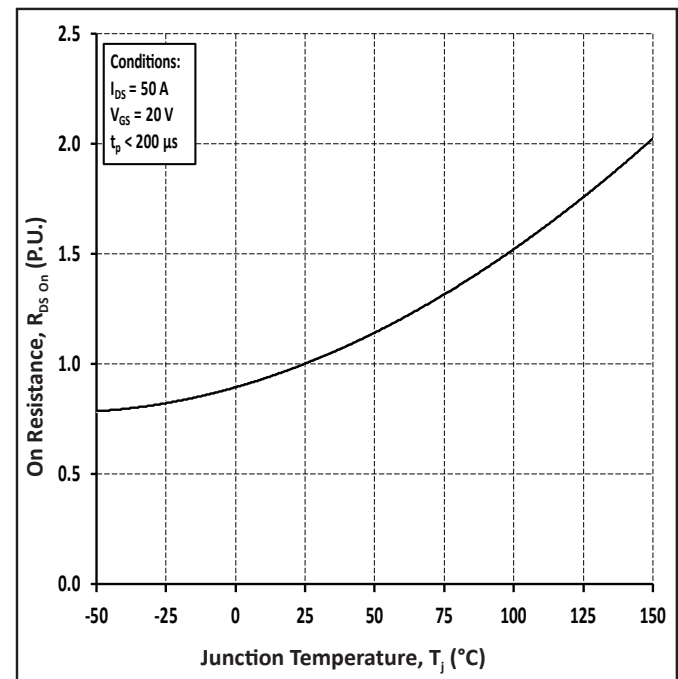


Figure 4. Normalized On-Resistance vs Temperature



Typical Performance

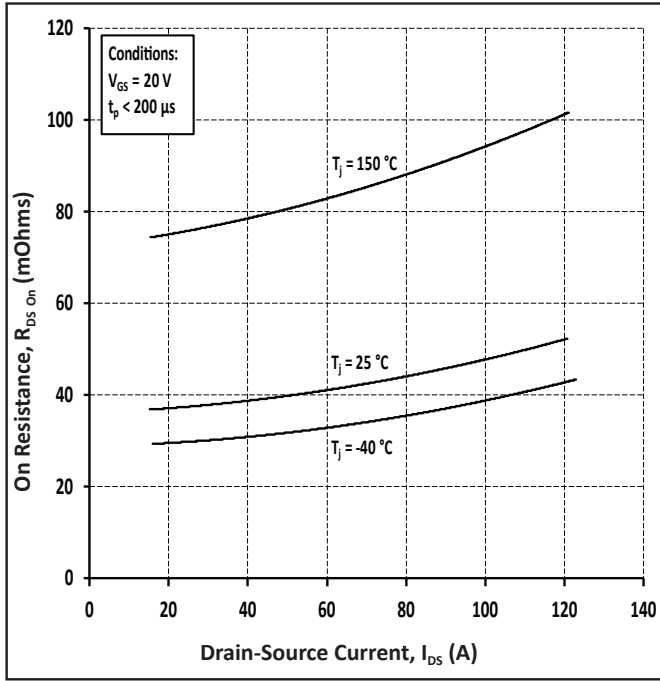


Figure 5. On-Resistance vs Drain Current for Various Temperatures

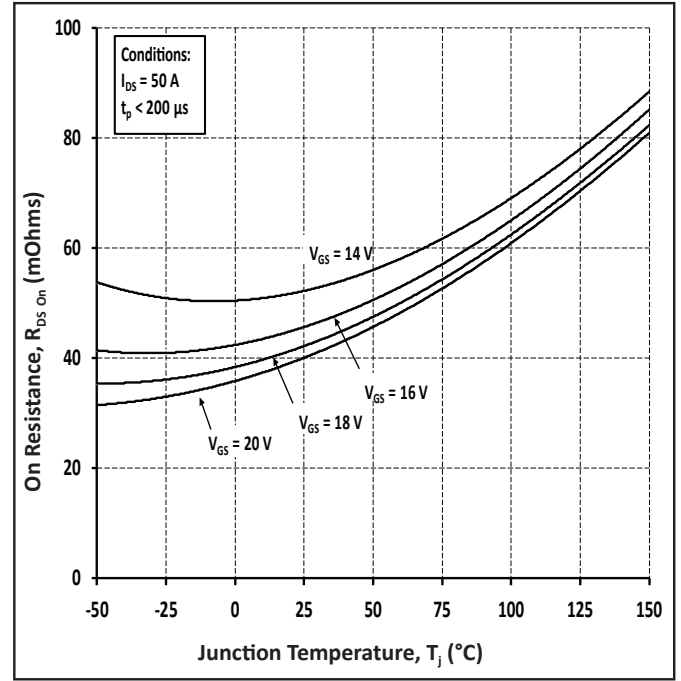


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

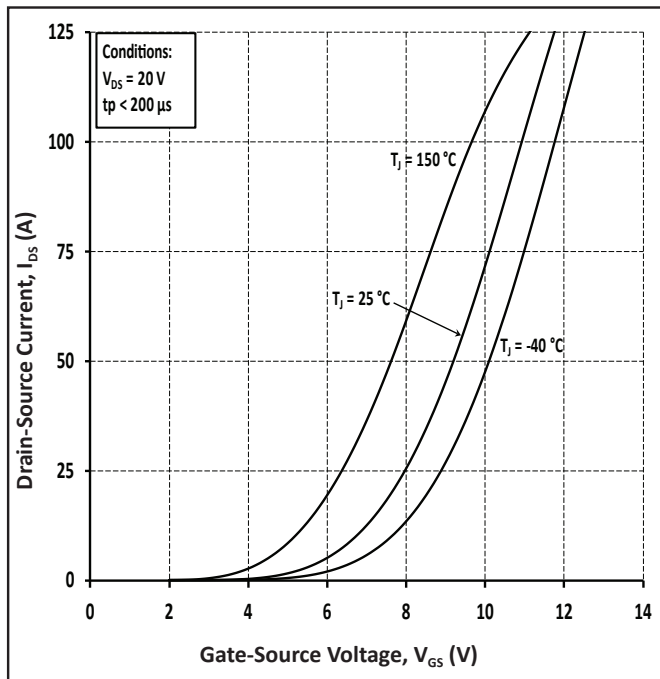


Figure 7. Transfer Characteristic for Various Junction Temperatures

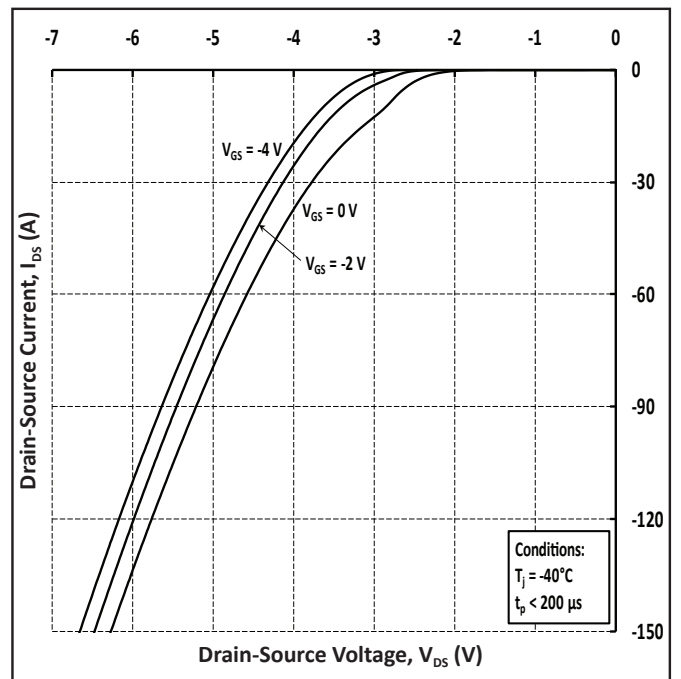


Figure 8. Body Diode Characteristic at -40 °C



Typical Performance

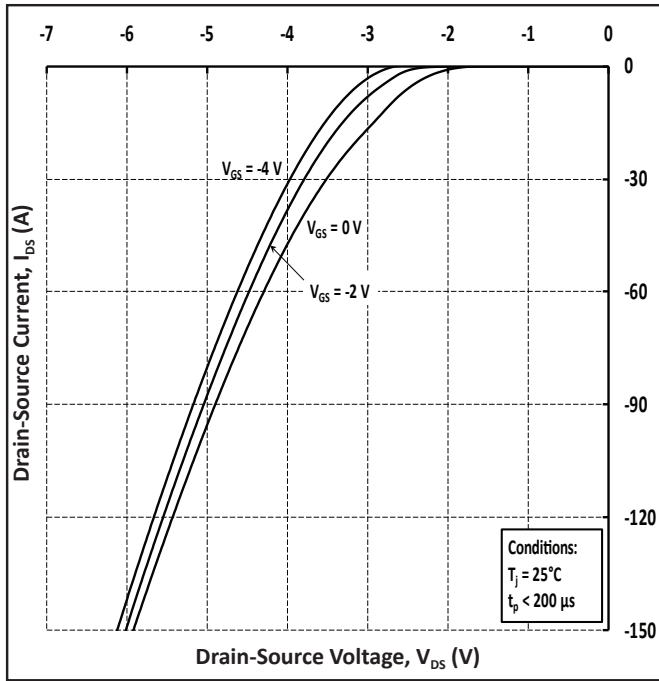


Figure 9. Body Diode Characteristic at 25 °C

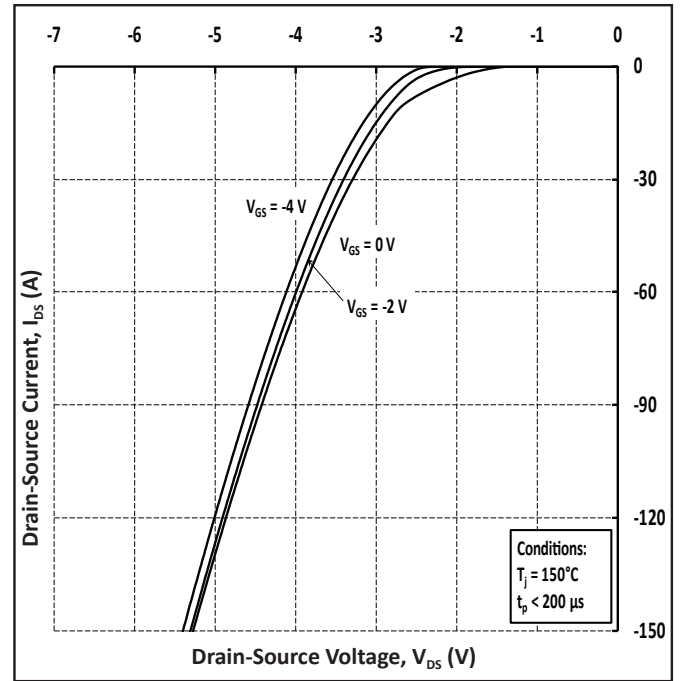


Figure 10. Body Diode Characteristic at 150 °C

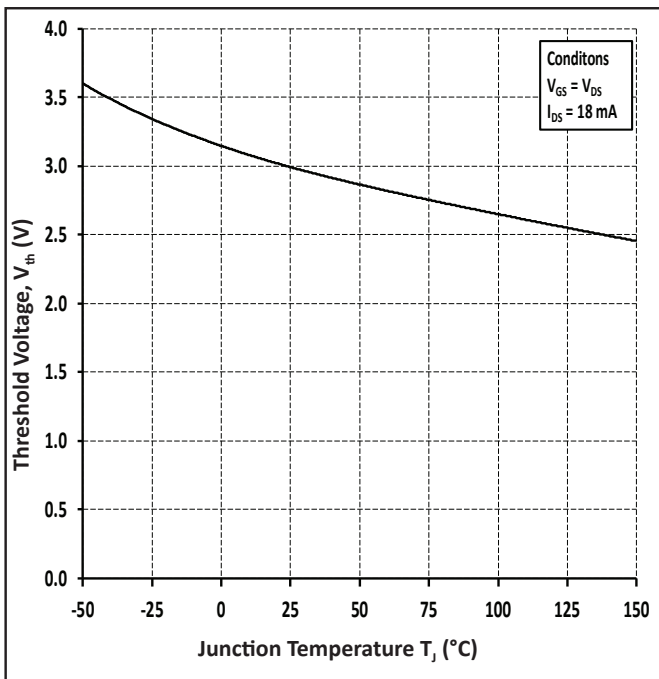


Figure 11. Threshold Voltage vs Temperature

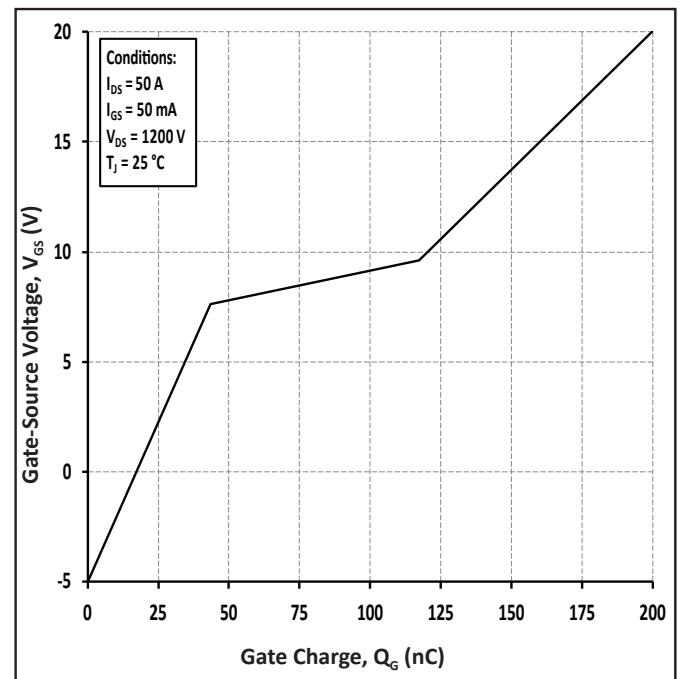


Figure 12. Gate Charge Characteristic



Typical Performance

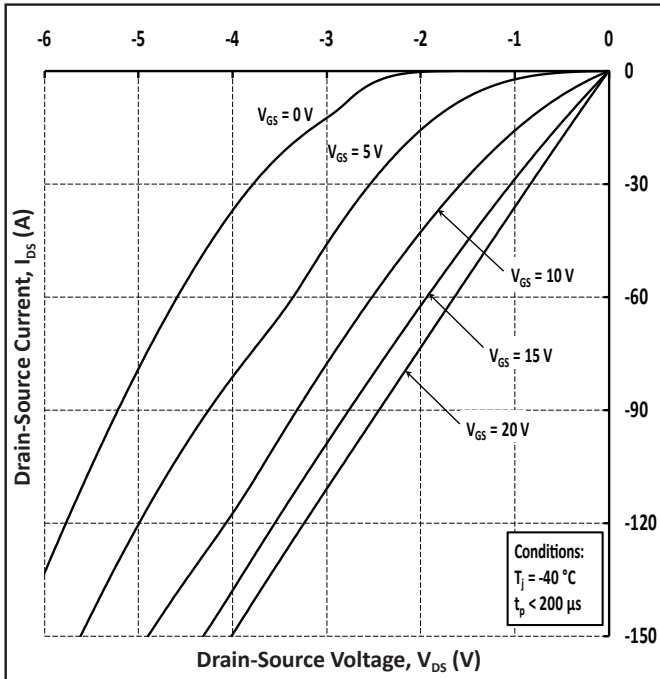


Figure 13. 3rd Quadrant Characteristic at $-40\text{ }^\circ\text{C}$

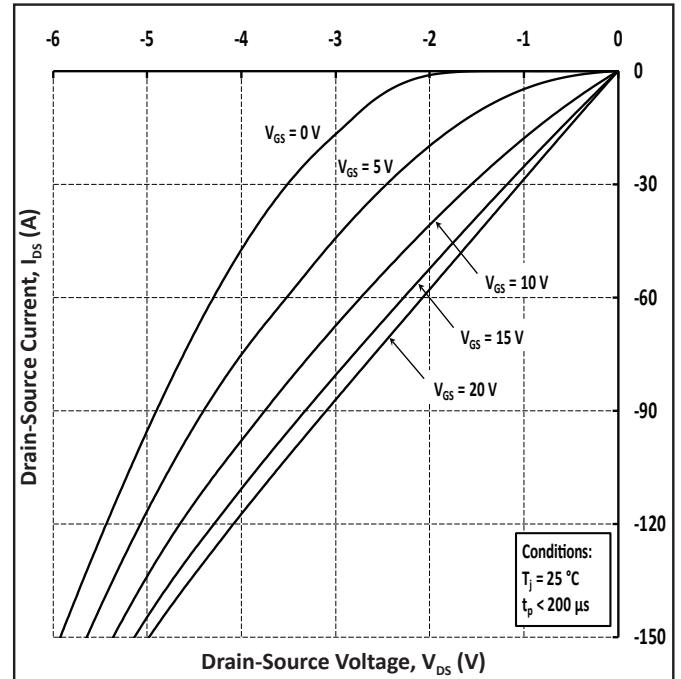


Figure 14. 3rd Quadrant Characteristic at $25\text{ }^\circ\text{C}$

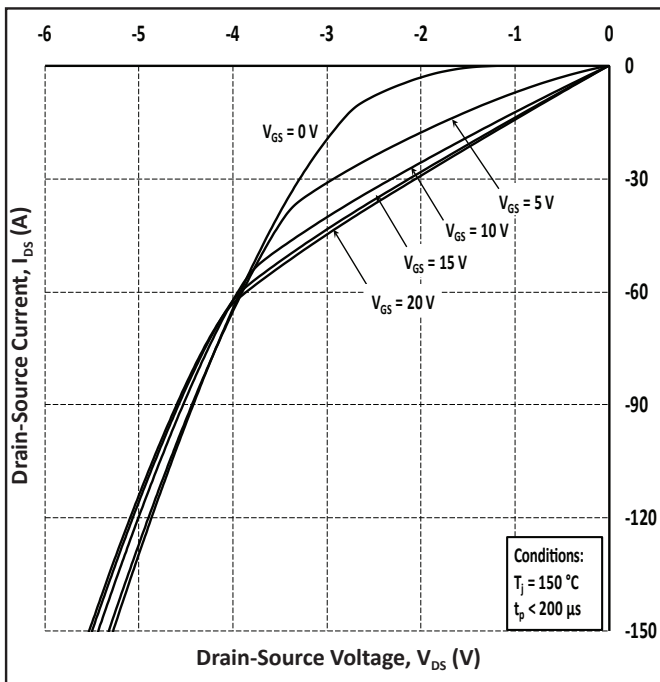


Figure 15. 3rd Quadrant Characteristic at $150\text{ }^\circ\text{C}$

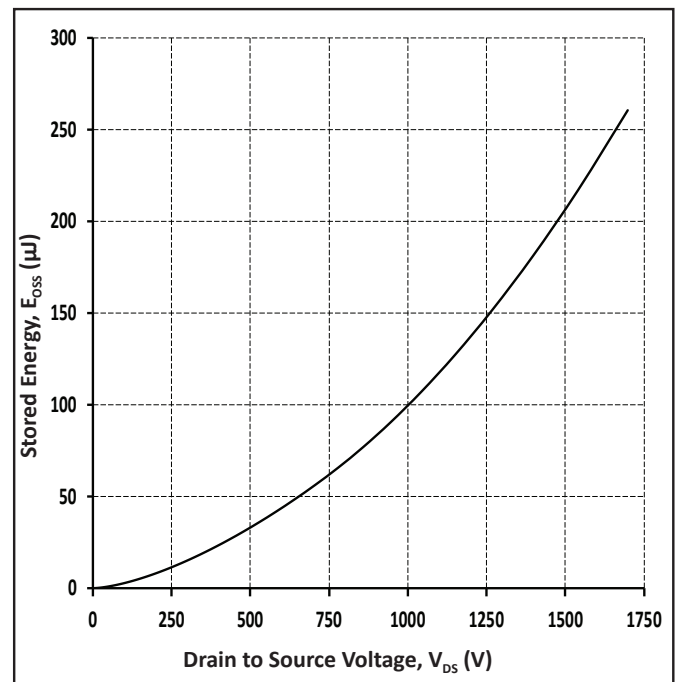


Figure 16. Output Capacitor Stored Energy



Typical Performance

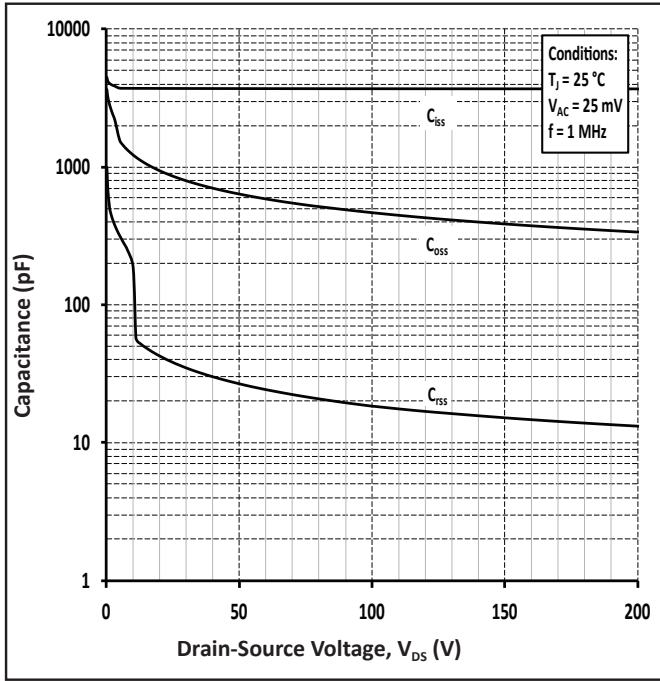


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

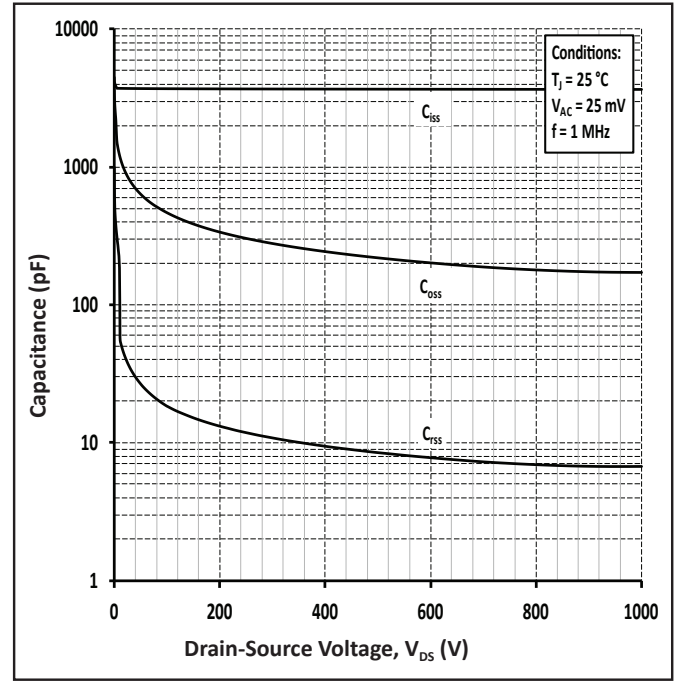


Figure 18. Capacitances vs Drain-Source Voltage (0-1000 V)

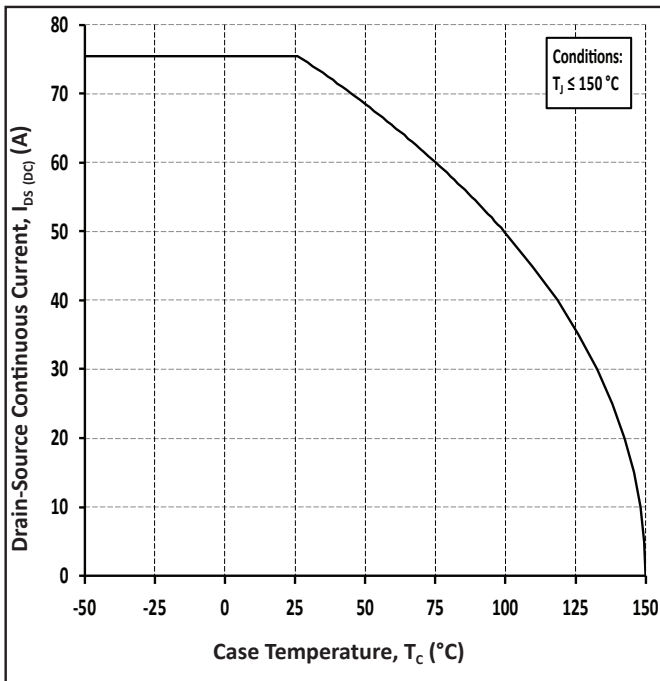


Figure 19. Continuous Drain Current Derating vs Case Temperature

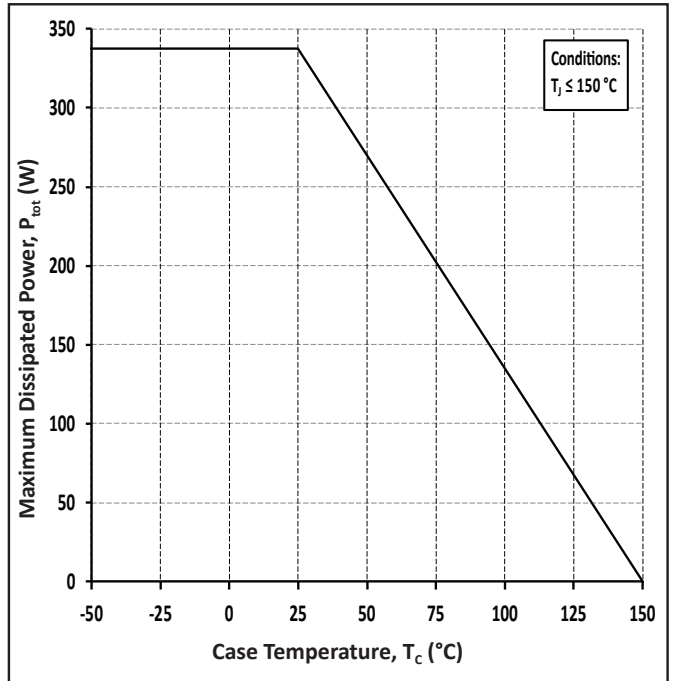


Figure 20. Maximum Power Dissipation Derating vs Case Temperature

Typical Performance

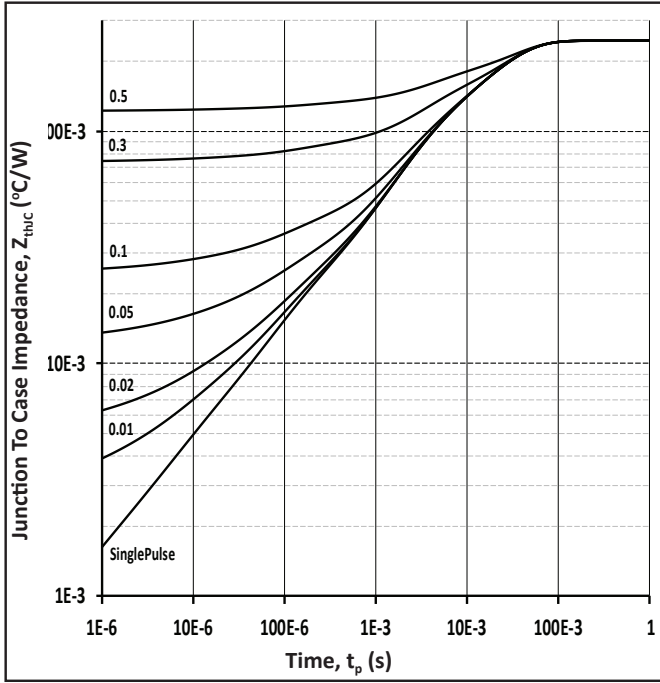


Figure 21. Transient Thermal Impedance (Junction - Case)

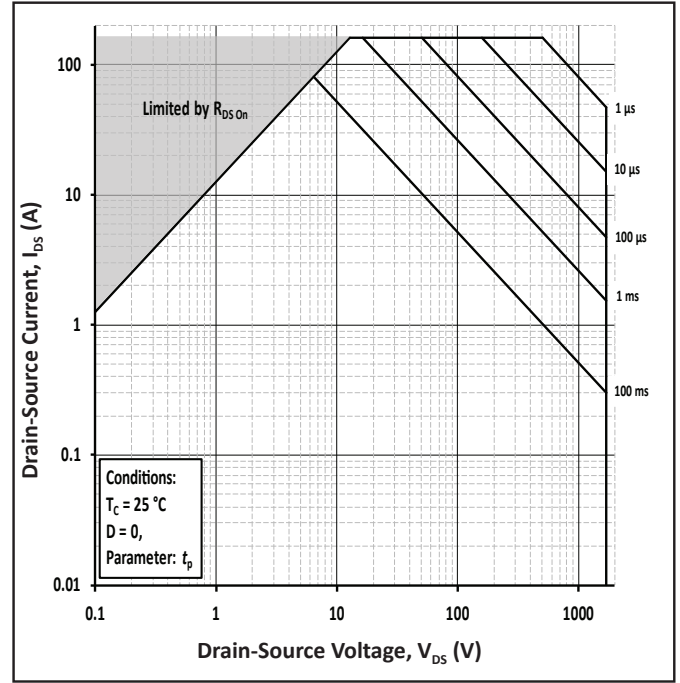


Figure 22. Safe Operating Area

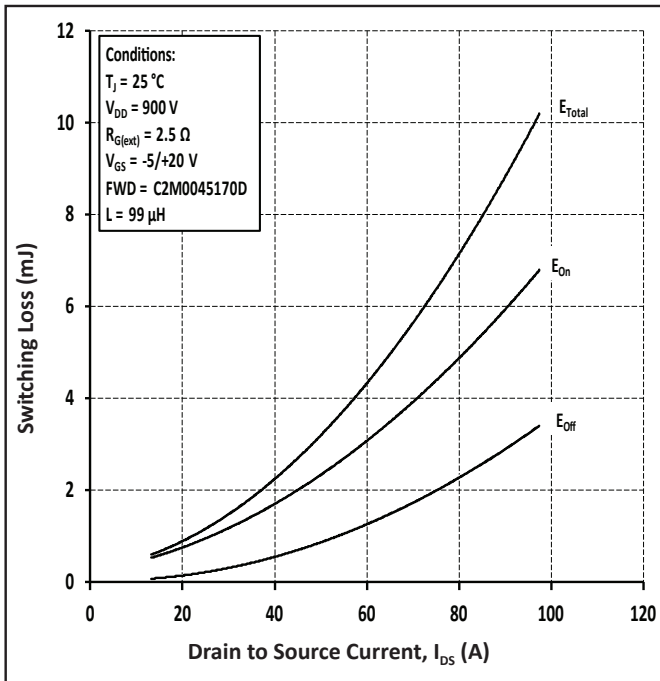


Figure 23. Clamped Inductive Switching Energy vs Drain Current ($V_{DD} = 900\text{ V}$)

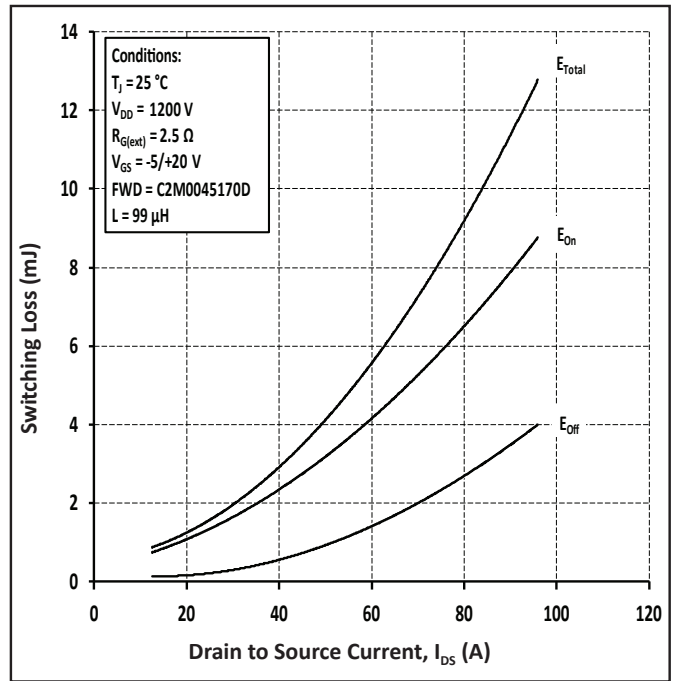


Figure 24. Clamped Inductive Switching Energy vs Drain Current ($V_{DD} = 1200\text{ V}$)



Typical Performance

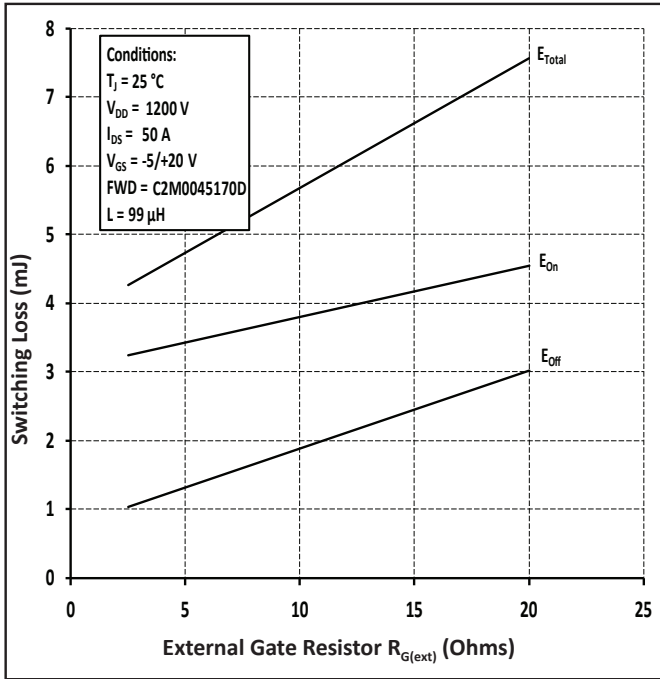


Figure 25. Clamped Inductive Switching Energy vs $R_{G(ext)}$

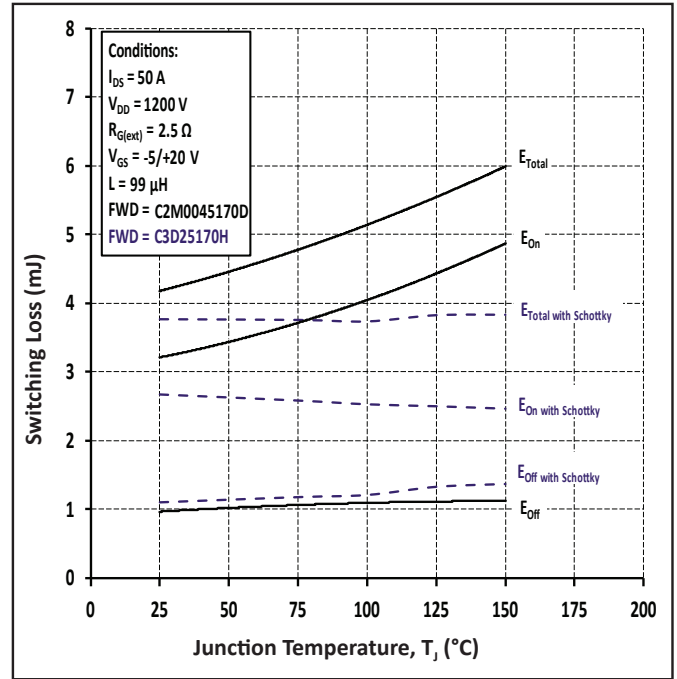


Figure 26. Clamped Inductive Switching Energy vs Temperature

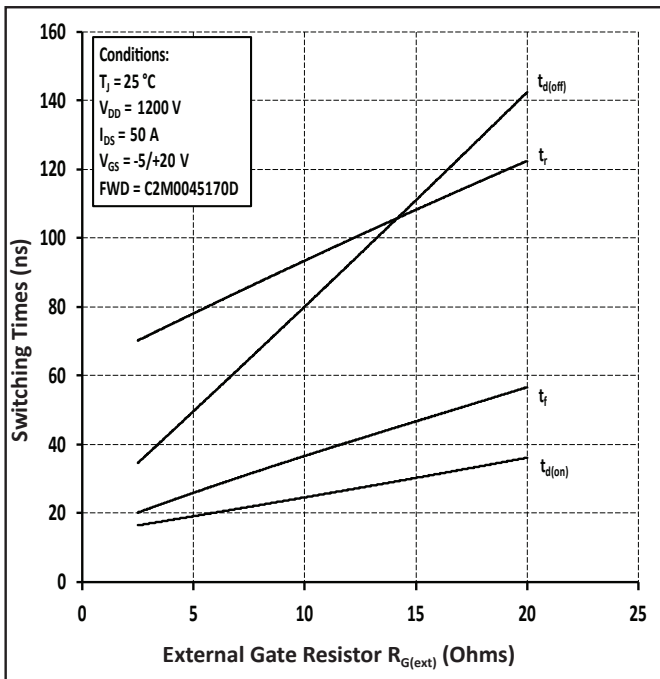


Figure 27. Switching Times vs $R_{G(ext)}$

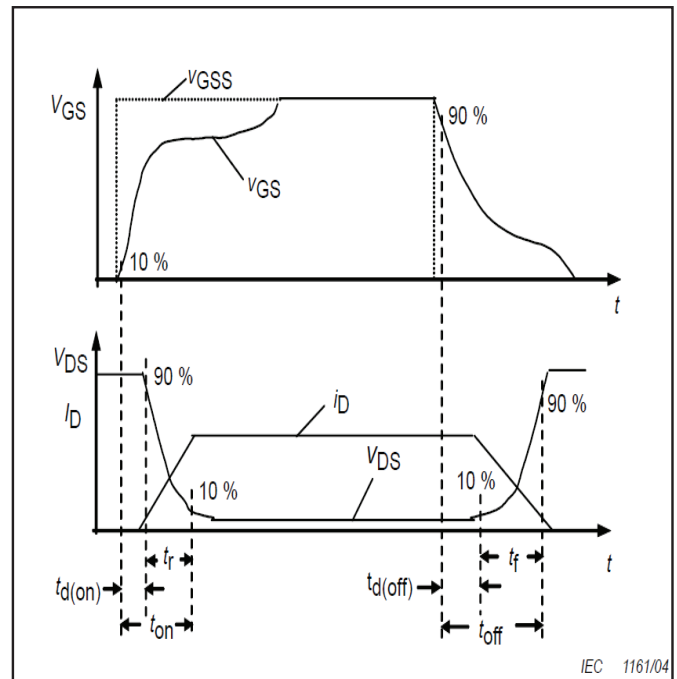


Figure 28. Switching Times Definition



Test Circuit Schematic

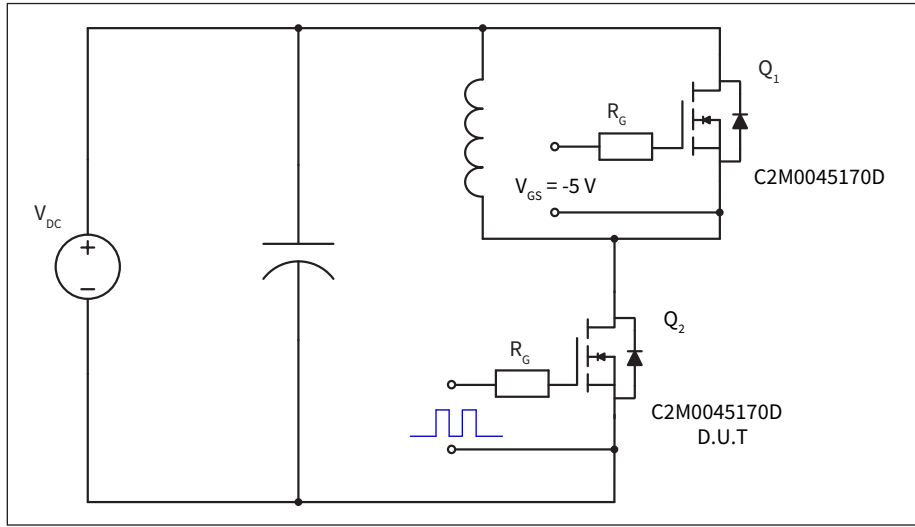


Figure 29a. Clamped Inductive Switching Test Circuit Using MOSFET Intrinsic Body Diode

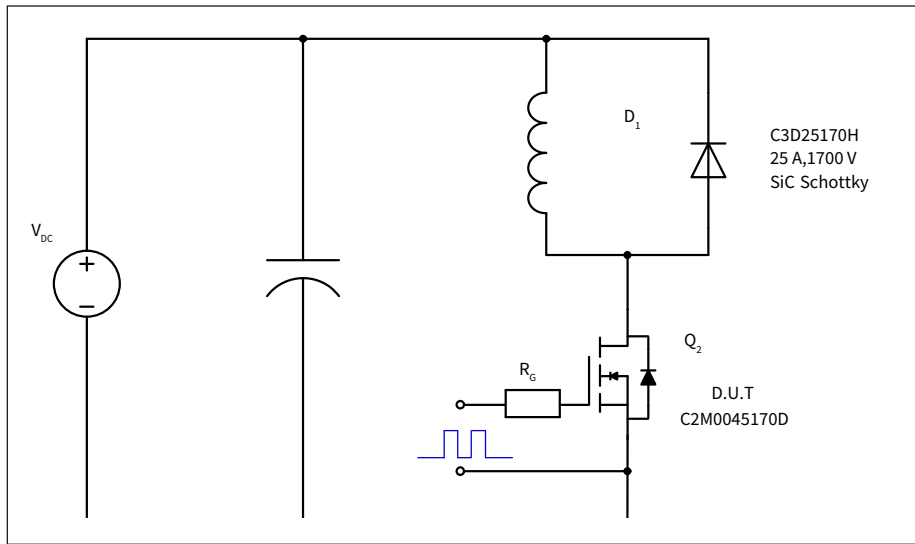
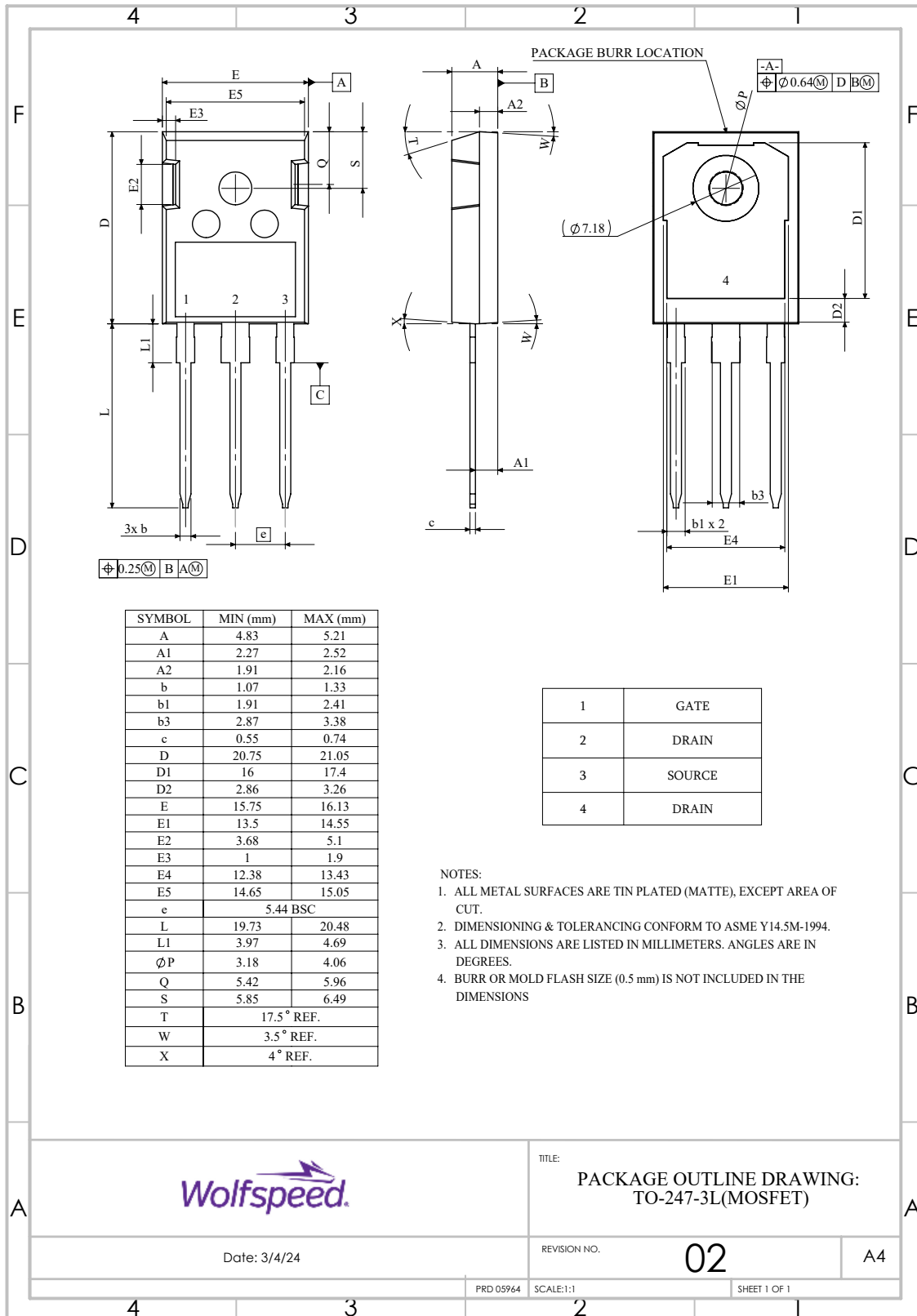


Figure 29b. Clamped Inductive Switching Test Circuit Using SiC Schottky Diode



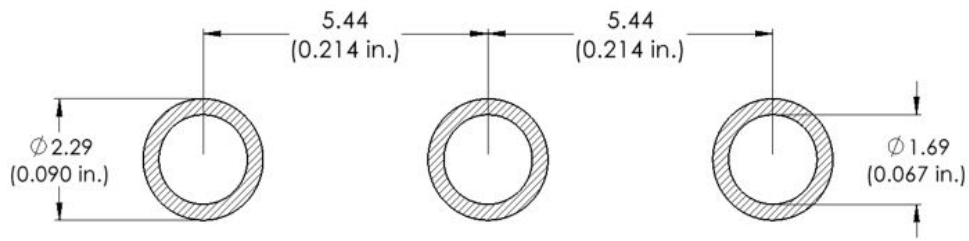
Package Dimensions

Package: TO-247-3L





Recommended Solder Pad Layout





Revision History

Current Revision	Date of Release	Description of Changes
0	May-2022	Initial Release
1	November-2023	Updated Wolfspeed branding, package drawing, and solder pad layout
2	February-2024	Qrr units corrected to uC
3	October - 2024	Legal Disclaimer, POD, Table 1 layout, Diode Pulse Current Symbol



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