C2P Inc.

MODEL No: C2P0347AMG-2

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Record of Revision

Date	Revision No.	Summary
2011-06-02	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of C2P0347AMG-2 active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 3.47'' display area contains 320(RGB) x 480 pixels.

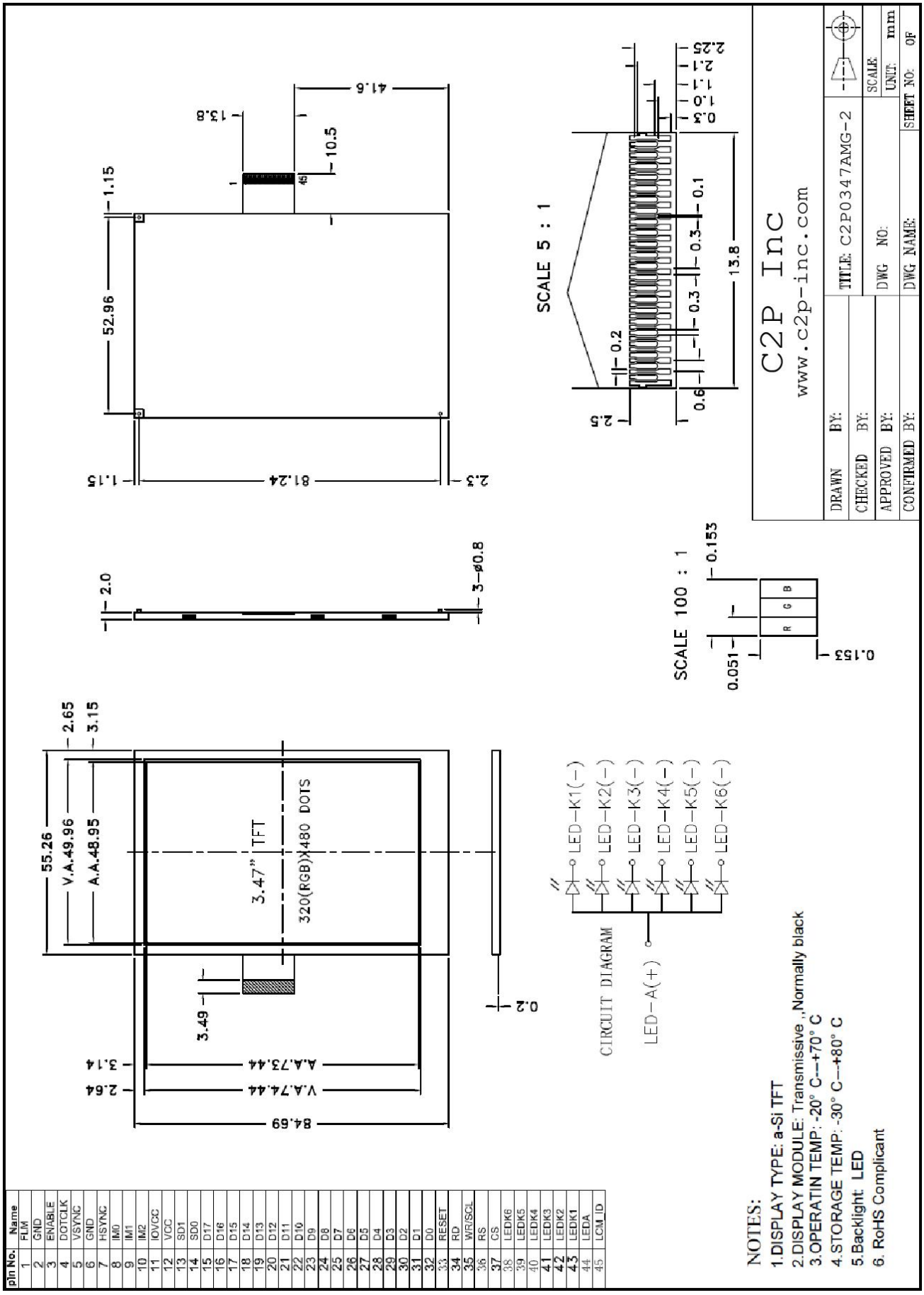
2. Application

Digital equipments which need color display, mobile phone, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	3.47	inch
Resolution	320(RGB) x 480	/
Interface	CPU/RGB	/
Technology type	a-Si TFT	/
Pixel pitch	0.153x0.153	mm
Pixel Configuration	R.G.B. Vertical Stripe	
Outline Dimension (W x H x D)	55.26X84.69X2.00	mm
Active Area	48.96X73.44	mm
Display Mode	Transmissive, Normally black	/
Viewing Direction	All angel	/
Backlight Type	LED	/
Driver IC	ILI9486	/

4. Outline Drawing



pin No.	Name
1	FLM
2	GND
3	ENABLE
4	DOTCLK
5	VSYNC
6	GND
7	HSYNC
8	IM0
9	IM1
10	IM2
11	IOVCC
12	VCC
13	SDI
14	SDO
15	D17
16	D16
17	D15
18	D14
19	D13
20	D12
21	D11
22	D10
23	D9
24	D8
25	D7
26	D6
27	D5
28	D4
29	D3
30	D2
31	D1
32	D0
33	RESET
34	RD
35	WR/SCL
36	RS
37	CS
38	LEDK6
39	LEDK5
40	LEDK4
41	LEDK3
42	LEDK2
43	LEDK1
44	LEDA
45	LCM_ID

5. Interface signals

No	Symbol	I/O	Description	Remarks
1	FLM	O	Tearing signal output. If not used, please open this pin.	
2	GND	P	Ground	
3	ENABLE	I	Data enable signal in RGB mode. If not used, please fix this pin to GND.	
4	DOTCLK	I	Pixel clock signal in RGB mode. If not used, please fix this pin to GND.	
5	VSYNC	I	Vertical sync. signal in RGB mode. If not used, please fix this pin to GND.	
6	GND	P	Ground	
7	HSYNC	I	Horizontal sync, signal in RGB mode. If not used, please fix this pin to GND.	
8	IM0	I	MPU system interface mode select	Note
9	IM1	I		
10	IM2	I		
11	IOVCC	P	Digital POWER	
12	VCC	P	Analog POWER	
13	SDI	I/O	Serial data in/out pin in DBI Type C 9bit mode Serial data input pin in DBI Type B 8bit mode. If not used, please fix this pin to GND.	
14	SDO	O	Serial data output pin. If not used, please fix this pin to GND.	
15	DB17	I/O	Data Bus	
16	DB16	I/O	Data Bus	
17	DB15	I/O	Data Bus	
18	DB14	I/O	Data Bus	
19	DB13	I/O	Data Bus	
20	DB12	I/O	Data Bus	
21	DB11	I/O	Data Bus	
22	DB10	I/O	Data Bus	
23	DB9	I/O	Data Bus	
24	DB8	I/O	Data Bus	
25	DB7	I/O	Data Bus	
26	DB6	I/O	Data Bus	
27	DB5	I/O	Data Bus	
28	DB4	I/O	Data Bus	
29	DB3	I/O	Data Bus	
30	DB2	I/O	Data Bus	
31	DB1	I/O	Data Bus	
32	DB0	I/O	Data Bus	
33	/RESET	I	Reset pin	
34	RD	I	Read strobe signal. If no used, please connect this pin to IOVCC	
35	/WR/SCL	I	(WR) Write data enable pin in DBI Type B (SCL) Write data enable pin in DBI Type C If no used, please connect this pin to IOVCC	
36	RS	I	Data/command selection pin. RS=1, select data; RS=0,select command. If not used, please connect this pin to GND.	
37	/CS	I	Chip select signal	
38	LEDK6	P	LED CATHODE	

39	LEDK5	P	LED CATHODE	
40	LEDK4	P	LED CATHODE	
41	LEDK3	P	LED CATHODE	
42	LEDK2	P	LED CATHODE	
43	LEDK1	P	LED CATHODE	
44	LEDA	P	LED ANODE	
45	LCM_ID	O	Connect to IOVCC	

The recommended connector: FH26-45S-0.3SHW.

Note: Select the MPU system interface mode

IM2	IM1	IM0	MPU Interface Mode	DB Pin in use	
				Register/Content	GRAM
0	0	0	DBI Type B 18-bit	DB[17:0]	DB[7:0]
0	0	1	DBI Type B 9-bit	DB[8:0]	DB[7:0]
0	1	0	DBI Type B 16-bit	DB[15:0]	DB[7:0]
0	1	1	DBI Type B 8-bit	DB[7:0]	DB[7:0]
1	0	1	DBI Type C 3-wire 9-bit	--	--
1	1	1	DBI Type C 4-wire 8-bit	--	--

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	IOVCC	-0.3	4.6	V	
Analog Supply Voltage	VCC	-0.3	4.6	V	
Input Voltage	/CS,/RD,/WR/SCL,RS, ENABLE,VSYNC,HSYNC, DOTCLK,SDO,SDI,/RESET,IM0 , IM1,IM2,DB[0~17]	-0.3	IOVCC +0.3	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

6.3. LED Backlight Absolute max. ratings

Item	Symbol	MIN	MAX	Unit	Remark
LED Forward Current	ILED	--	25	mA	For each LED

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage	IOVCC	1.65	2.8	3.3	V	
Analog Supply Voltage	VCC	2.5	2.8	3.3	V	
Input Signal Voltage	V_{IL}	--	--	0.3xIOVCC	V	Note
	V_{IH}	0.7xIOVCC	--	IOVCC	V	
Output Signal Voltage	V_{OL}	--	--	0.2xIOVCC	V	SD0
	V_{OH}	0.8xIOVCC	--	--	V	

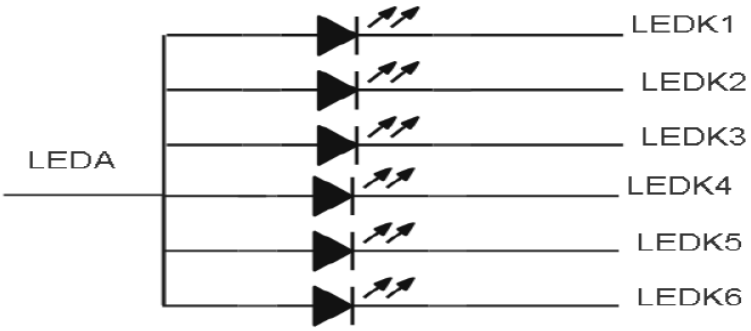
Note:
/CS,/RD,/WR/SCL,RS,ENABLE,VSYNC,HSYNC,DOTCLK,SDO,SDI,/RESET,IM0,IM1,IM2,DB[0~17]

7.2 LED Backlight

Ta=25℃

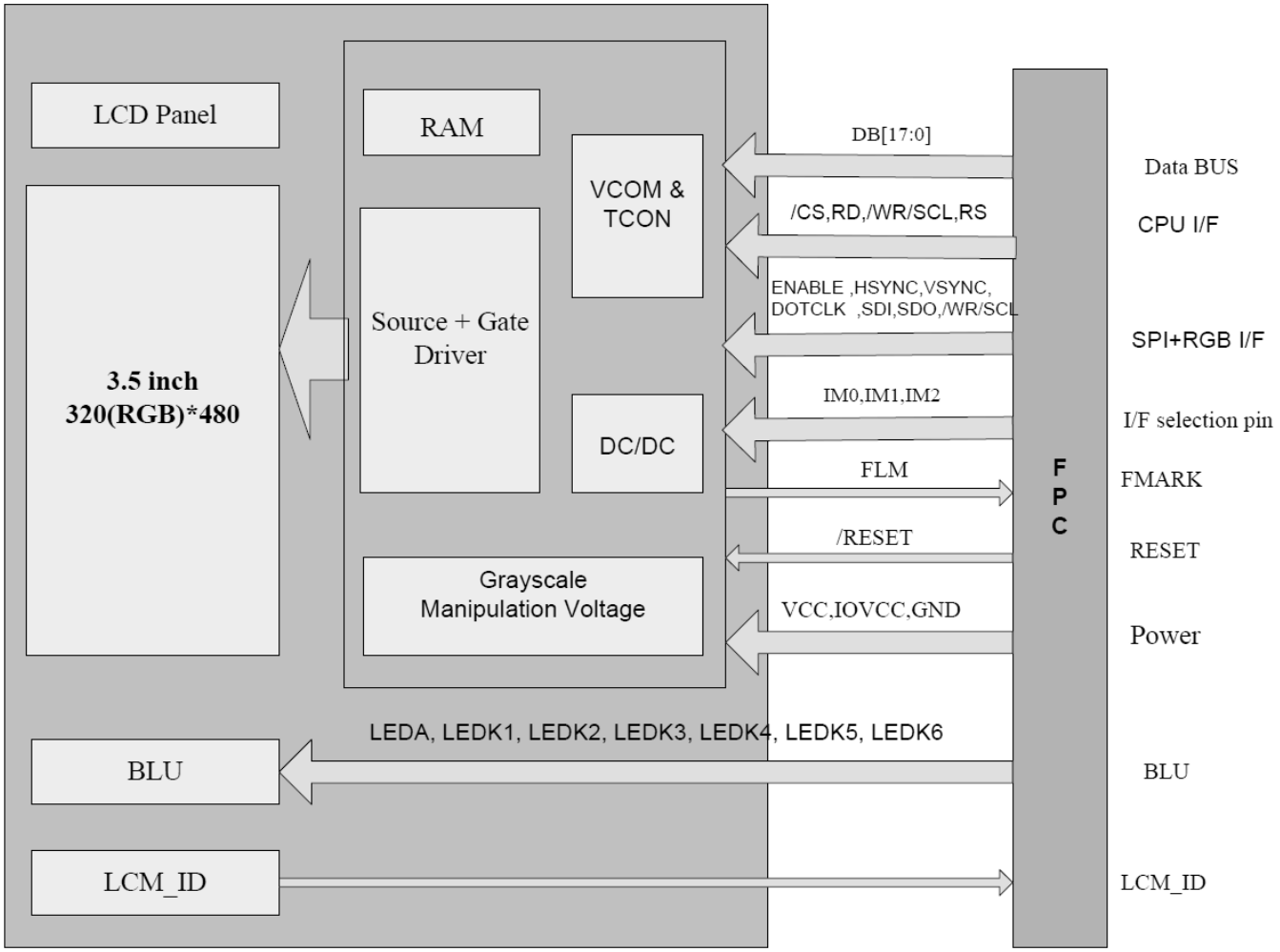
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	--	20	--	mA	For One LED
Forward Voltage	VF	--	3.2	--	V	
Power Consumption	WBL	--	384	--	mW	For 6 LEDs

Note 1: The connection of Backlight LED:



Note 2: One LED: If=20mA, Vf=3.2V.

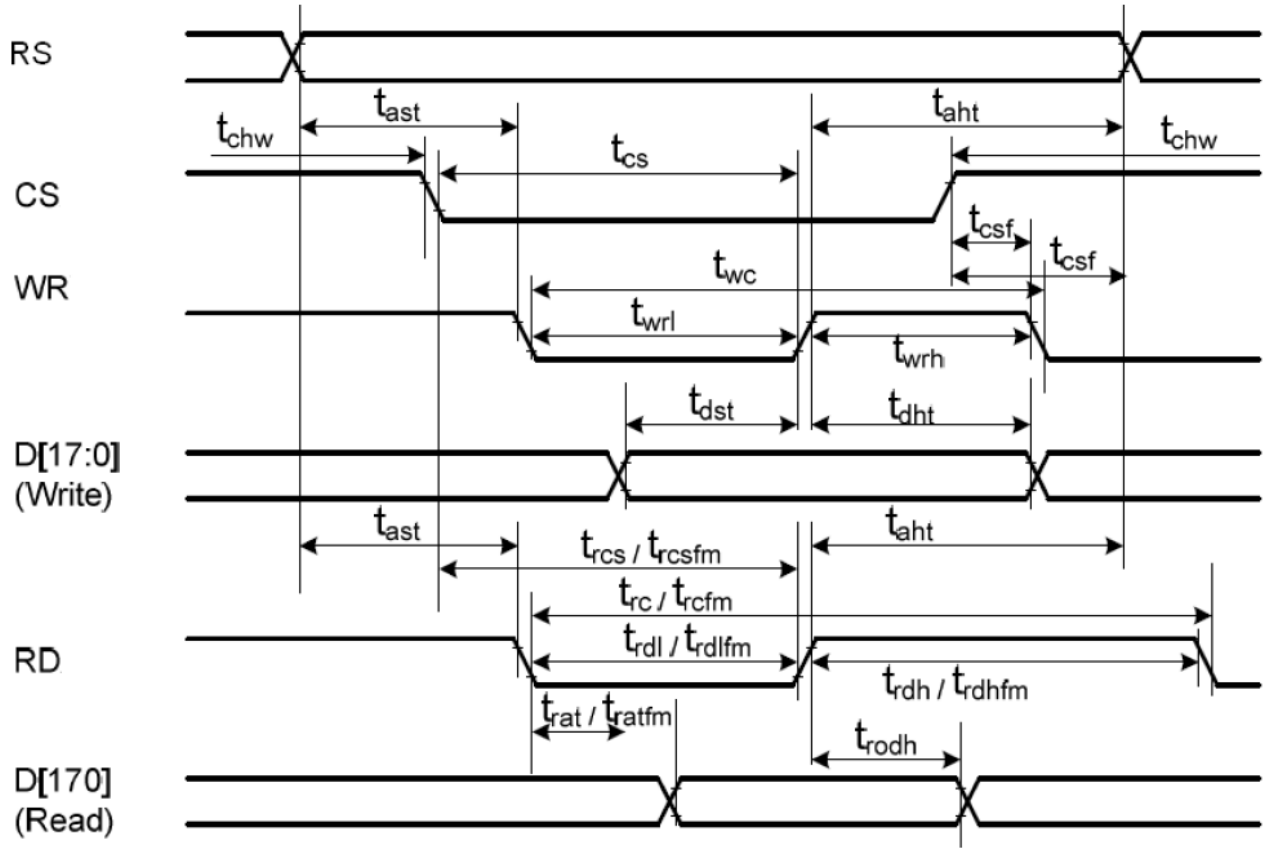
7.3 Schematic of LCD module system



8. Command/AC Timing

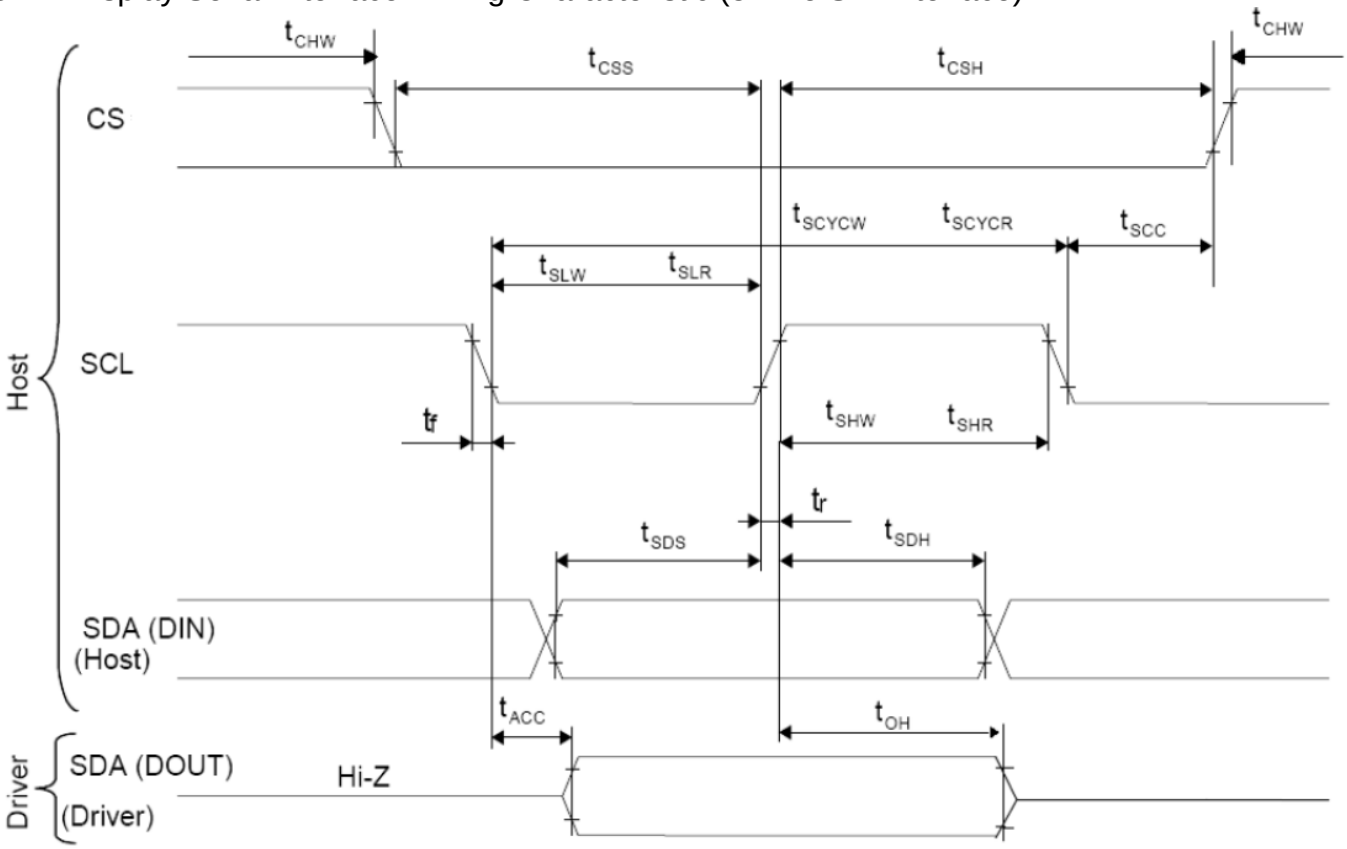
8.1 Timing Parameter DBI Type B

8.1.1 Display Parallel 18/16/9/8bit Interface Timing Characteristic (8080-series)



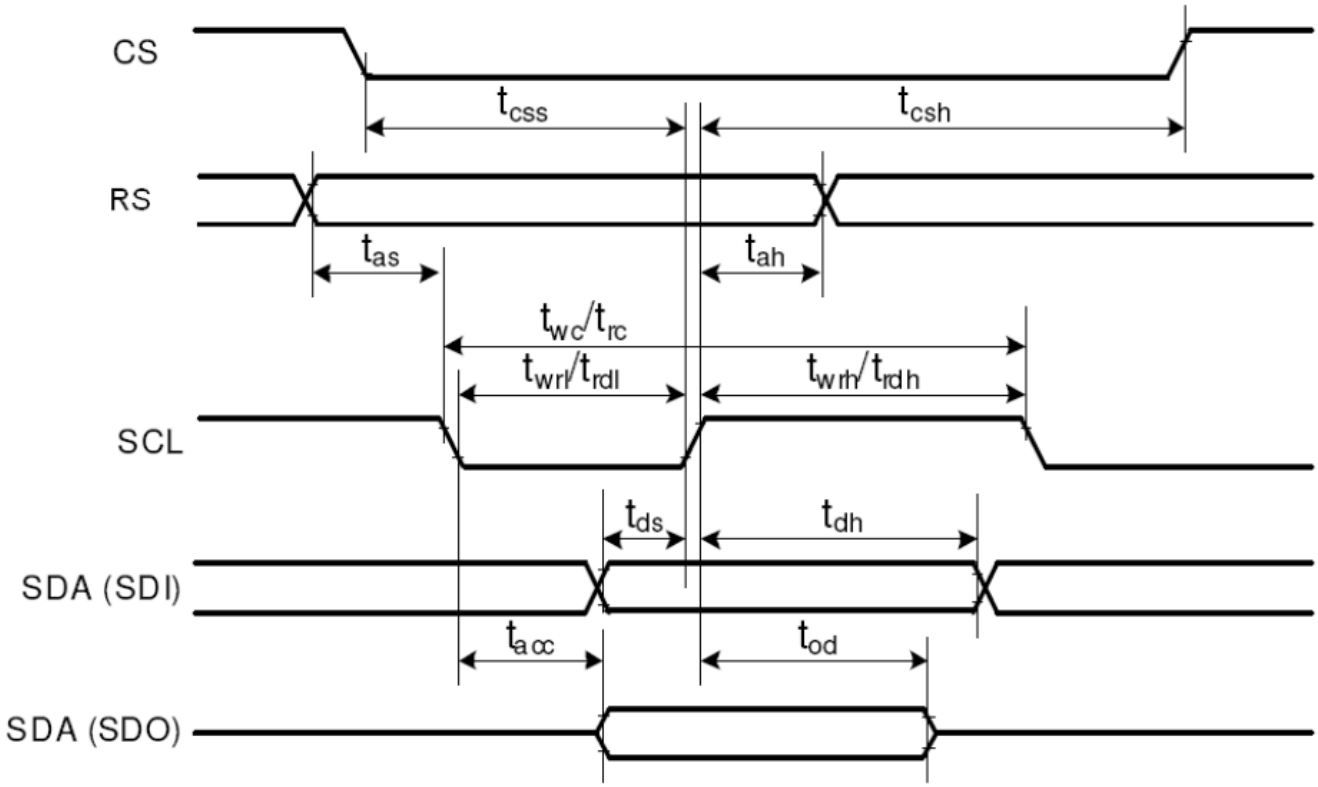
Signal	Symbol	Parameter	min	max	Unit	Description
RS	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	0	-	ns	-
CS	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WR	twc	Write cycle	66	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RD(FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RD(ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0], DB[15:0], DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

8.1.2 Display Serial Interface Timing Characteristic (3-Line SPI Interface)



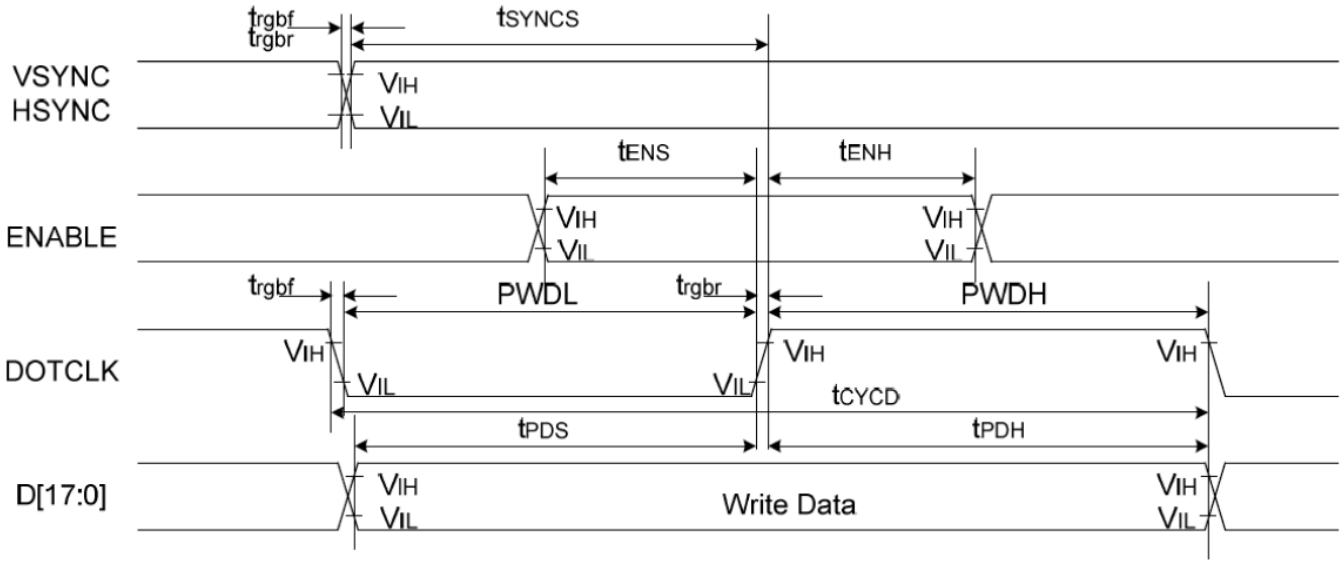
Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	66	-	ns	
	tshw	SCL "H" Pulse Width (Write)	15	-	ns	
	tslw	SCL "L" Pulse Width (Write)	15	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	10	-	ns	
	tsdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	
	toh	Output disable time (Read)	15	50	ns	
CS	tscc	SCL-CSX	15	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

8.1.3 Display Serial Interface Timing Characteristic (4-Line SPI Interface)



Signal	Symbol	Parameter	min	max	Unit	Description
CS	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	60	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL “H” pulse width (Write)	15	-	ns	
	twrl	SCL “L” pulse width (Write)	15	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
RS	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write / Read)	10	-	ns	
SDA / SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

8.1.4 Parallel 18/16bit RGB Interface Timing Characteristic

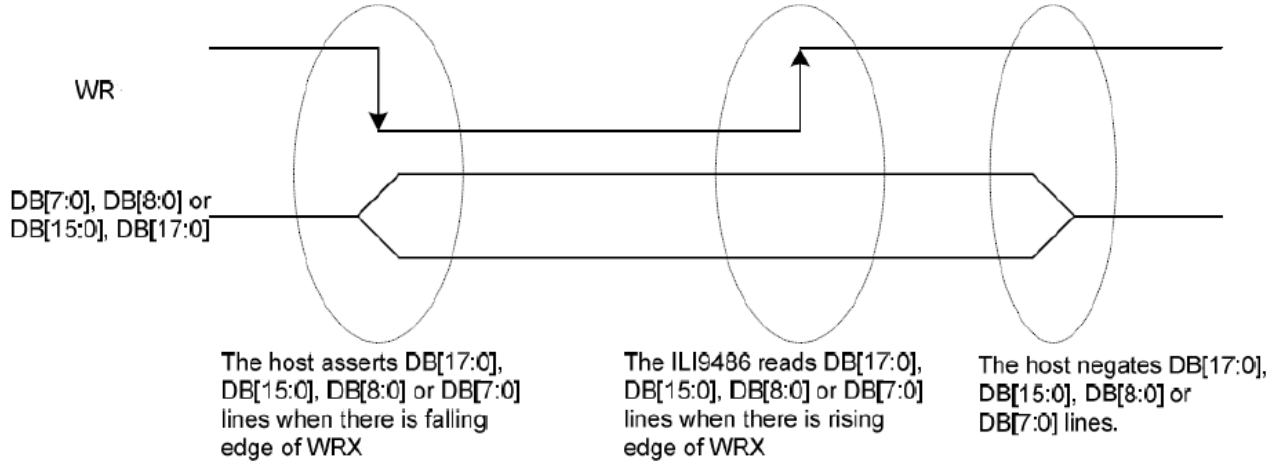


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	66	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

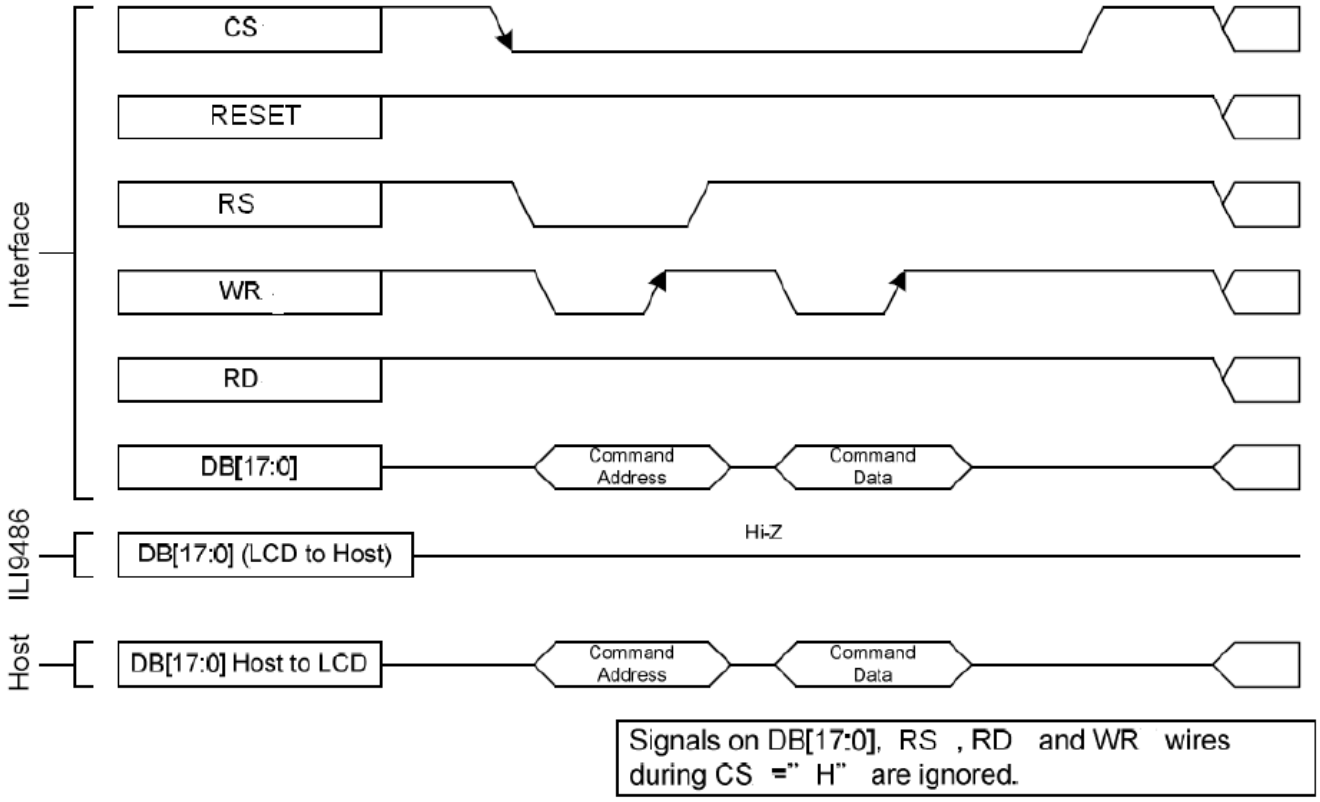
Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.3V, AGND=DGND=0V

8.2 Register write/read timing (DBI type C)

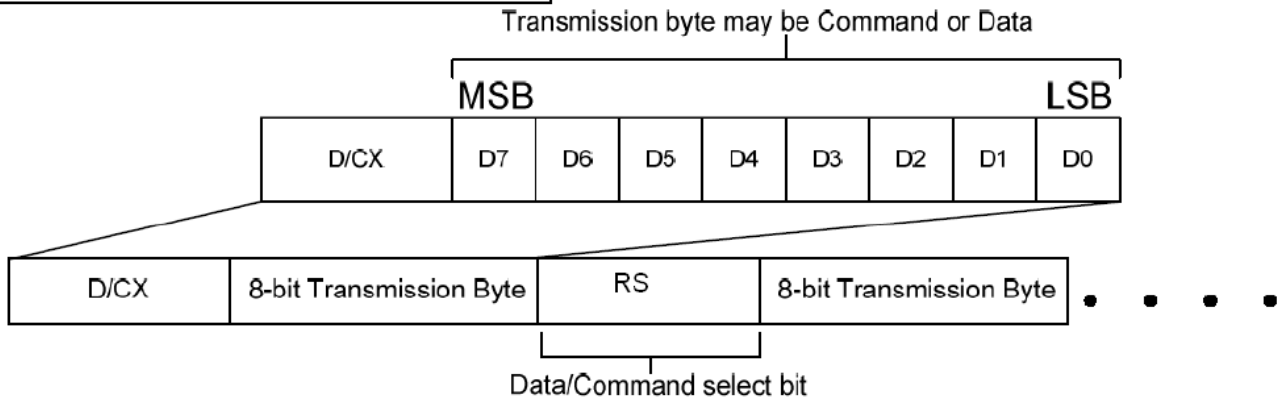
8.2.1 Write to register



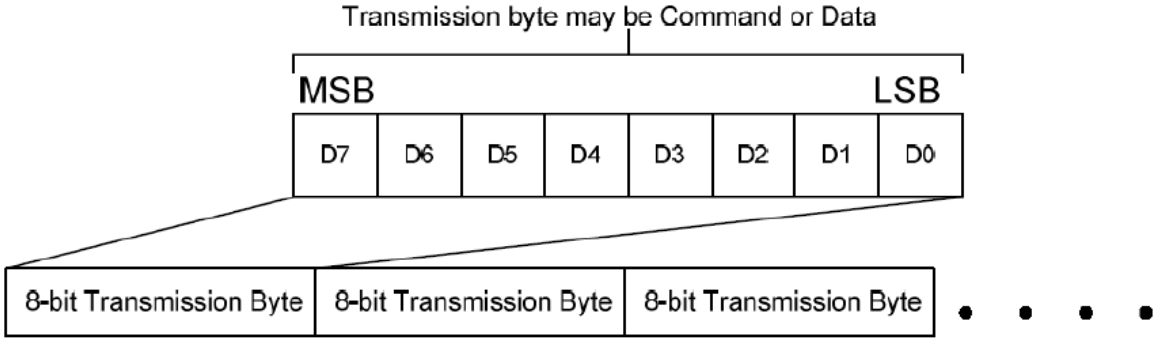
Note: WR is an unsynchronized signal (It can be stopped)



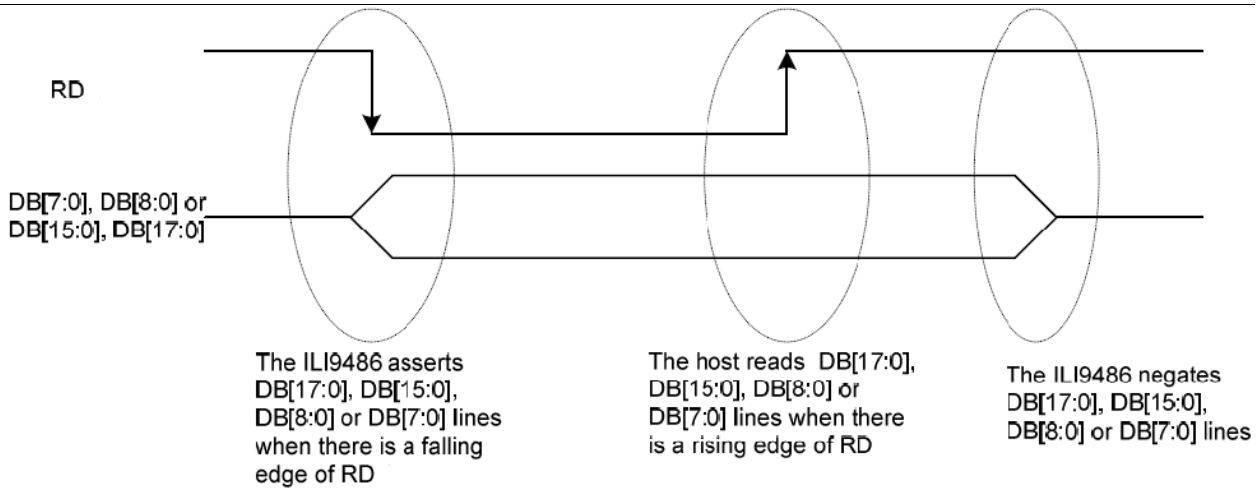
Data Format for 3-line Serial Interface



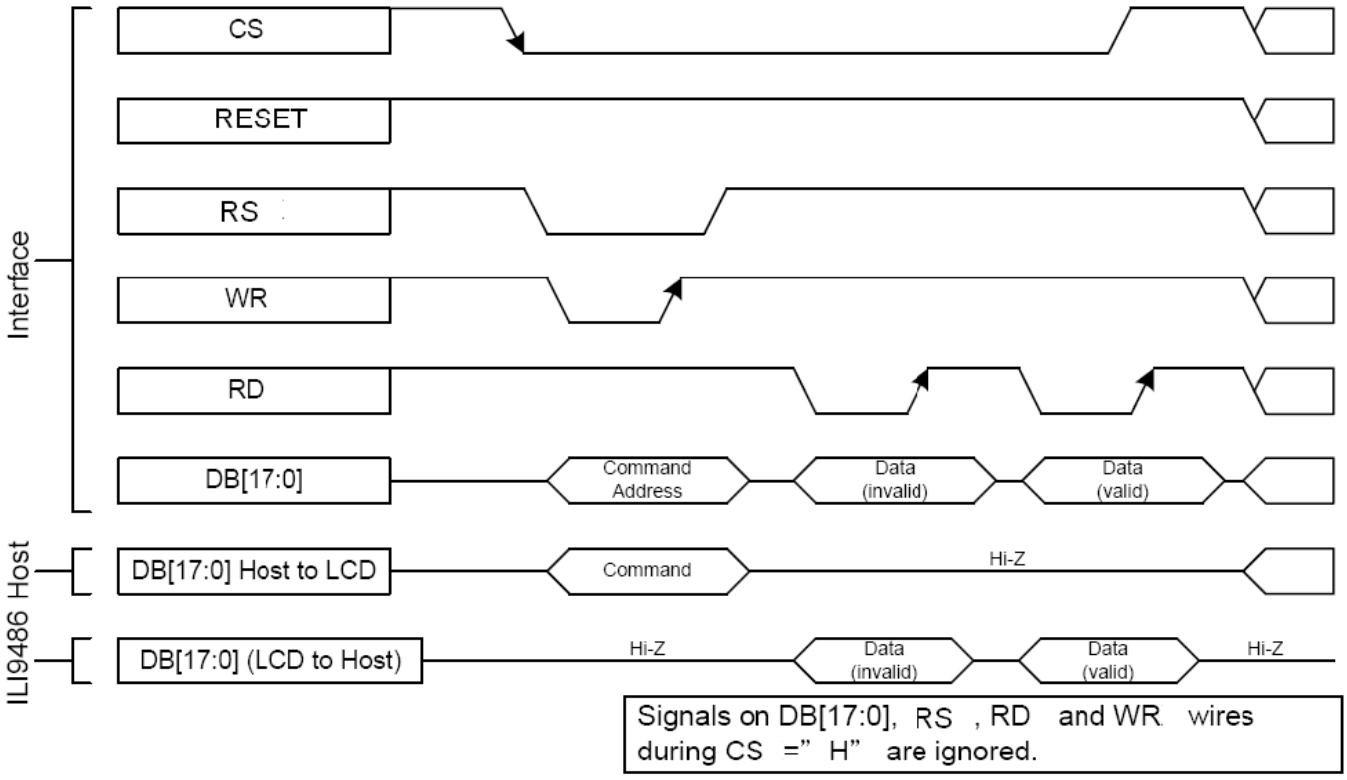
Data Format for 4-line Serial Interface



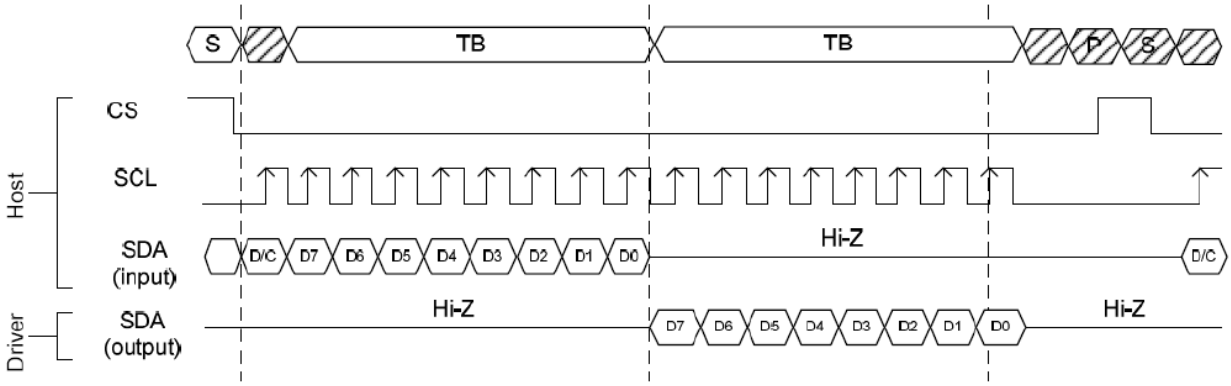
8.2.2 Read from register



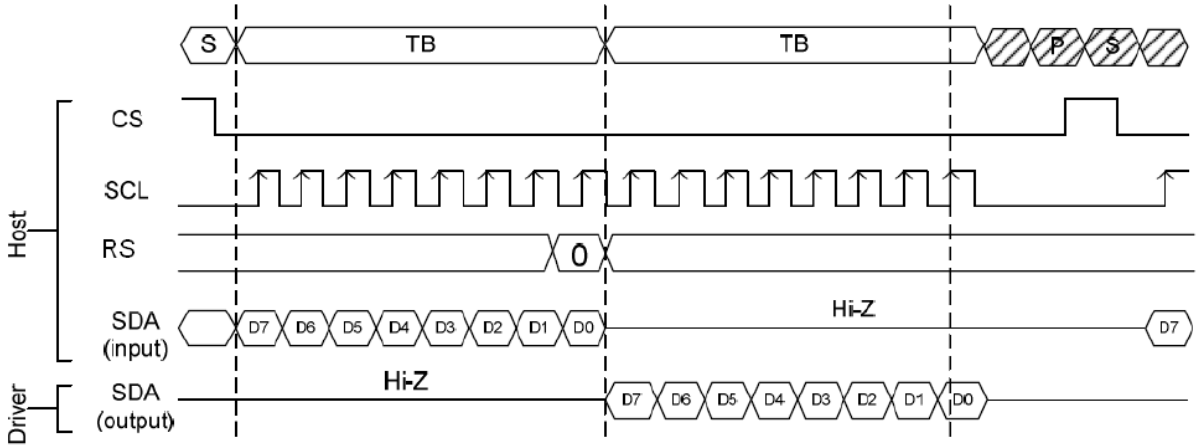
Note: RD is an unsynchronized signal (It can be stopped).



3-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)

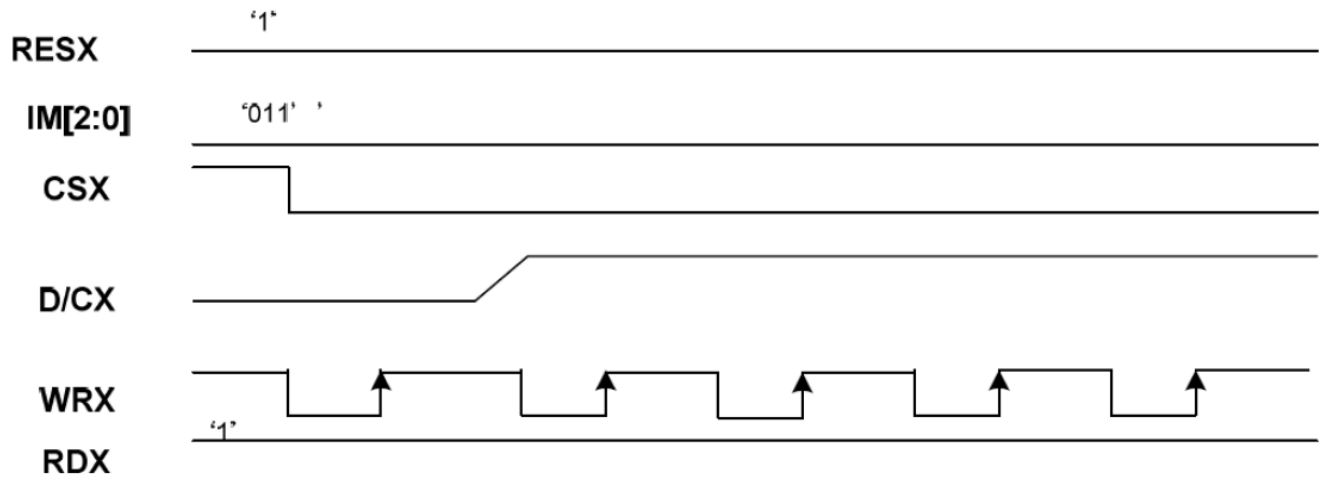


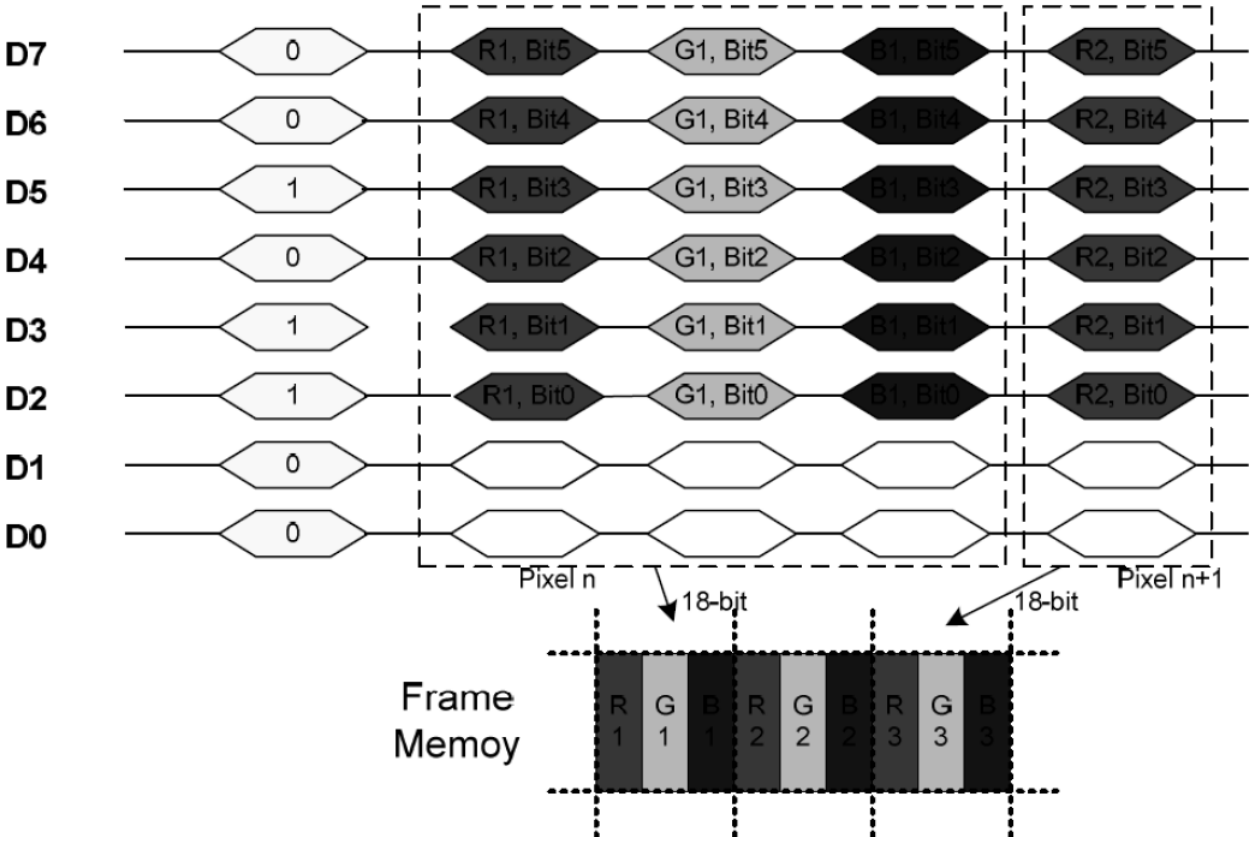
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



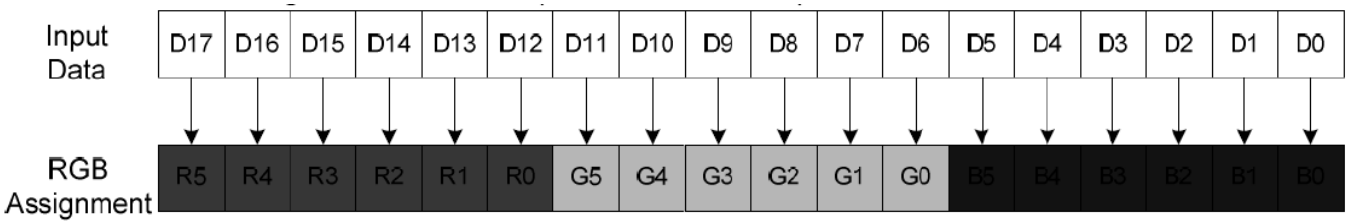
8.3 DPI Data Format

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors

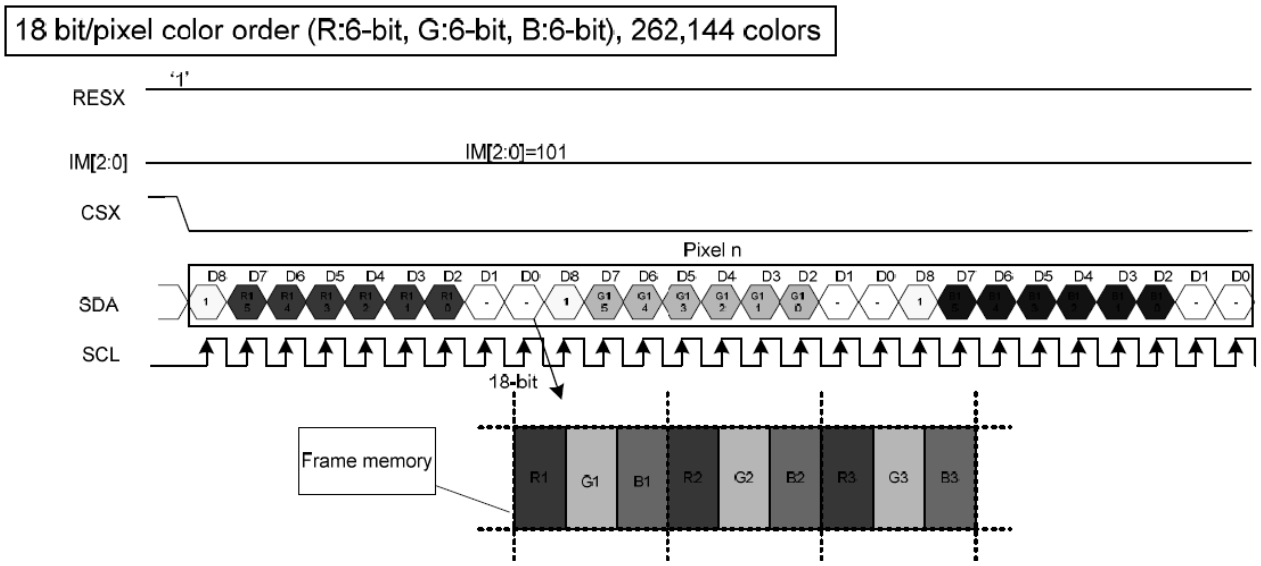




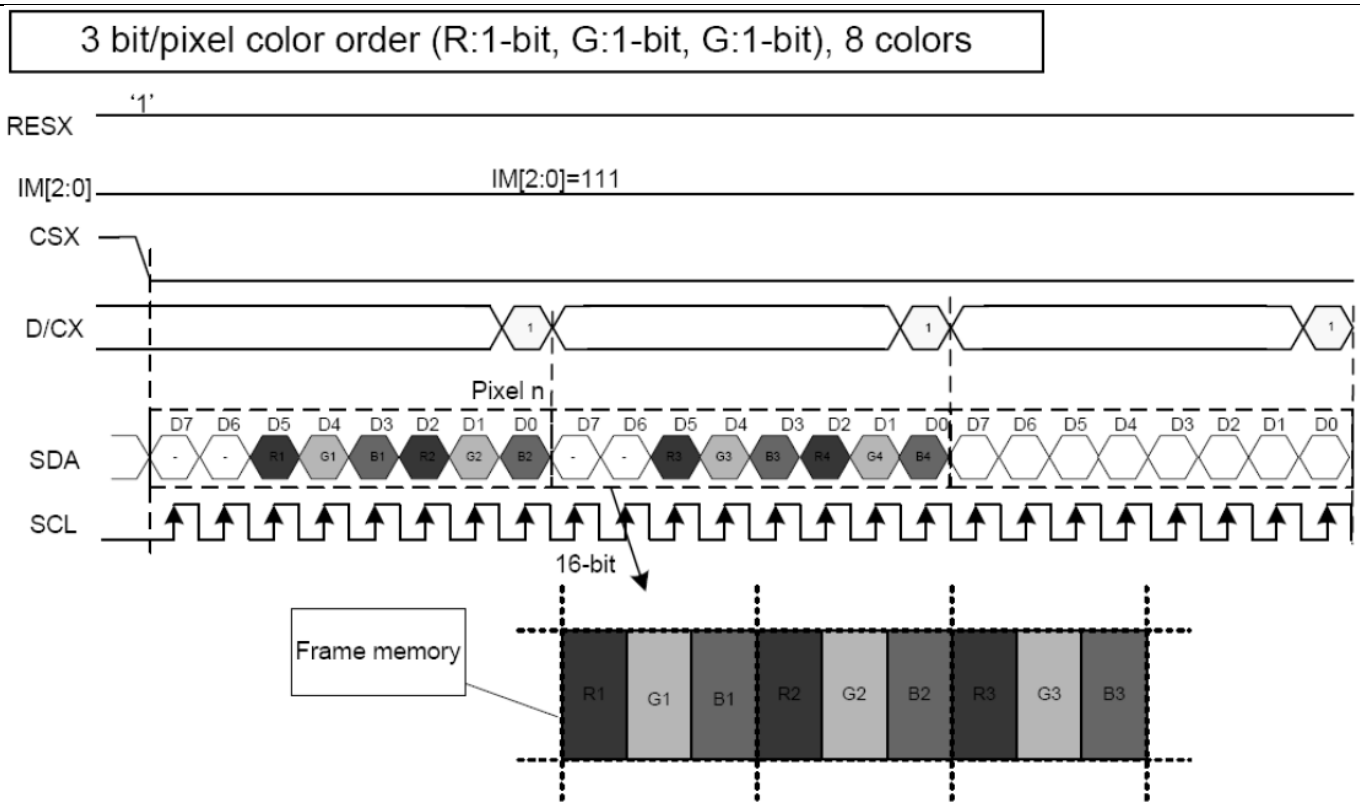
CPU 8bit (R: 6bit, G: 6bit, B: 8bit) Data format



RGB 18bit Data format

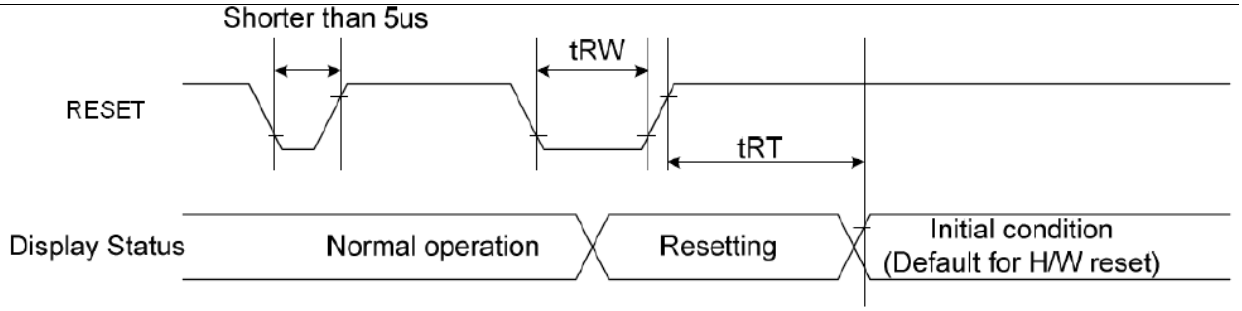


3-SPI Data format



4-SPI Data Format

8.4 Reset Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit
RESET	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

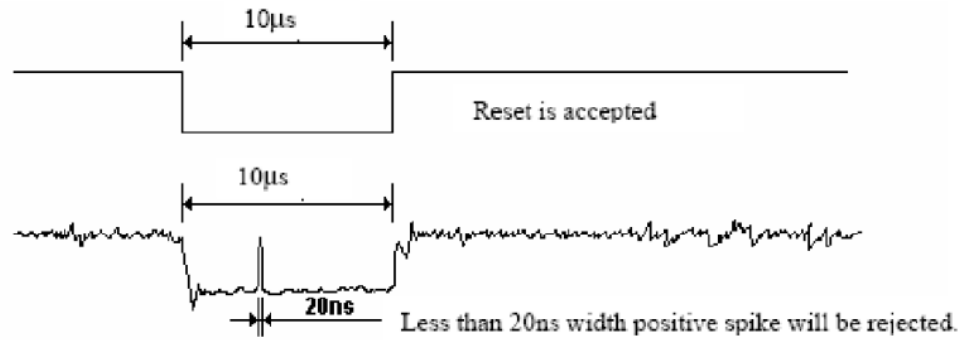
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESET

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



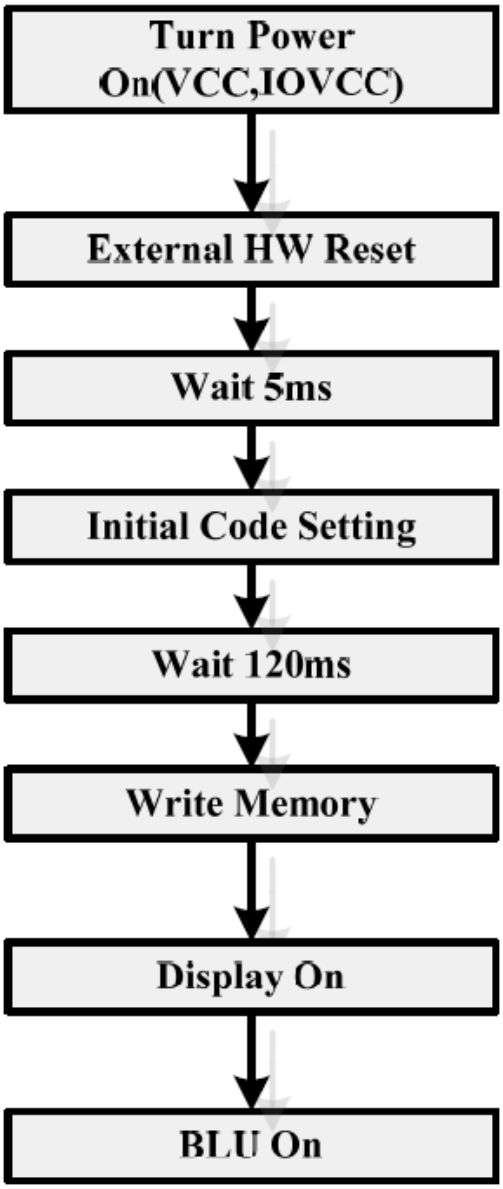
Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

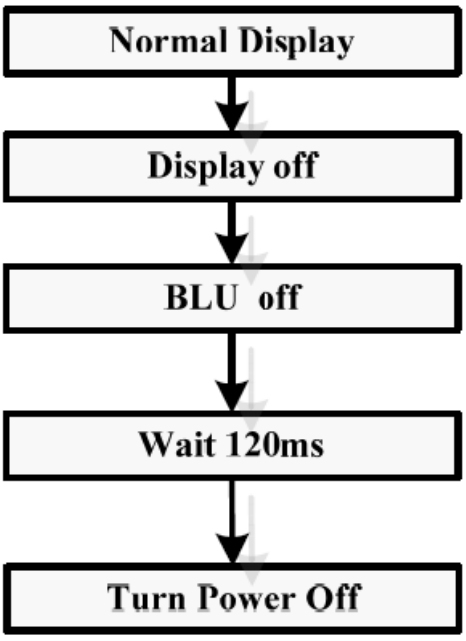
Note7: It is necessary to wait 5msec after releasing RESET *before sending commands. Also Sleep Out command cannot be sent for 120msec.*

8.5 Power ON/Off Sequence

Power on Sequence



Power off Sequence



9. Optical Specification

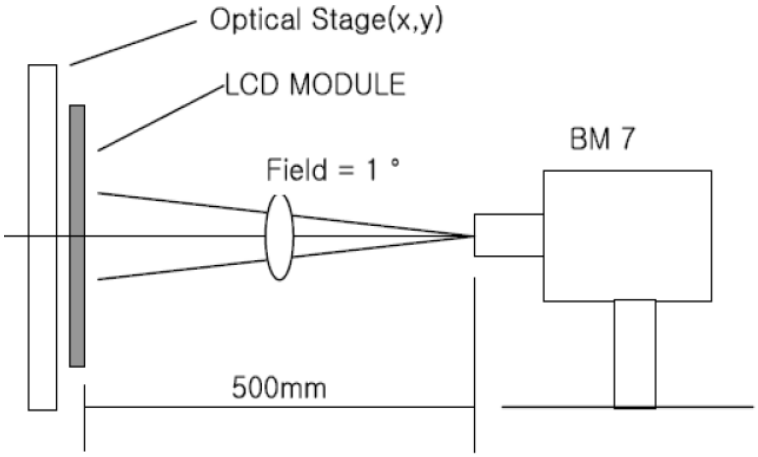
Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	600	800	--	--	Note1 Note2
Response Time		Tr + Tf	25℃	--	35	45	ms	Note1 Note3
View Angles		ΘT	CR≧10	70	80	--	Degree	Note 4
		ΘB		70	80	--		
		ΘL		70	80	--		
		ΘR		70	80	--		
Chromaticity	White	x	Brightness is on	0.265	0.315	0.365	--	Note5, Note1
		y		0.293	0.343	0.393		
NTSC		S	--	55	60	--	%	Note5
Luminance		L	--	280	350	--	cd/m^2	Note1 Note6
Uniformity		U	--	75	80	--	%	Note1 Note7

Note 1: Definition of optical measurement system.

Temperature = 25°C(±3°C)

LED back-light: ON, Environment brightness < 150 lx

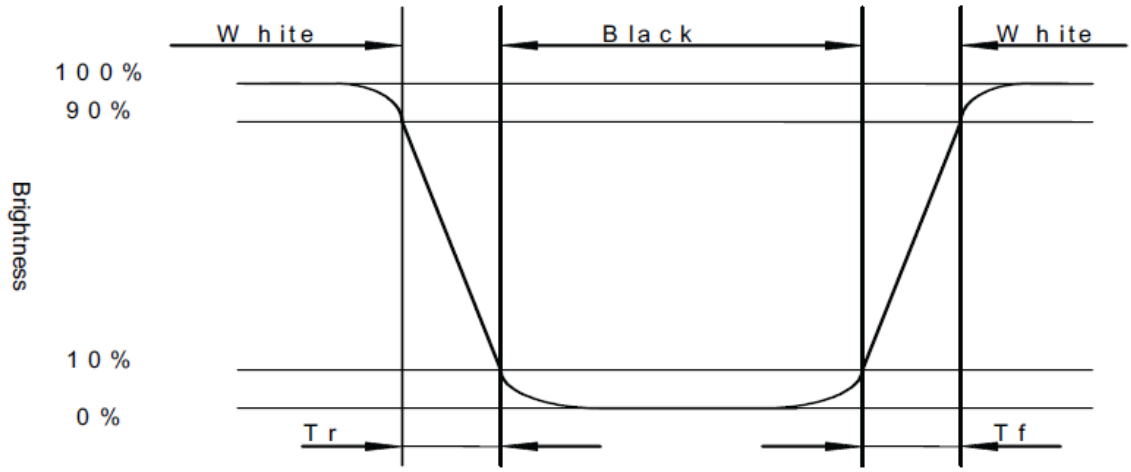


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

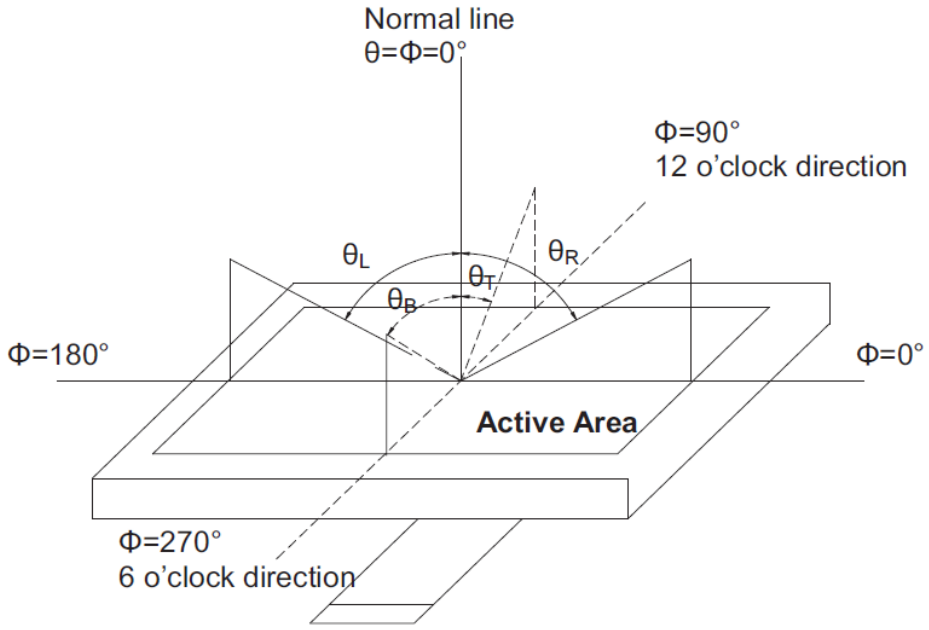
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black (Decay Time, Tf).



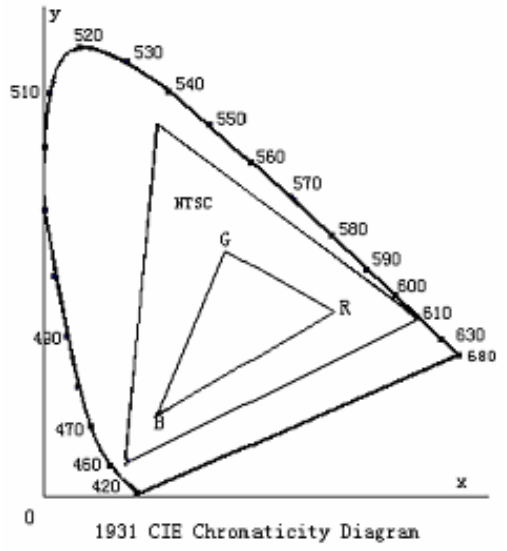
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity(U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

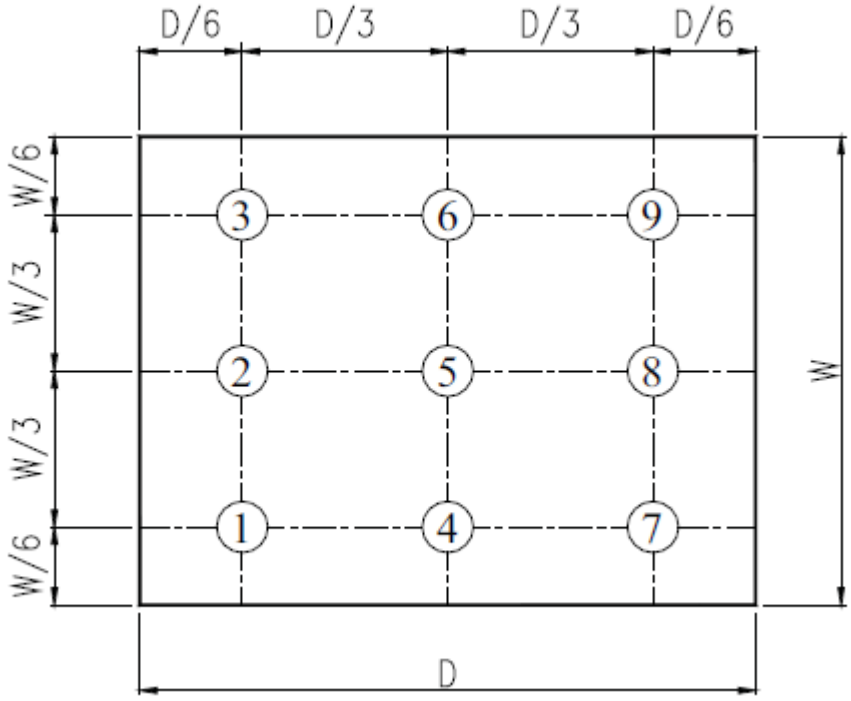


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 240hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 240hrs	Per table in below
3	High Temp Storage	Ta=+80℃, 240hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 240hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60℃, 90% RH 240 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+80℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.