# C3M0021120J2

## Silicon Carbide Power MOSFET
## N-Channel Enhancement Mode

### Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- Larger drain tab for better thermal performance
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ($Q_{rr}$)
- Halogen free, RoHS compliant

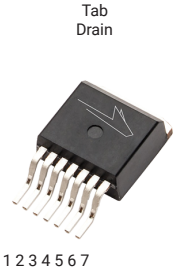
### Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

### Applications

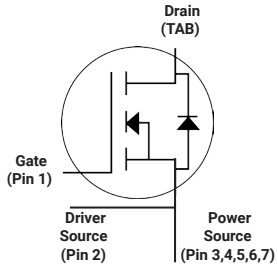
- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

### Package




Halogen-Free

RoHS compliant




| Part Number | Package | Marking |
|---|---|---|
| C3M0021120J2 | TO-263-7XL | C3M0021120J2 |

### Key Parameters

| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions | Note |
|---|---|---|---|---|---|---|---|
| Drain - Source Voltage | $V_{DS}$ | | | 1200 | v | $T_C$ = 25°C | |
| Maximum Gate - Source Voltage | $V_{GS(max)}$ | -8 | | +19 | | Transient | |
| Operational Gate-Source Voltage | $V_{GS\ op}$ | | -4/15 | | | Static | Note 1 |
| DC Continuous Drain Current | $I_D$ | | | 114 | A | $V_{GS}$ = 15 V, $T_C$ = 25 °C, $T_J$ ≤175 °C | Fig. 19 Note 2 |
| | | | | 83 | | $V_{GS}$ = 15 V, $T_C$ = 100 °C, $T_J$ ≤175 °C | |
| Pulsed Drain Current | $I_{DM}$ | | | 248 | | $t_{Pmax}$ limited by $T_{jmax}$ $V_{GS}$ = 15V, $T_C$ = 25 °C | Fig. 22 |
| Power Dissipation | $P_D$ | | | 500 | W | $T_C$ = 25 °C, $T_J$ = 175 °C | Fig. 20 |
| Operating Junction and Storage Temperature | $T_J$, $T_{stg}$ | | | -40 to +175 | °C | | |
| Solder Temperature | $T_L$ | | | 260 | | According to JEDEC J-STD-020 | |

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design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## Electrical Characteristics ($T_C$ = 25˚C unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 1200 | | | V | $V_{GS}$ = 0 V, $I_D$ = 100 µA | |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.8 | 2.9 | 3.8 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 17.10 mA | Fig. 11 |
| | | | 2.3 | | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 17.10 mA, $T_J$ = 175ºC | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | 1 | 50 | µA | $V_{DS}$ = 1200 V, $V_{GS}$ = 0 V | |
| $I_{GSS}$ | Gate-Source Leakage Current | | 10 | 250 | nA | $V_{GS}$ = 15 V, $V_{DS}$ = 0 V | |
| $R_{DS(on)}$ | Drain-Source On-State Resistance | | 21 | 29 | mΩ | $V_{GS}$ = 15 V, $I_D$ = 62.12 A | Fig. 4, 5, 6 |
| | | | 35 | | | $V_{GS}$ = 15 V, $I_D$ = 62.12 A, $T_J$ = 175ºC | |
| $g_{fs}$ | Transconductance | | 38 | | S | $V_{DS}$= 20 V, $I_{DS}$= 62.12 A | Fig. 7 |
| | | | 35 | | | $V_{DS}$= 20 V, $I_{DS}$= 62.12 A, $T_J$ = 175ºC | |
| $C_{iss}$ | Input Capacitance | | 5100 | | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 0V to 1000 V<br>f = 100 kHz<br>$V_{AC}$ = 25 mV | Fig. 17, 18 |
| $C_{oss}$ | Output Capacitance | | 174 | | | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | 11 | | | | |
| $E_{oss}$ | $C_{oss}$ Stored Energy | | 98 | | µJ | $V_{DS}$= 1000 V, f = 100 kHz | Fig. 16 |
| $C_{o(er)}$ | Effective Output Capacitance (Energy Related) | | 210 | | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 800V | Note: 3 |
| $C_{o(tr)}$ | Effective Output Capacitance (Time Related) | | 323 | | pF | | |
| $E_{ON}$ | Turn-On Switching Energy (Body Diode FWD) | | 1.7 | | mJ | $V_{DS}$= 800 V, $V_{GS}$= -4 V/15 V, $I_D$= 62.12 A, $R_{G(ext)}$ = 2.5 Ω, L= 59 µH, $T_J$ = 175ºC<br>FWD = Internal Body Diode | Fig. 26, 28 |
| $E_{OFF}$ | Turn-Off Switching Energy (Body Diode FWD) | | 0.3 | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | | 15 | | ns | $V_{DD}$ = 800 V, $V_{GS}$ = -4 V/15 V, $I_D$ = 62.12 A, $R_{G(ext)}$ = 2.5 Ω, L= 59 µH, $T_J$ = 25ºC<br>Timing relative to $V_{DS}$<br>Inductive load | Fig. 27, 28 |
| $t_r$ | Rise Time | | 34 | | | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | 54 | | | | |
| $t_f$ | Fall Time | | 13 | | | | |
| $R_{G(int)}$ | Internal Gate Resistance | | 2.9 | | Ω | f = 1 MHz, $V_{AC}$ = 25 mV | |
| $Q_{gs}$ | Gate to Source Charge | | 60 | | nC | $V_{DS}$ = 800 V, $V_{GS}$ = -4 V/15 V<br>$I_D$ = 62.12 A<br>Per IEC60747-8-4 pg 21 | Fig. 12 |
| $Q_{gd}$ | Gate to Drain Charge | | 45 | | | | |
| $Q_g$ | Total Gate Charge | | 169 | | | | |

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 800V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 800V

## Reverse Diode Characteristics ($T_C$ = 25˚C unless otherwise specified)

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Diode Forward Voltage | 4.9 | | V | $V_{GS}$ = -4 V, $I_{SD}$ = 31.1 A, $T_J$ = 25 °C | Fig. 8, 9, 10 |
| | | 4.4 | | V | $V_{GS}$ = -4 V, $I_{SD}$ = 31.1 A, $T_J$ = 175 °C | |
| $I_S$ | Continuous Diode Forward Current | | 85 | A | $V_{GS}$ = -4 V, $T_C$ = 25˚C | |
| $I_{SM}$ | Diode pulse Current | | 248 | A | $V_{GS}$ = -4 V, pulse width $t_P$ limited by $T_{jmax}$ | |
| $t_{rr}$ | Reverse Recover time | 16 | | ns | $V_{GS}$ = -4 V, $I_{SD}$ = 62.12 A, $V_R$ = 800 V<br>$di_F/dt$ = 5300 A/µs, $T_J$ = 25 °C | |
| $Q_{rr}$ | Reverse Recovery Charge | 416 | | nC | | |
| $I_{rrm}$ | Peak Reverse Recovery Current | 44 | | A | | |
| $t_{rr}$ | Reverse Recover time | 22 | | ns | $V_{GS}$ = -4 V, $I_{SD}$ = 62.12 A, $V_R$ = 800 V<br>$di_F/dt$ = 2240 A/µs, $T_J$ = 25 °C | |
| $Q_{rr}$ | Reverse Recovery Charge | 268 | | nC | | |
| $I_{rrm}$ | Peak Reverse Recovery Current | 21 | | A | | |

## Thermal Characteristics

| Symbol | Parameter | Typ. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance from Junction to Case | 0.23 | °C/W | | Fig. 21 |

## Typical Performance

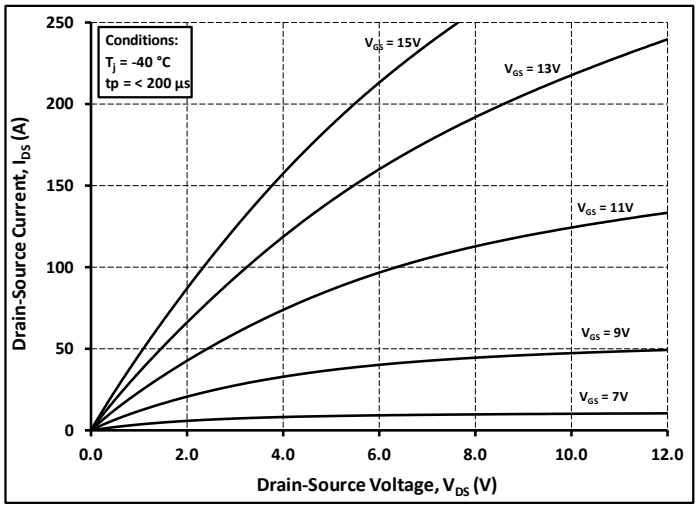



Figure 1. Output Characteristics $T_J$ = -40 ºC

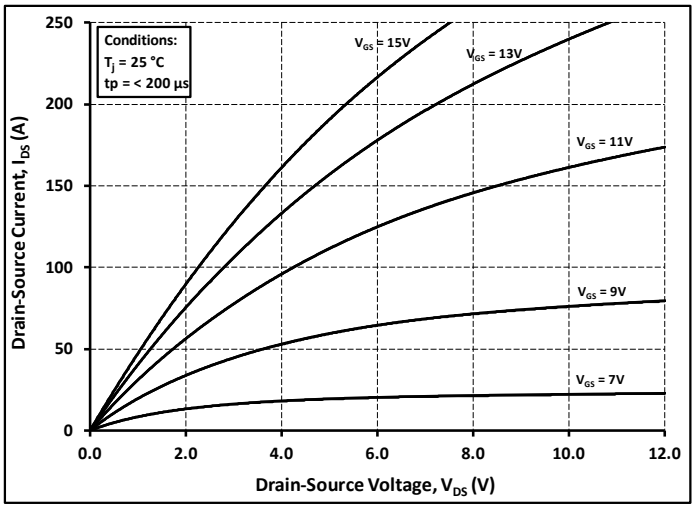



Figure 2. Output Characteristics $T_J$ = 25 ºC

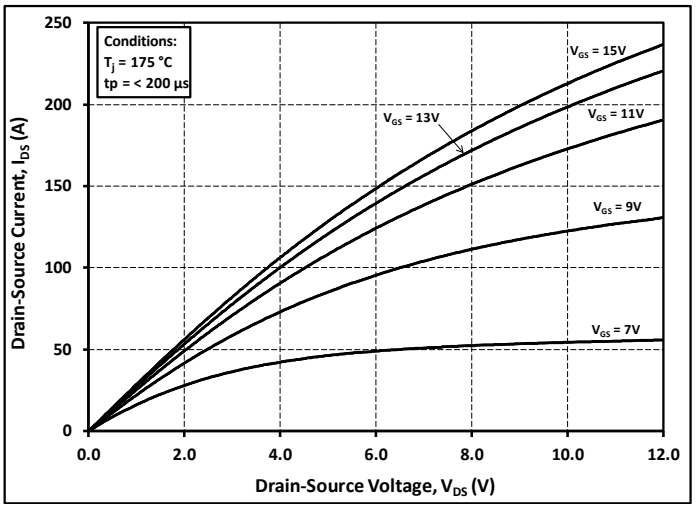



Figure 3. Output Characteristics $T_J$ = 175 ºC

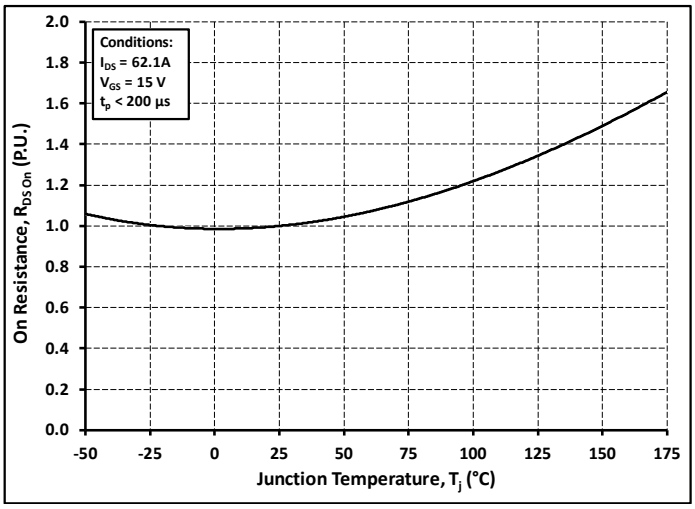



Figure 4. Normalized On-Resistance vs. Temperature

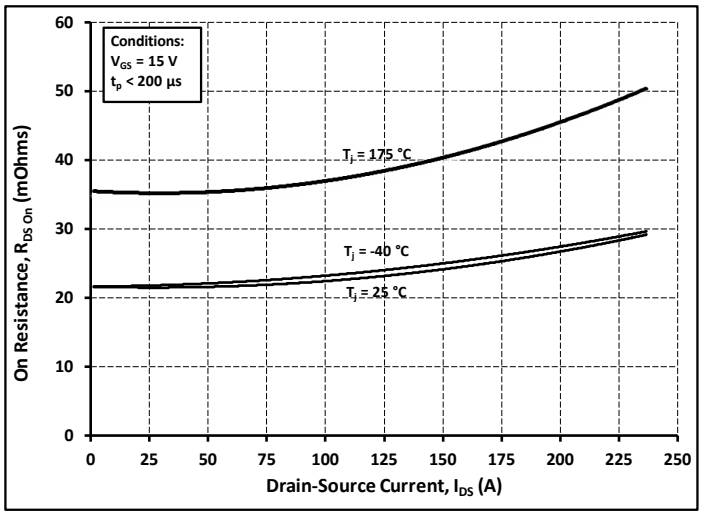



Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

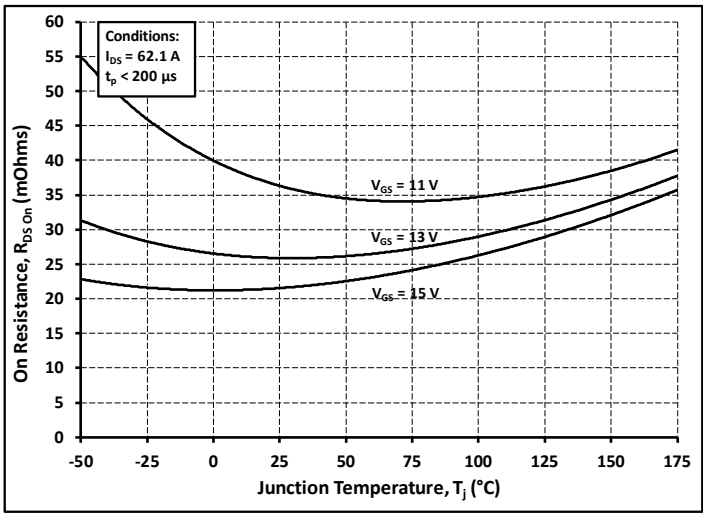



Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

## Typical Performance

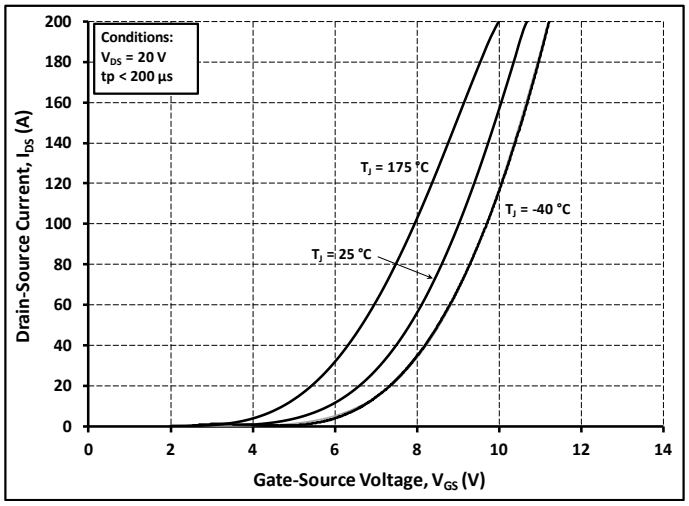



Figure 7. Transfer Characteristic for Various Junction Temperatures

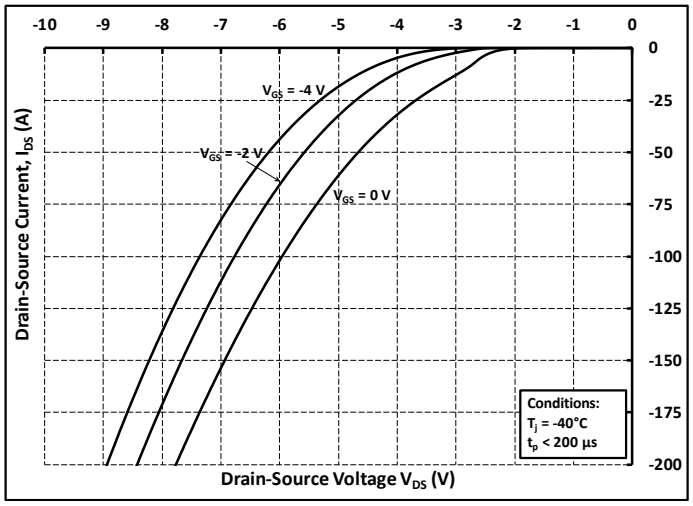



Figure 8. Body Diode Characteristic at -40 ºC

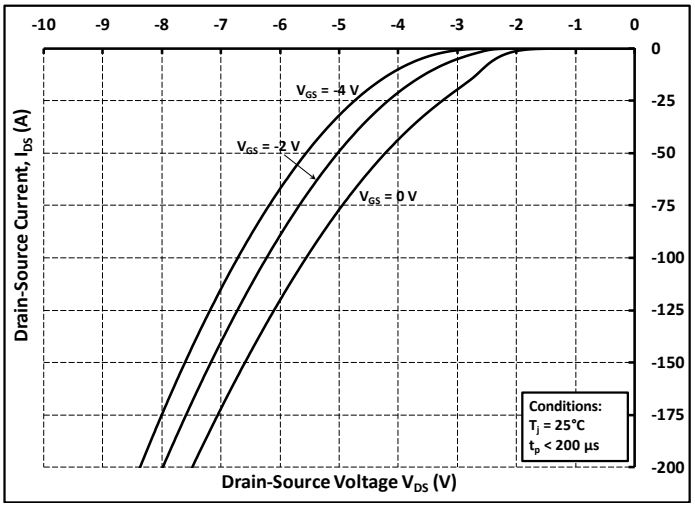



Figure 9. Body Diode Characteristic at 25 ºC

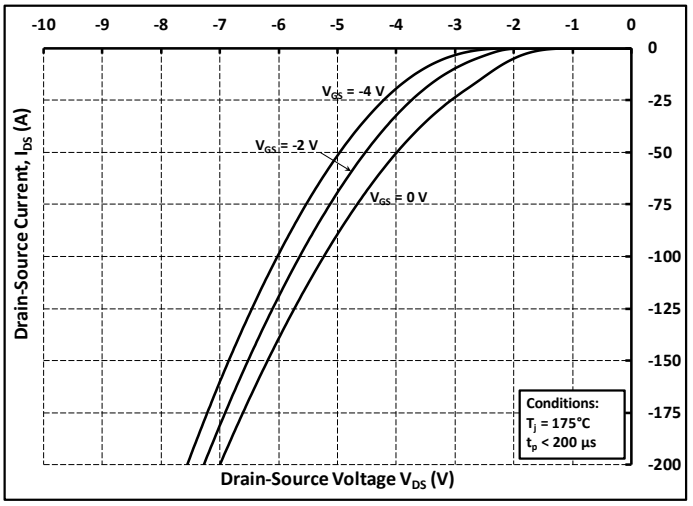



Figure 10. Body Diode Characteristic at 175 ºC

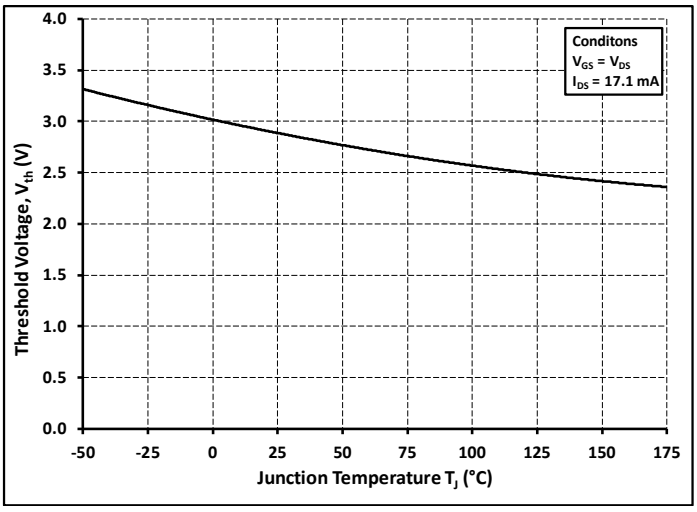



Figure 11. Threshold Voltage vs. Temperature

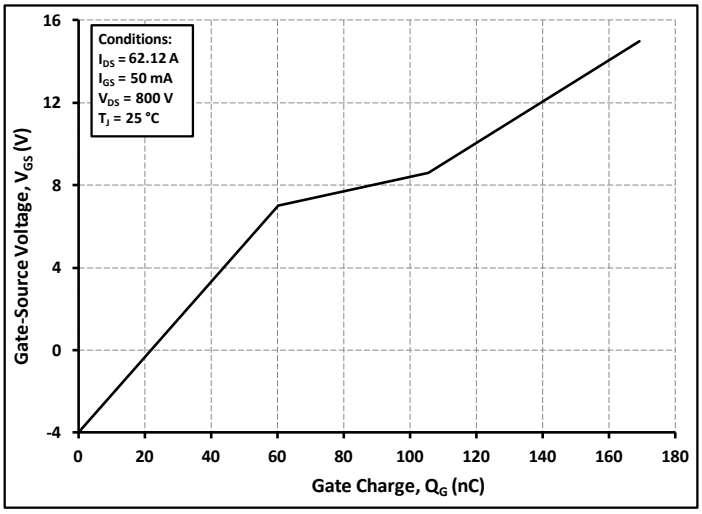



Figure 12. Gate Charge Characteristics

## Typical Performance

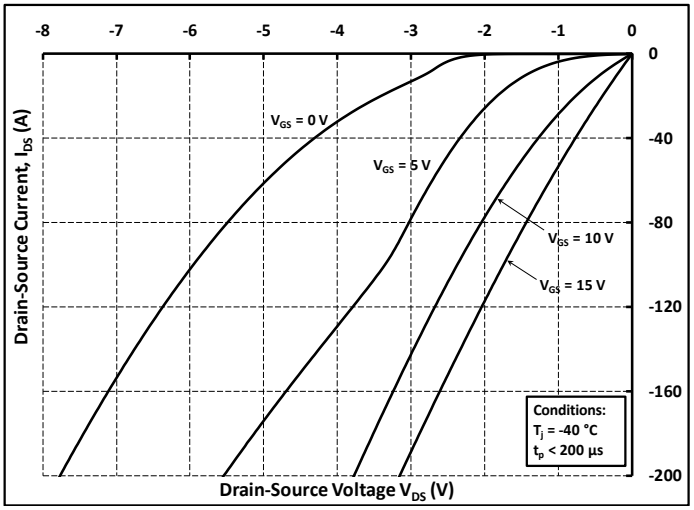



Figure 13. 3rd Quadrant Characteristic at -40 ºC

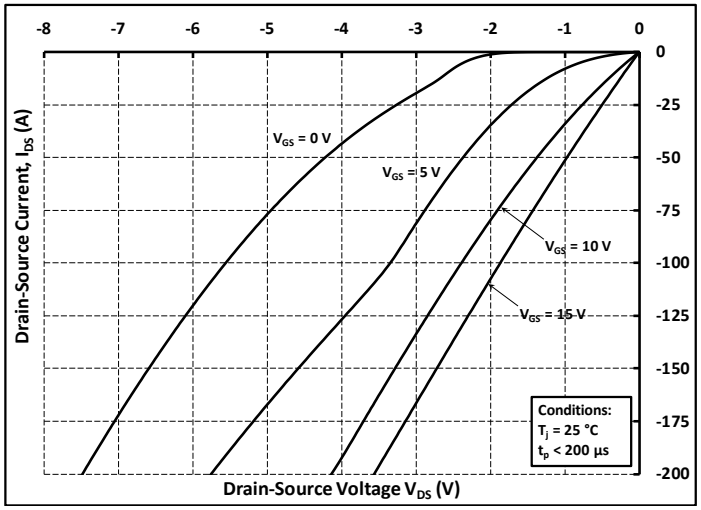



Figure 14. 3rd Quadrant Characteristic at 25 ºC

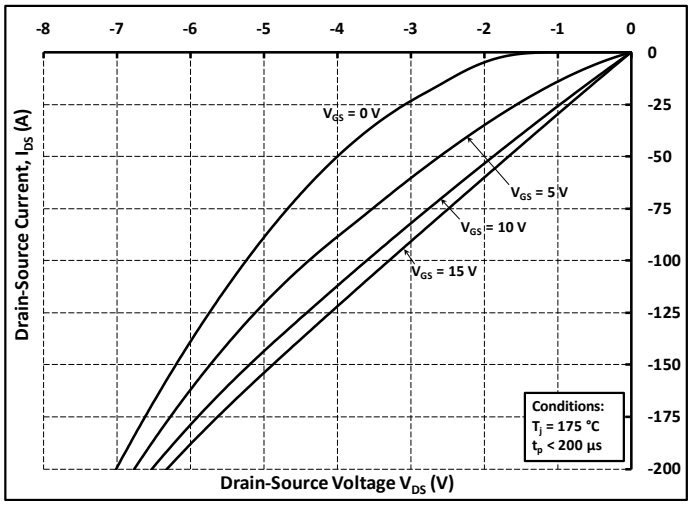



Figure 15. 3rd Quadrant Characteristic at 175 ºC

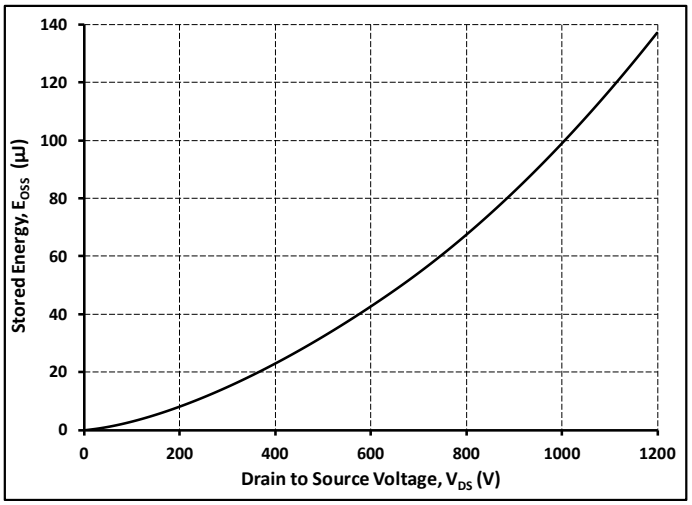



Figure 16. Output Capacitor Stored Energy

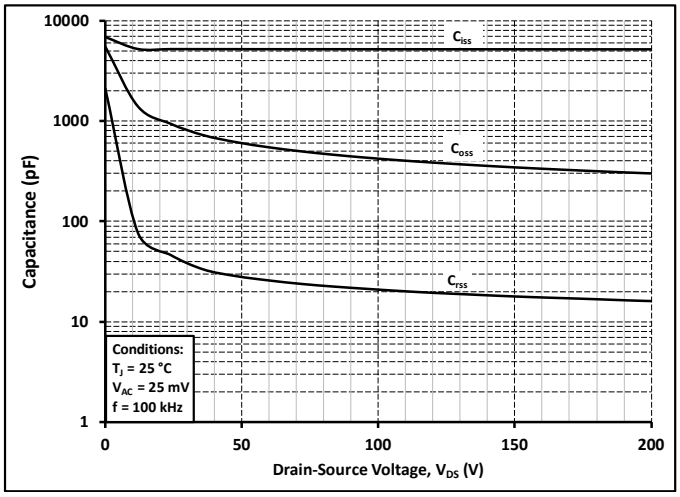



Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

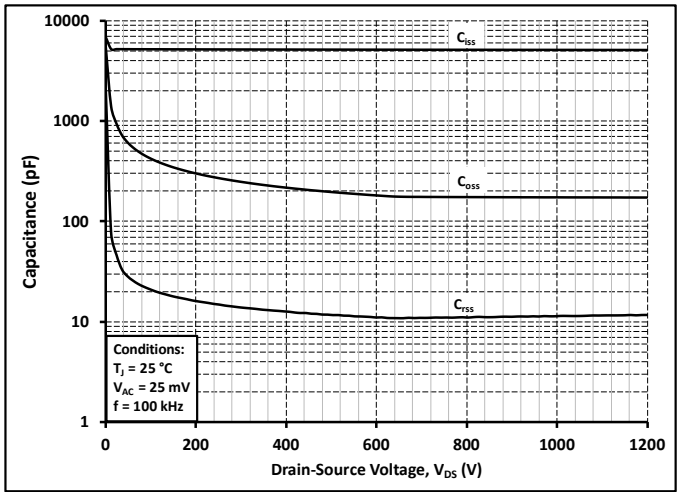



Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

## Typical Performance

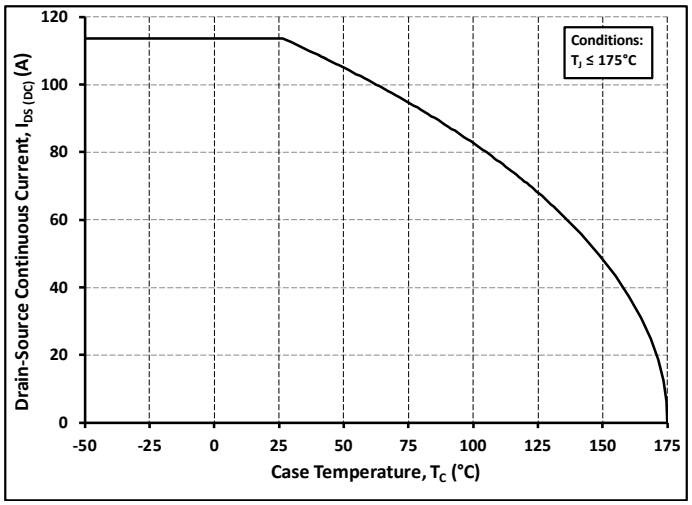



Figure 19. Continuous Drain Current Derating vs. Case Temperature

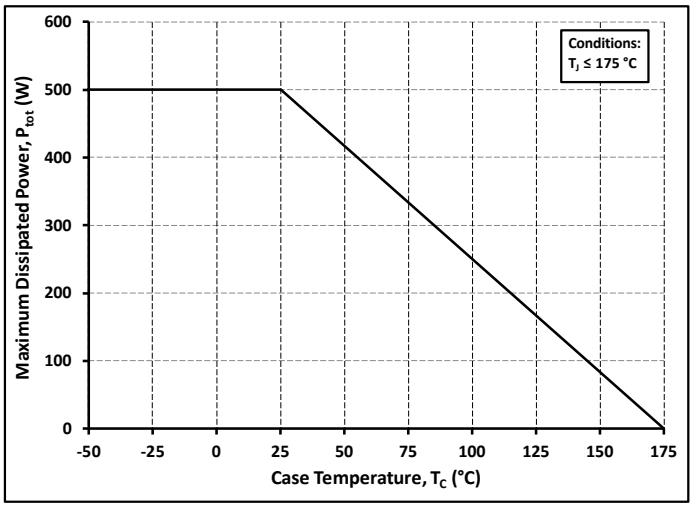



Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

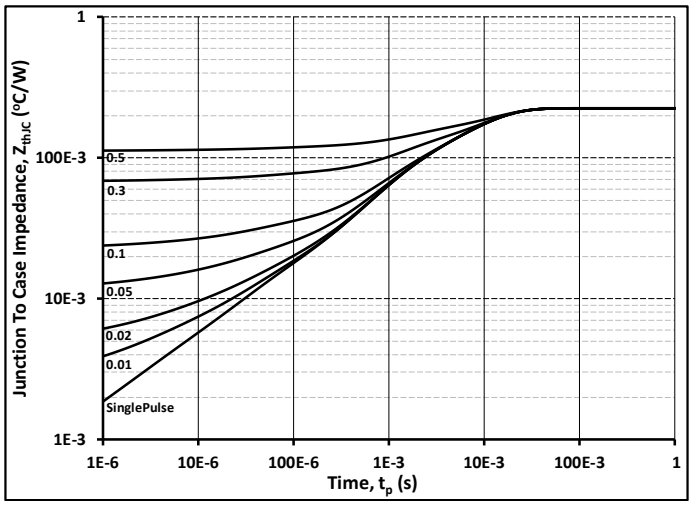



Figure 21. Transient Thermal Impedance (Junction - Case)

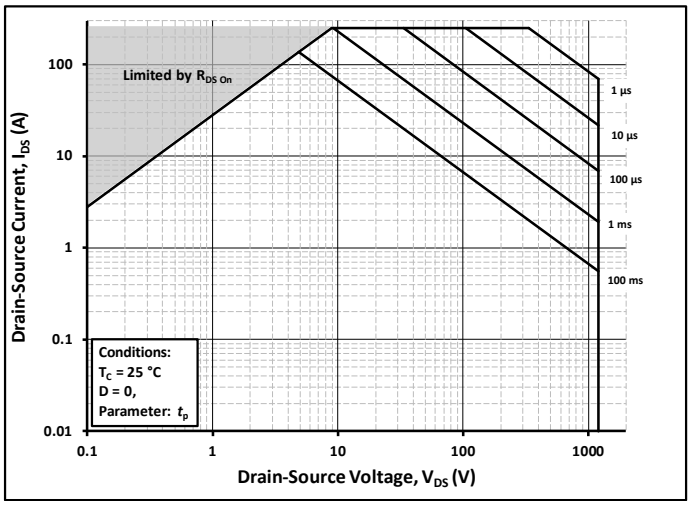



Figure 22. Safe Operating Area

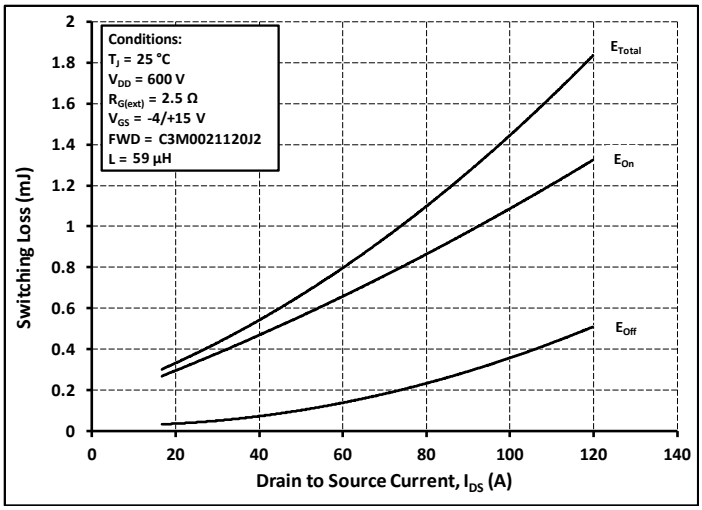



Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}$ = 600V)

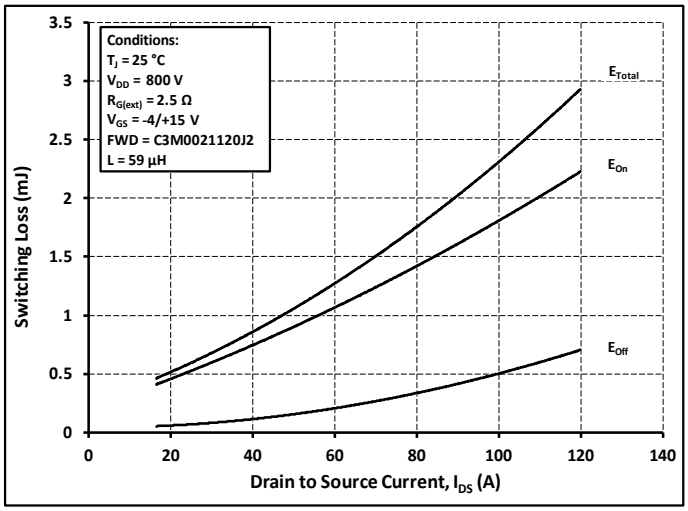



Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}$ = 800V)

## Typical Performance

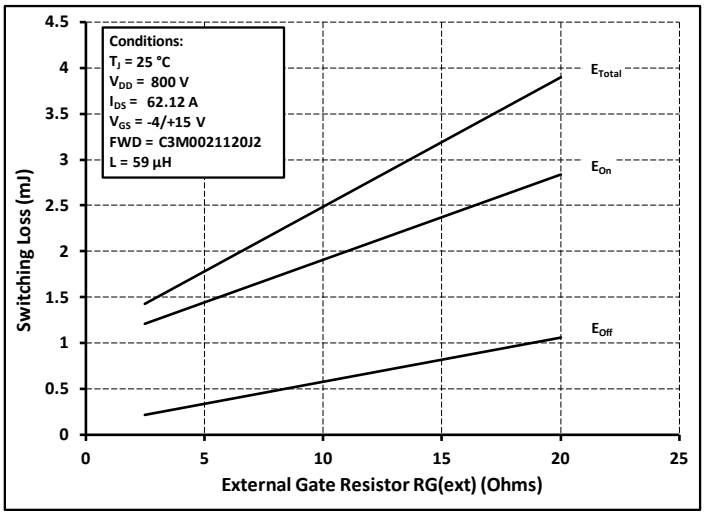



Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

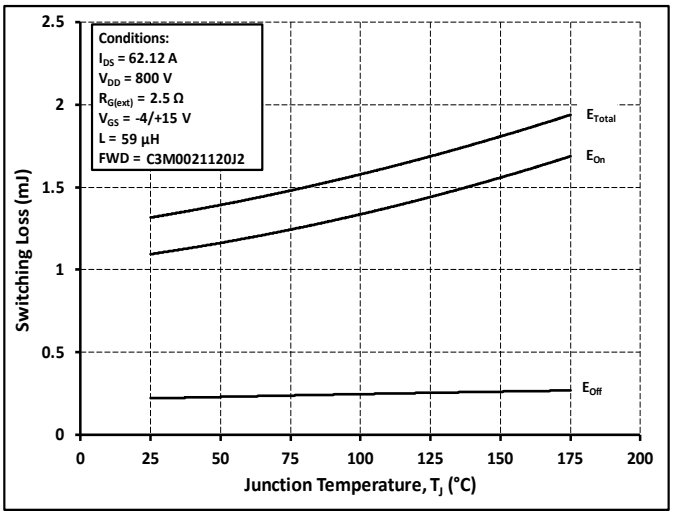



Figure 26. Clamped Inductive Switching Energy vs. Temperature

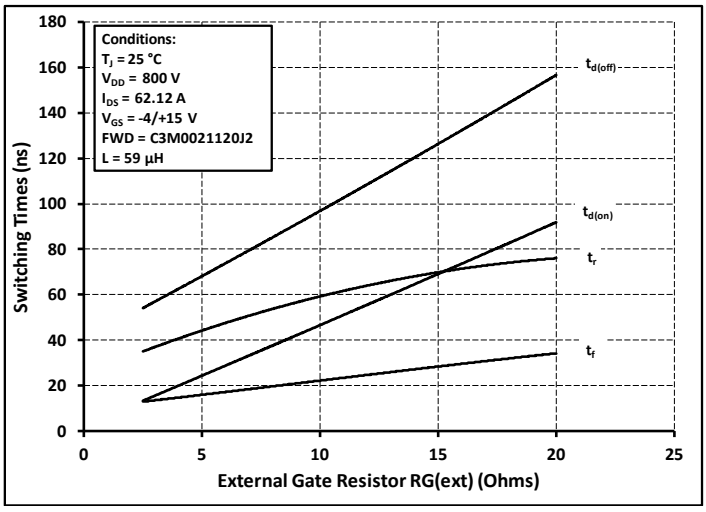



Figure 27. Switching Times vs. $R_{G(ext)}$

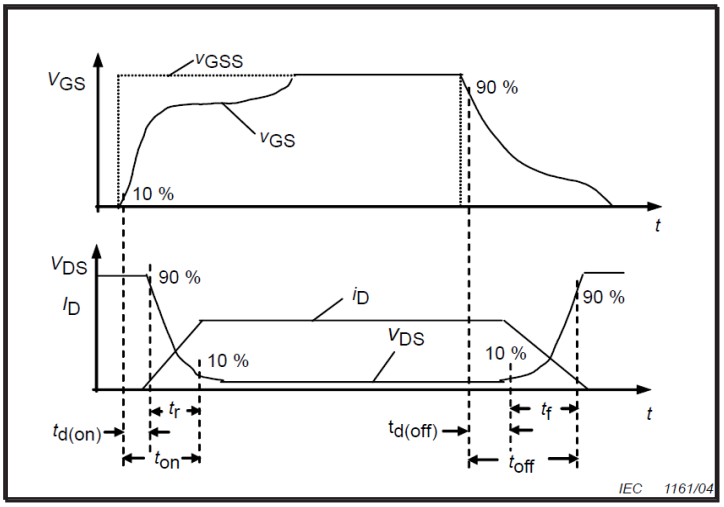



Figure 28. Switching Times Definition

## Test Circuit Schematic

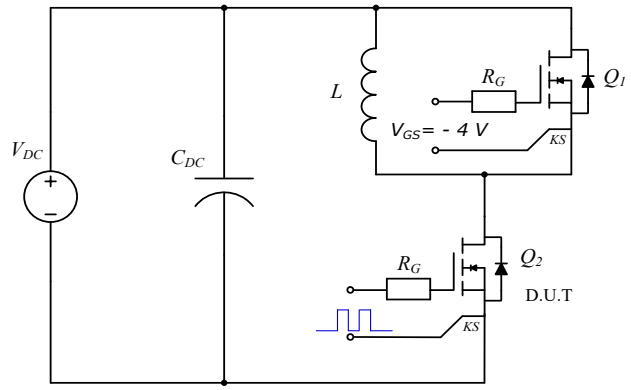
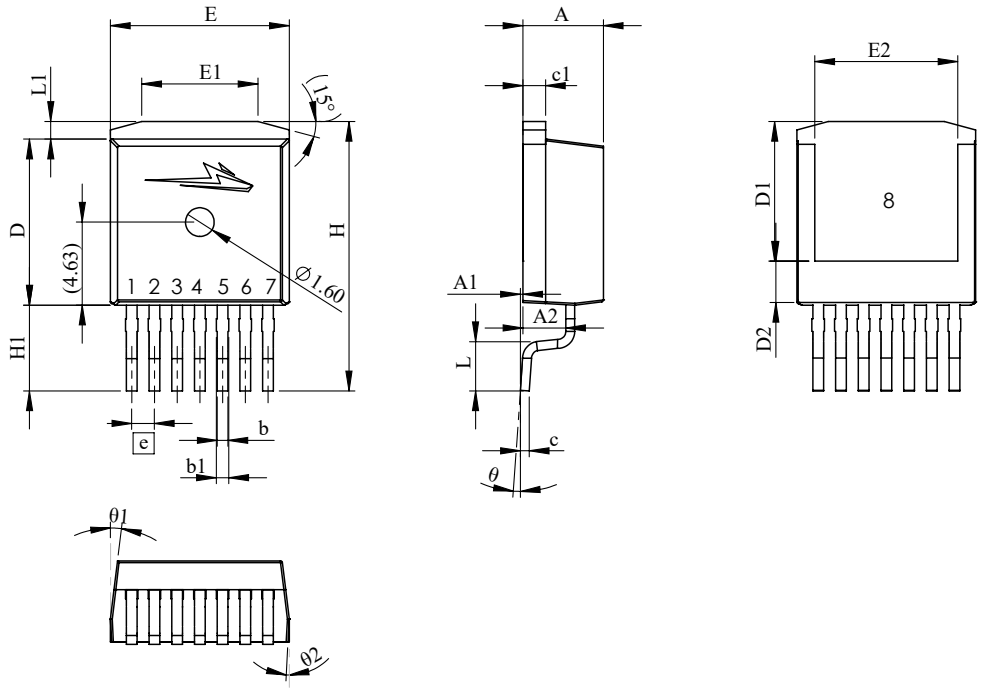



Figure 29. Clamped Inductive Switching Waveform Test Circuit

## Package Dimensions




| SYMBOL | MIN (mm) | MAX (mm) |
|---|---|---|
| A | 4.30 | 4.70 |
| A1 | 0.00 | 0.25 |
| A2 | 2.20 | 2.60 |
| b | 0.52 | 0.72 |
| b1 | 0.60 | 0.80 |
| c | 0.42 | 0.62 |
| c1 | 1.07 | 1.47 |
| D | 9.05 | 9.45 |
| D1 | 7.58 | 7.98 |
| D2 | 2.05 | 2.45 |
| E | 9.80 | 10.20 |
| E1 | 6.30 | 6.97 |
| E2 | 7.80 | 8.20 |
| e | 1.27 BSC | |
| H | 14.87 | 15.27 |
| H1 | 4.55 | 4.95 |
| L | 2.48 | 2.88 |
| L1 | 0.87 | 1.27 |
| θ | 0° | 8° |
| θ1 | 4° | 10° |
| θ2 | 0° | 6° |

| | |
|---|---|
| 1 | GATE |
| 2 | KELVIN |
| 3 | SOURCE |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | DRAIN |

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

TITLE: PACKAGE OUTLINE DRAWING: TO-263-7L (J2)

Date: 03/17/23

REVISION NO. 01

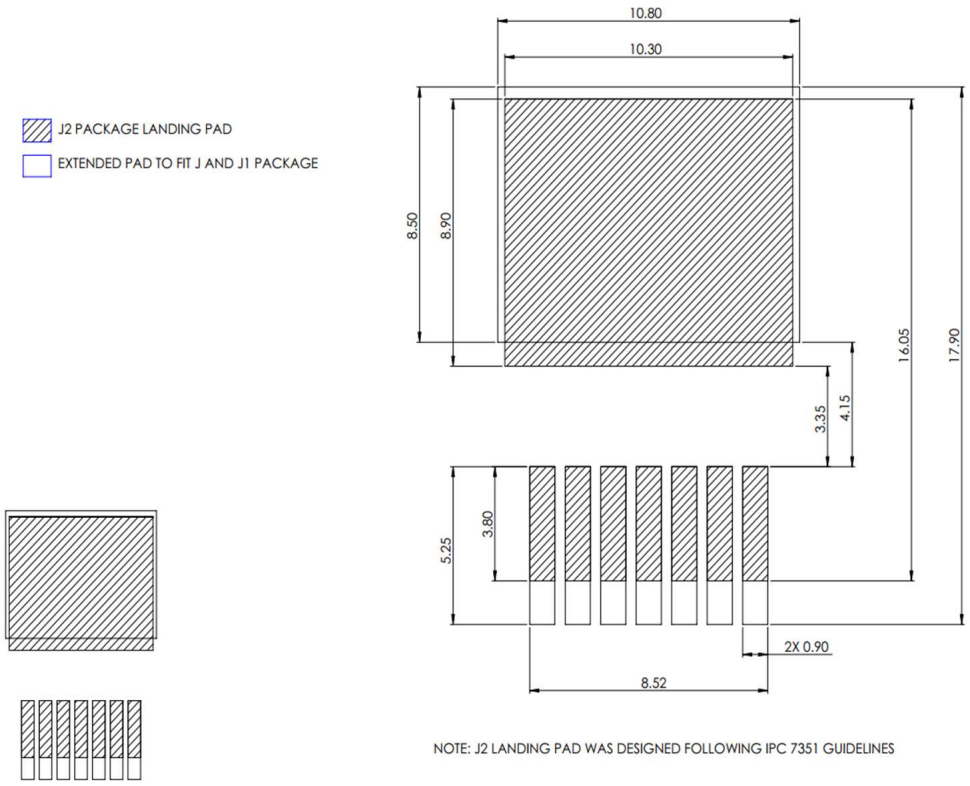
A4

SCALE:1:1

SHEET 1 OF 1

## Recommended Solder Pad Layout

All dimensions in mm




NOTE: J2 LANDING PAD WAS DESIGNED FOLLOWING IPC 7351 GUIDELINES

## Revision history

| Document Version | Date of release | Descriptiion of changes |
|---|---|---|
| 1 | March 2024 | Initial release |

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