

C3M0040120K1

Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- Optimized package with separate driver source pin
- Lower profile TO-247-4 package body
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

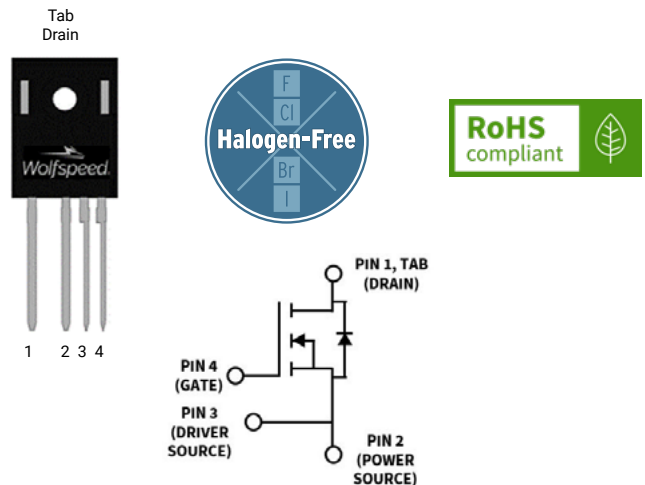
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters
- Solar/ESS
- UPS
- Enterprise PSU

Package



Part Number	Package	Marking
C3M0040120K1	TO-247-4L LP	C3M0040120K1

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	v	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			57	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19
				41		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
Pulsed Drain Current	I_{DM}			128		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			242	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.7	3.8	V	$V_{DS} = V_{GS}, I_D = 8.77\ \text{mA}$	Fig. 11
			2.2		V	$V_{DS} = V_{GS}, I_D = 8.77\ \text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 1200\ \text{V}, V_{GS} = 0\ \text{V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		39	53	m Ω	$V_{GS} = 15\ \text{V}, I_D = 31.9\ \text{A}$	Fig. 4, 5, 6
			70			$V_{GS} = 15\ \text{V}, I_D = 31.9\ \text{A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		22		S	$V_{DS} = 20\ \text{V}, I_{DS} = 31.9\ \text{A}$	Fig. 7
			20			$V_{DS} = 20\ \text{V}, I_{DS} = 31.9\ \text{A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		2726		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 1000\ \text{V}$ $F = 100\ \text{kHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		100				
C_{riss}	Reverse Transfer Capacitance		6				
E_{oss}	C_{oss} Stored Energy		56		μJ		
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		127		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0... 800\ \text{V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		197		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		300		μJ	$V_{DS} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 31.9\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 98\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC DIODE	Fig. 26, 28
E_{OFF}	Turn Off Switching Energy (External Diode)		73				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		658		μJ	$V_{DS} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 31.9\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 98\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26, 28
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		74				
$t_{d(on)}$	Turn-On Delay Time		13		ns	$V_{DD} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 31.9\ \text{A}, R_{G(ext)} = 2.5\ \Omega,$ Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		16				
$t_{d(off)}$	Turn-Off Delay Time		23				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		2.2		Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Q_{gs}	Gate to Source Charge		32		nC	$V_{DS} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 31.9\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		28				
Q_g	Total Gate Charge		94				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 800V
 $C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 800V



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	$V_{GS} = -4\text{ V}, I_{SD} = 15.95\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.3		V	$V_{GS} = -4\text{ V}, I_{SD} = 15.95\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		43	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
I_{SM}	Diode pulse Current		128	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recover time	18		ns	$V_{GS} = -4\text{ V}, I_{SD} = 31.9\text{ A}, V_R = 800\text{ V}$ $dif/dt = 8350\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	811		nC		
I_{rrm}	Peak Reverse Recovery Current	79		A		
t_{rr}	Reverse Recover time	32		ns	$V_{GS} = -4\text{ V}, I_{SD} = 31.9\text{ A}, V_R = 800\text{ V}$ $dif/dt = 2250\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	603		nC		
I_{rrm}	Peak Reverse Recovery Current	30		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.46	$^\circ\text{C}/\text{W}$		Fig. 21



Typical Performance

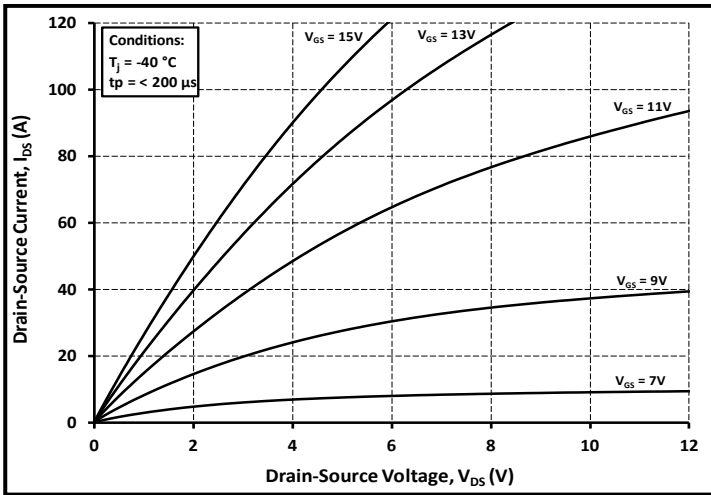


Figure 1. Output Characteristics $T_J = -40\text{ }^\circ\text{C}$

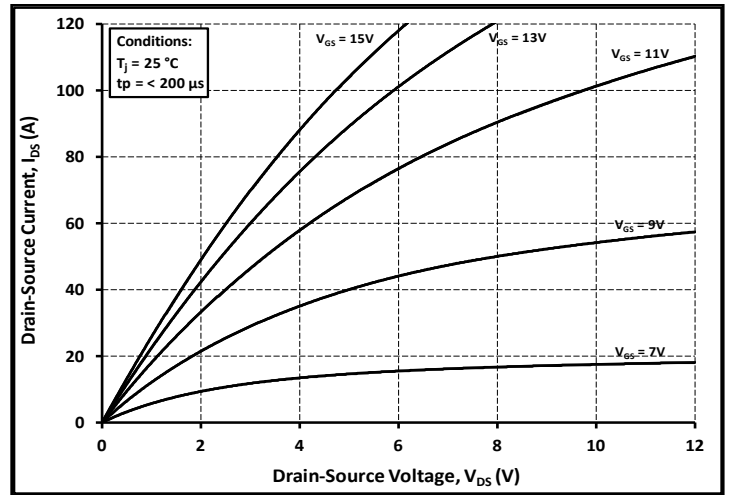


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

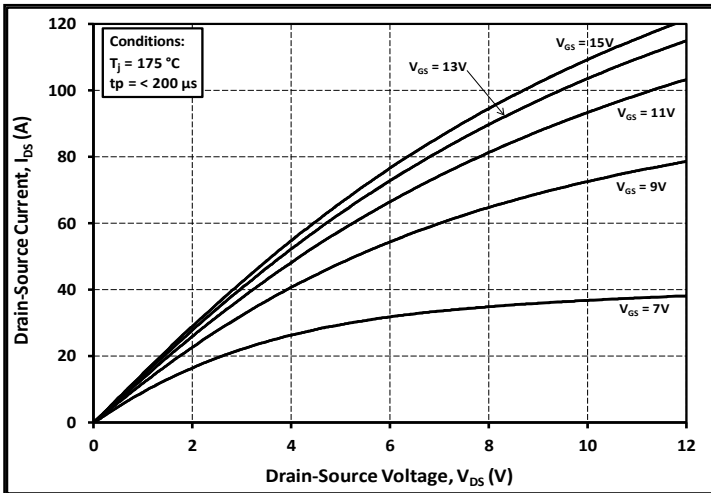


Figure 3. Output Characteristics $T_J = 175\text{ }^\circ\text{C}$

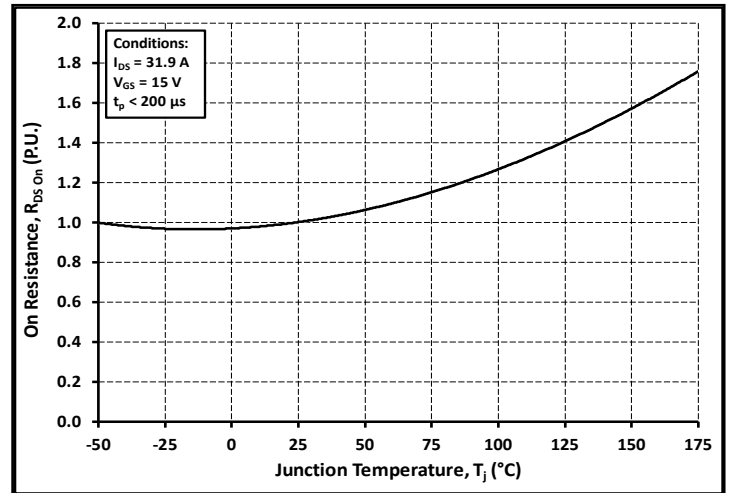


Figure 4. Normalized On-Resistance vs. Temperature

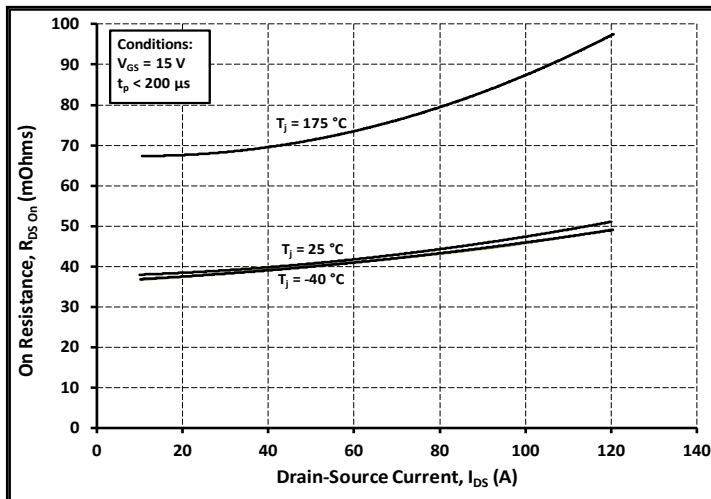


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

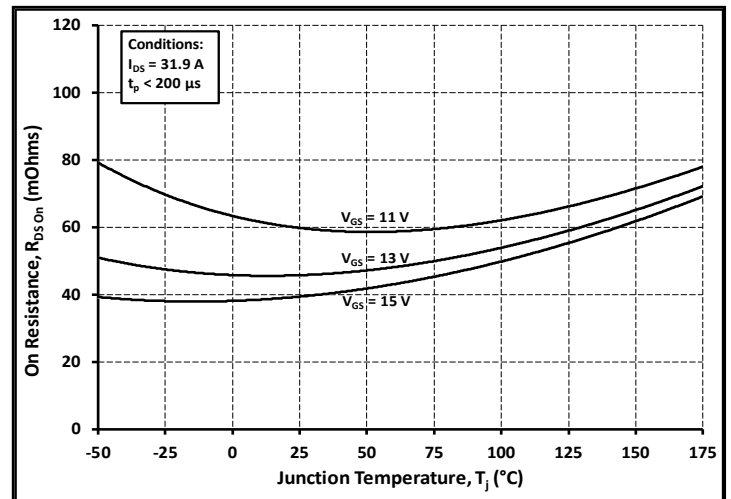


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

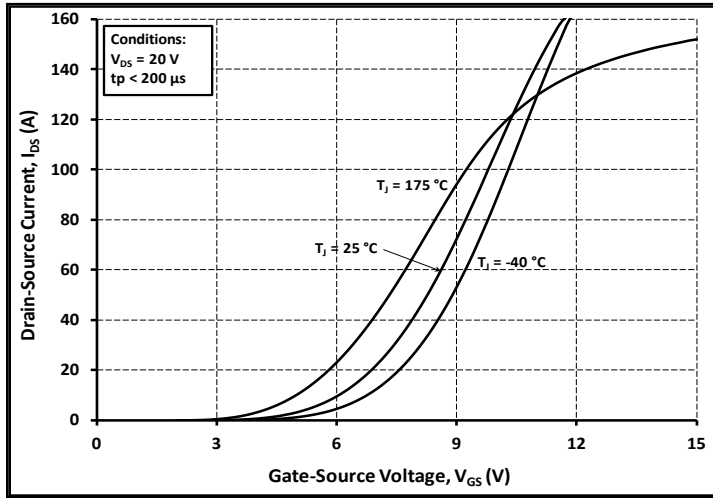


Figure 7. Transfer Characteristic for Various Junction Temperatures

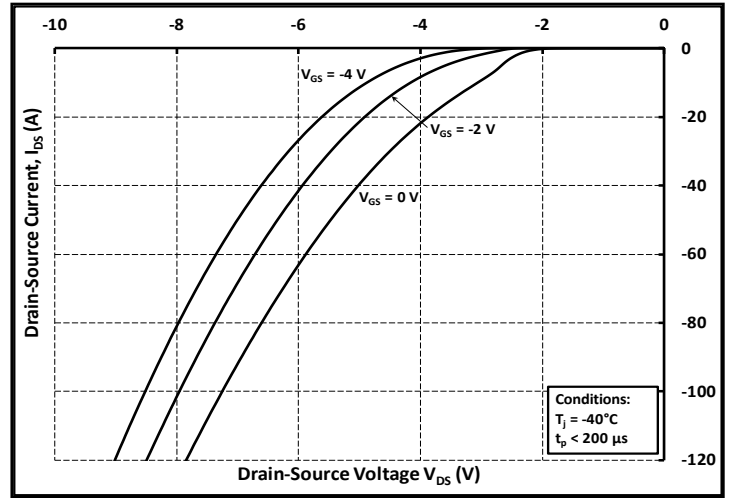


Figure 8. Body Diode Characteristic at -40 °C

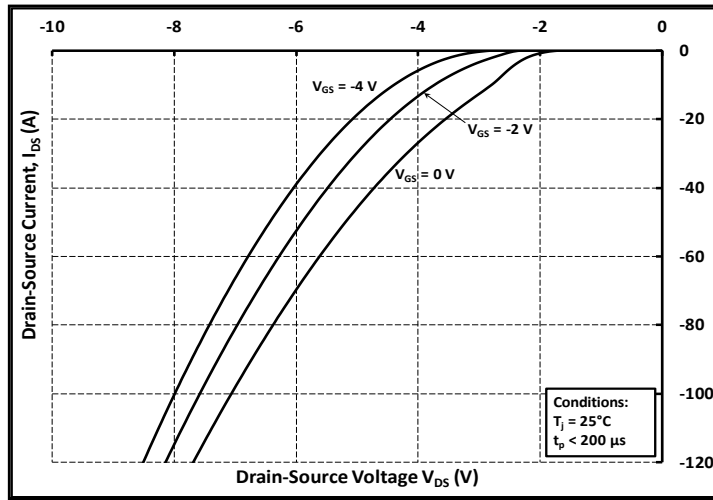


Figure 9. Body Diode Characteristic at 25 °C

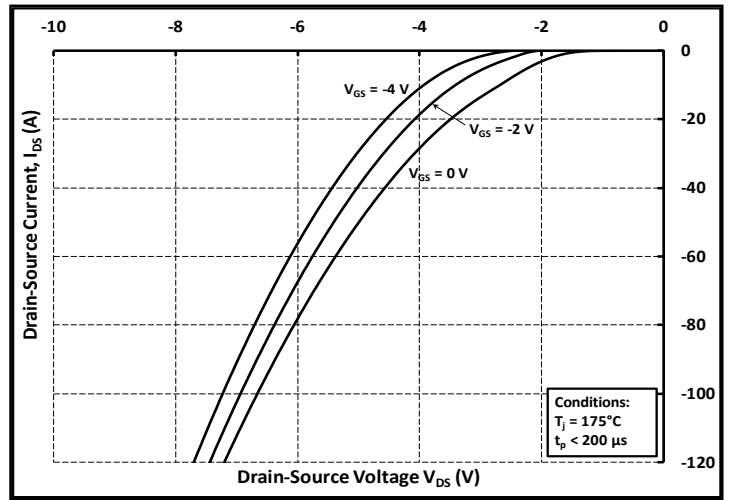


Figure 10. Body Diode Characteristic at 175 °C

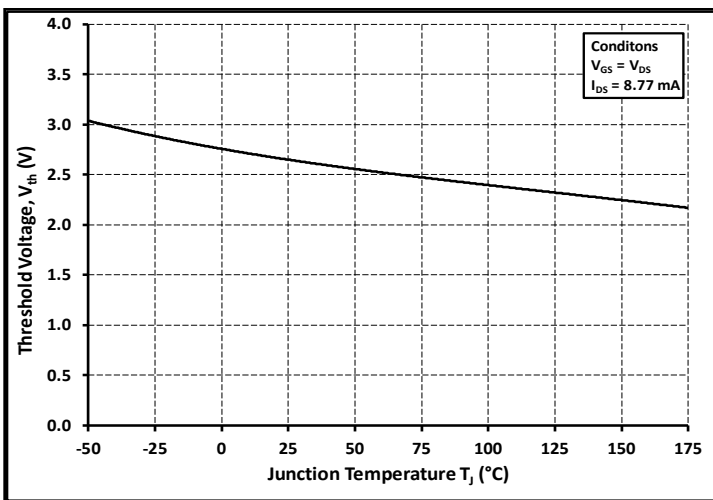


Figure 11. Threshold Voltage vs. Temperature

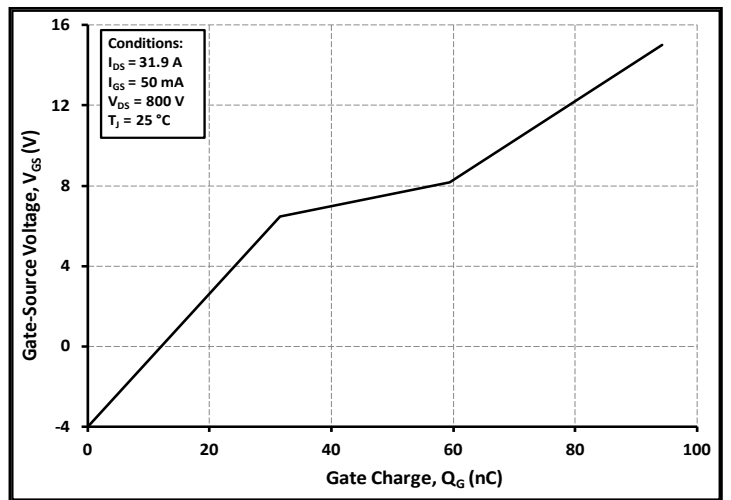


Figure 12. Gate Charge Characteristics



Typical Performance

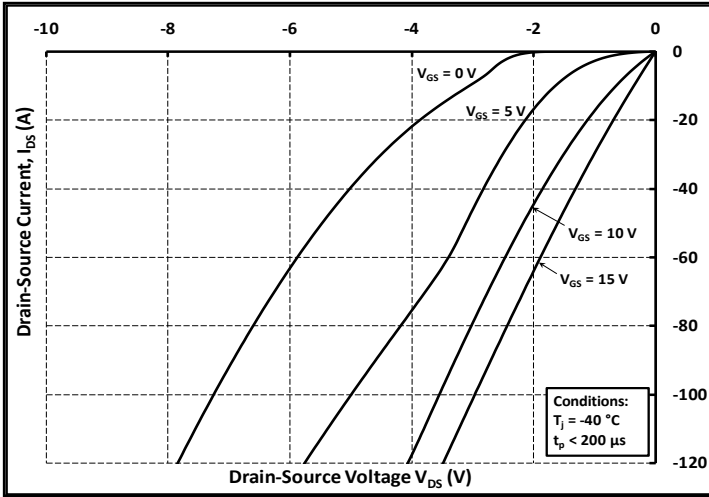


Figure 13. 3rd Quadrant Characteristic at $-40\text{ }^{\circ}\text{C}$

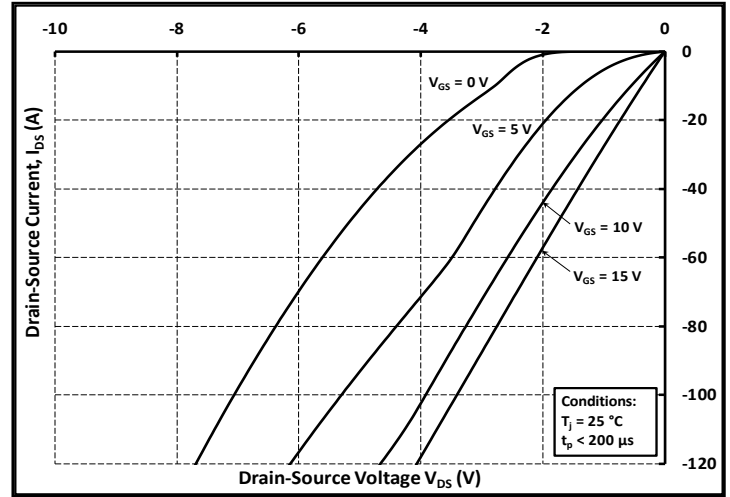


Figure 14. 3rd Quadrant Characteristic at $25\text{ }^{\circ}\text{C}$

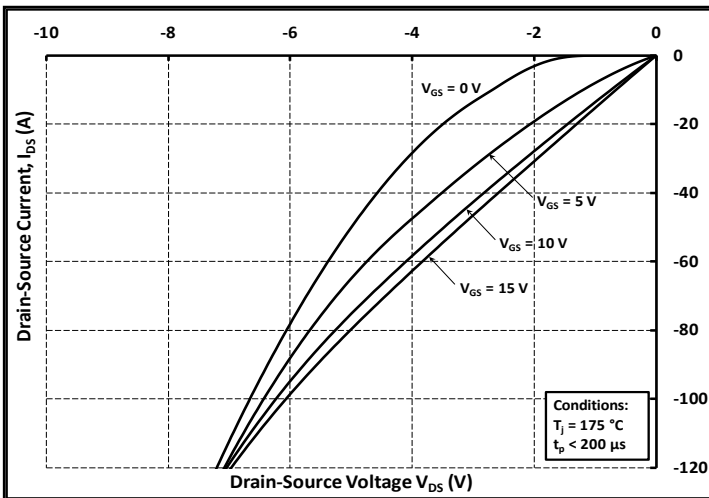


Figure 15. 3rd Quadrant Characteristic at $175\text{ }^{\circ}\text{C}$

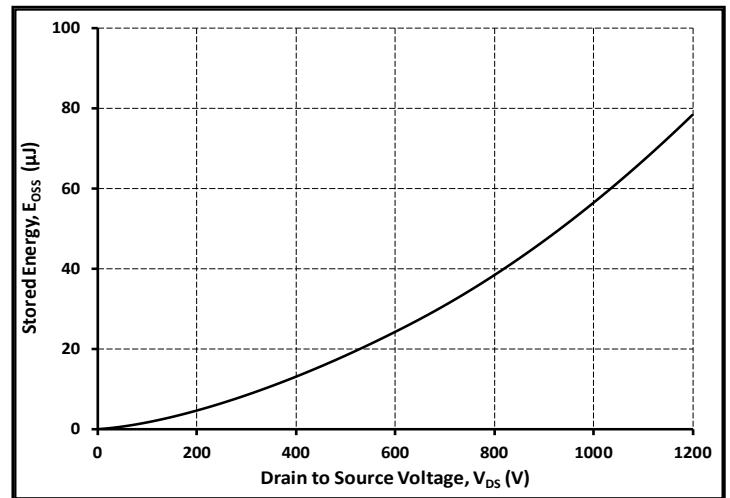


Figure 16. Output Capacitor Stored Energy

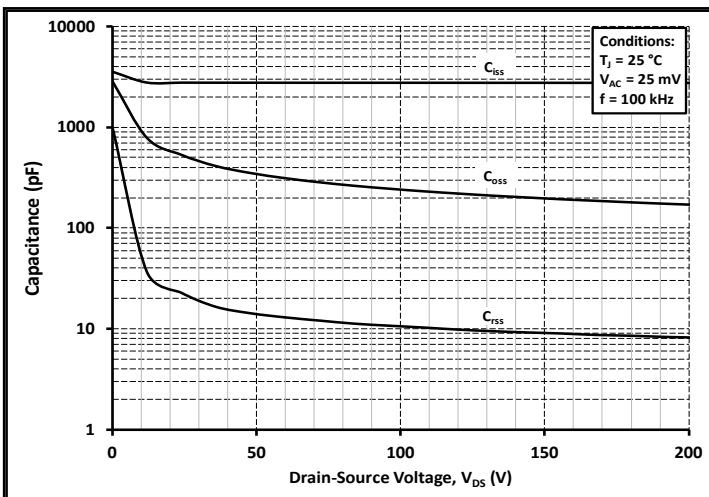


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

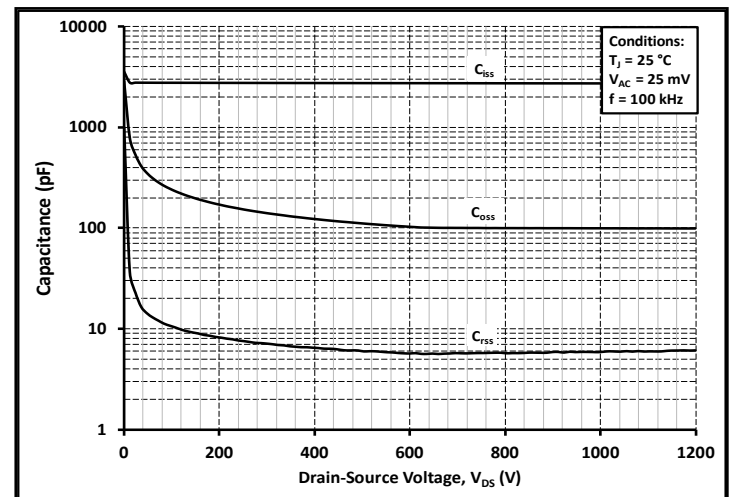


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)



Typical Performance

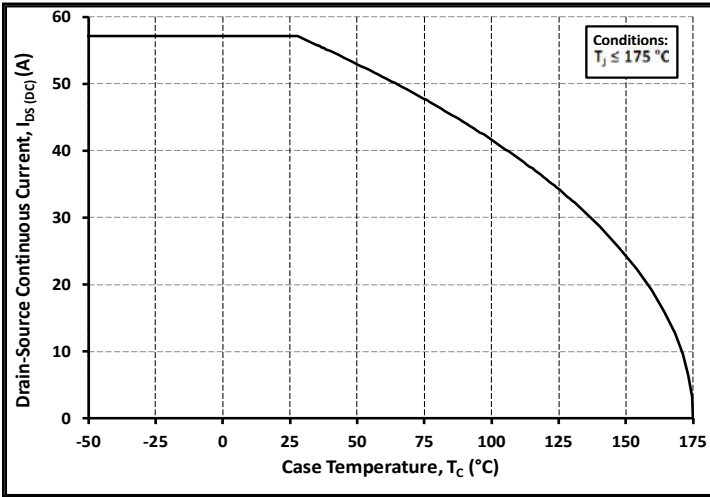


Figure 19. Continuous Drain Current Derating vs. Case Temperature

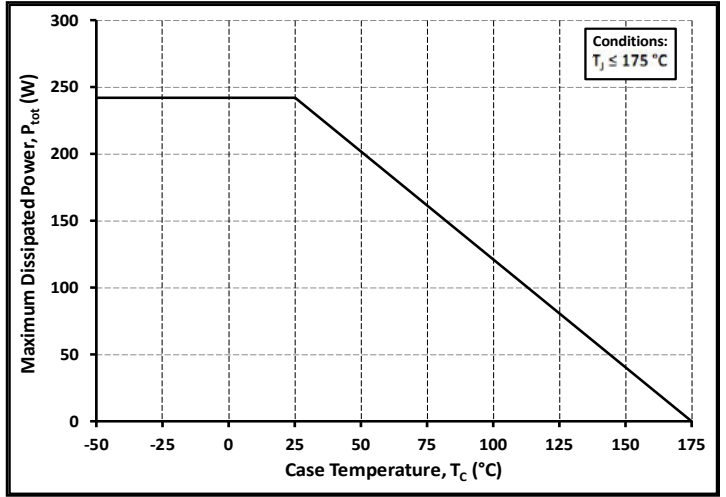


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

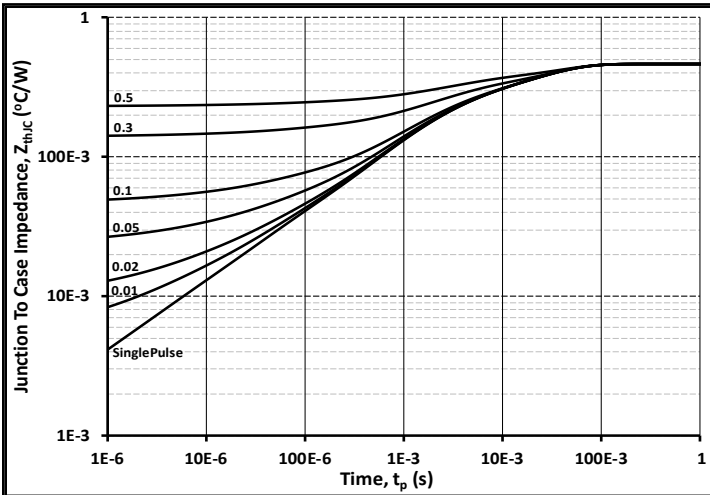


Figure 21. Transient Thermal Impedance (Junction - Case)

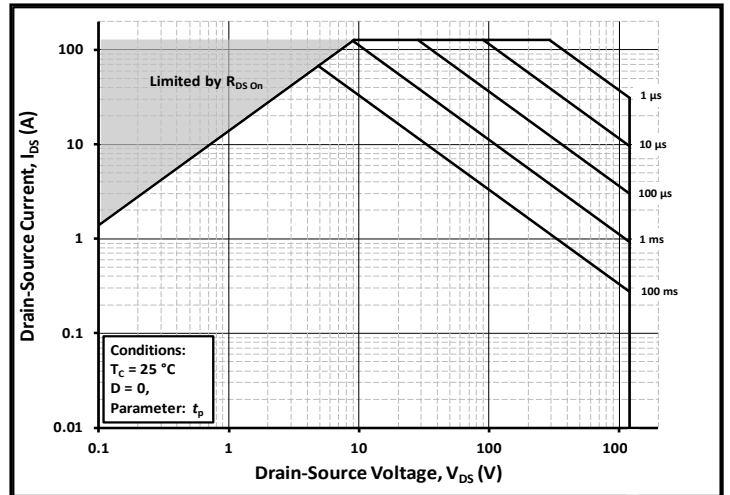


Figure 22. Safe Operating Area

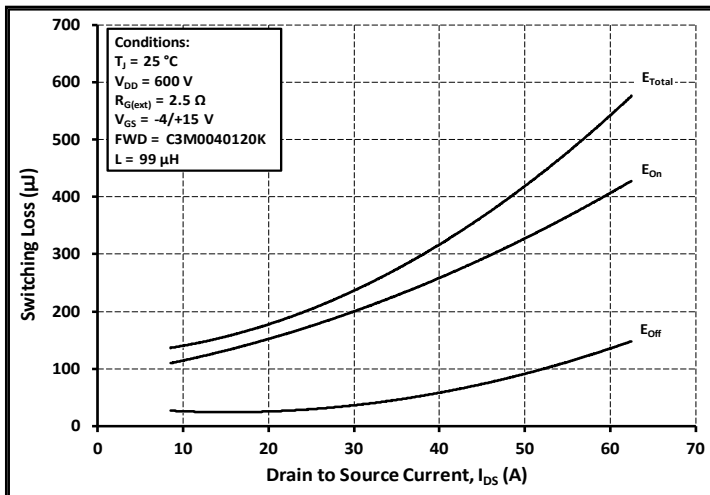


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600V$)

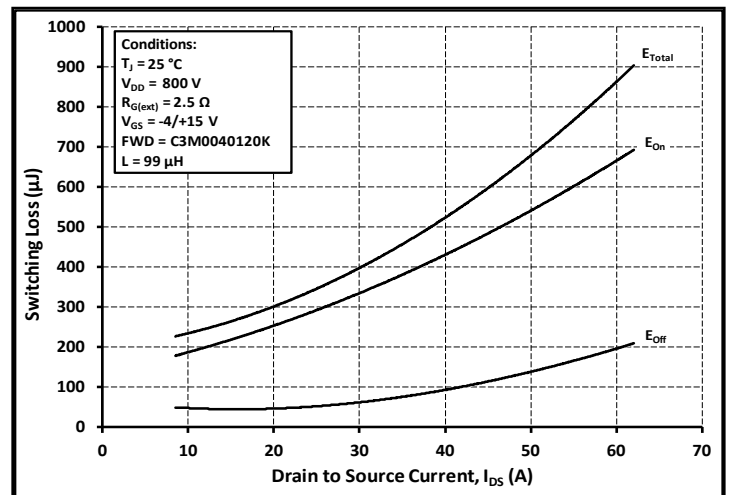


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800V$)



Typical Performance

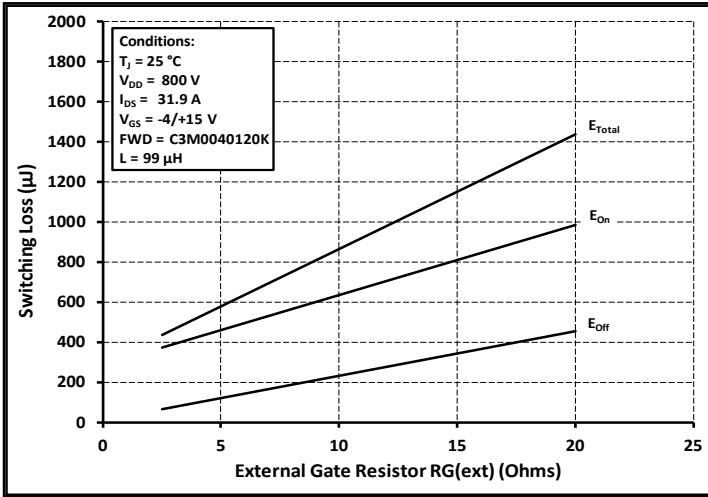


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

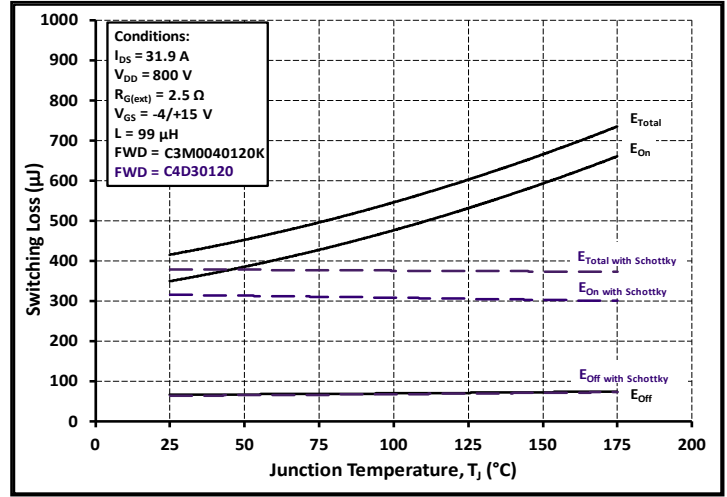


Figure 26. Clamped Inductive Switching Energy vs. Temperature

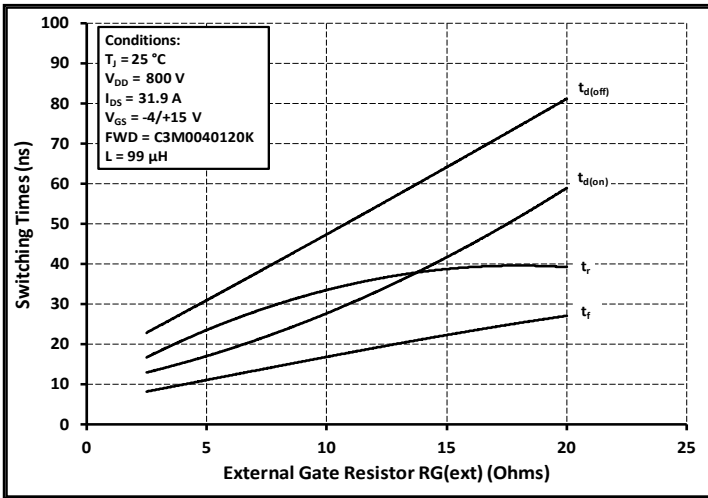


Figure 27. Switching Times vs. $R_{G(ext)}$

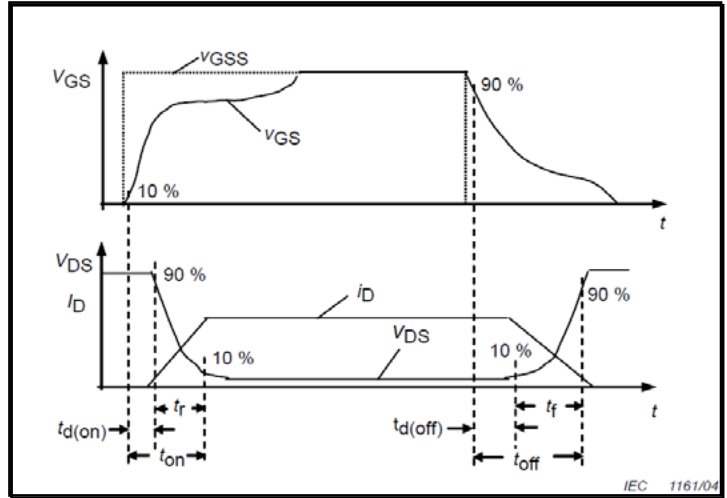


Figure 28. Switching Times Definition

Test Circuit Schematic

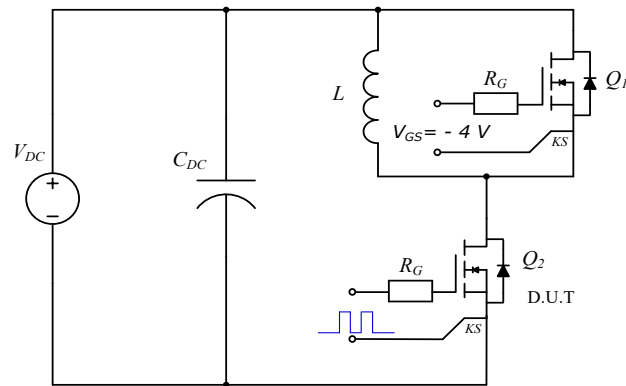
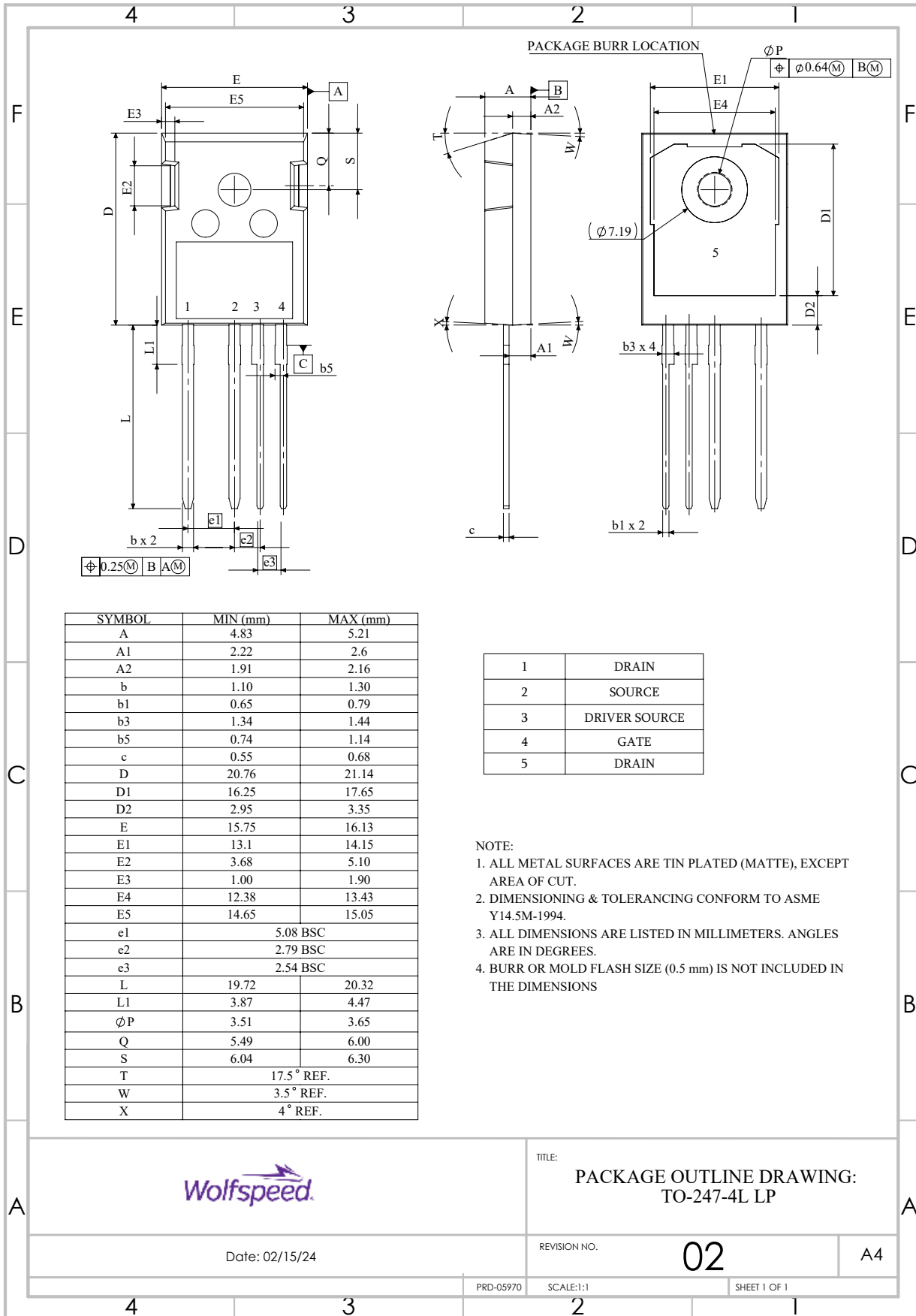


Figure 29. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



TITLE:
PACKAGE OUTLINE DRAWING:
TO-247-4L LP

Date: 02/15/24

REVISION NO.

02

A4

PRD-05970

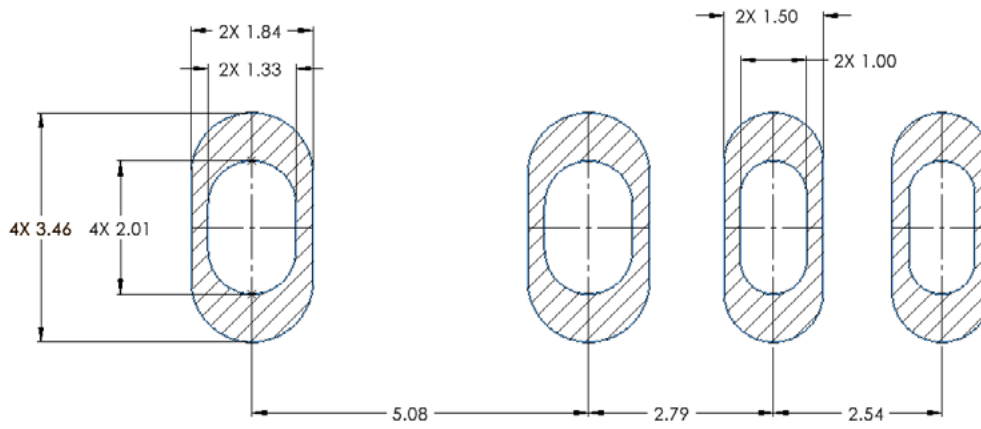
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SHEET 1 OF 1



Recommended Solder Pad Layout

All dimensions in mm





Revision history

Document Version	Date of release	Description of changes
1.0	April-2024	Initial datasheet



Notes & Disclaimer

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