Ordering number:EN3145

NPN Triple Diffused Planar Silicon Transistor

2SC4599

Switching Regulator Applications

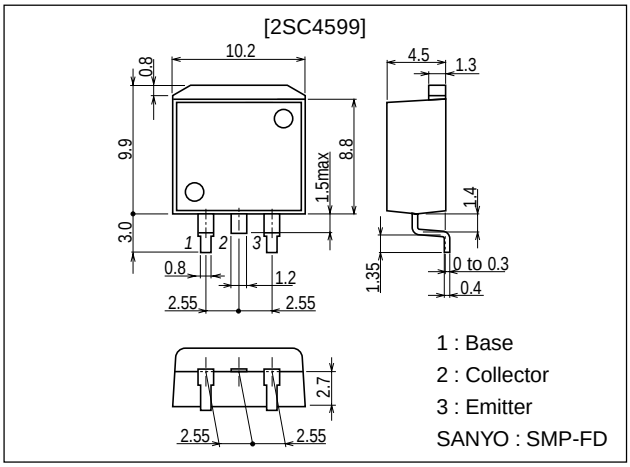
Features

- Surface mount type device making the following possible.
  -Reduction in the number of manufacturing processes for 2SC4599-applied equipment.
  -High density surface mount applications.
  -Small size of 2SC4599-applied equipment.
- High breakdown voltage, high reliability.
- Fast switching speed.
- Wide ASO.
- Adoption of MBIT process.

Package Dimensions

unit:mm

2069C



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		800	V
Collector-to-Emitter Voltage	V_{CEO}		500	V
Emitter-to-Base Voltage	V_{EBO}		7	V
Collector Current	I_C		3	A
Collector Current (Pulse)	I_{CP}	PW≤300μs, duty cycle≤10%	6	A
Base Current	I_B		1	A
Collector Dissipation	P_C		1.65	W
		Tc=25˚C	40	W
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=500V, I_E=0			10	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=5V, I_C=0			10	μA
DC Current Gain	$h_{FE}1$	V_{CE}=5V, I_C=0.3A	15*		50*	
	$h_{FE}2$	V_{CE}=5V, I_C=1.5A	8			

* : For the $h_{FE}1$ of the 2SC4599, specify two ranks or more in principle.

15	L	30	20	M	40	30	N	50

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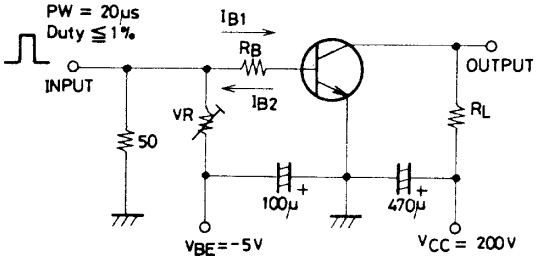
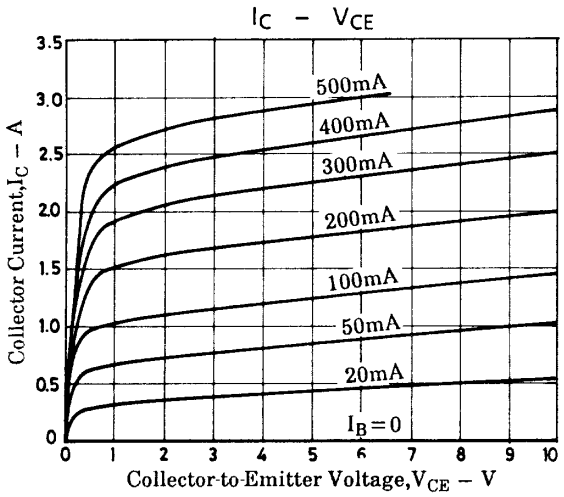
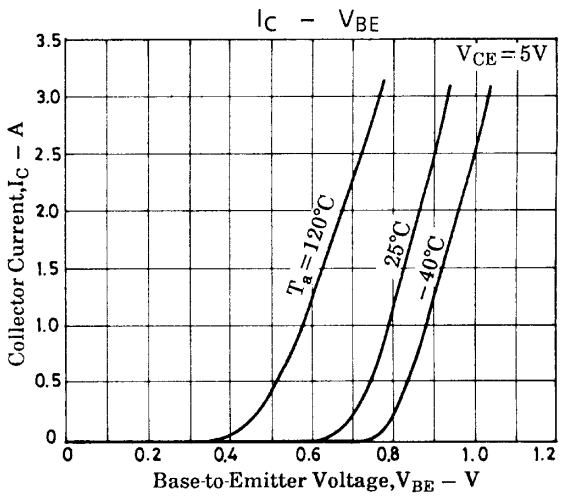
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=0.3A		18		MHz
Output Capacitance	C_{ob}	V_{CB}=10V, f=1MHz		50		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=1.5A, I_B=0.3A			1.0	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=1.5A, I_B=0.3A			1.5	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=1mA, I_E=0	800			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=5mA, R_{BE}=∞	500			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=1mA, I_C=0	7			V
Collector-to-Emitter Sustain Voltage	$V_{CEX(sus)}$	I_C=1.5A, I_{B1}=0.6A, L=2mH, I_{B2}=–0.6A, clamped	500			V
Turn-ON Time	t_{on}	I_C=2A, I_{B1}=0.4A, I_{B2}=–0.8A, R_L=100Ω, V_{CC}=200V			0.5	μs
Storage Time	t_{stg}	I_C=2A, I_{B1}=0.4A, I_{B2}=–0.8A, R_L=100Ω, V_{CC}=200V			3.0	μs
Fall Time	t_f	I_C=2A, I_{B1}=0.4A, I_{B2}=–0.8A, R_L=100Ω, V_{CC}=200V			0.3	μs

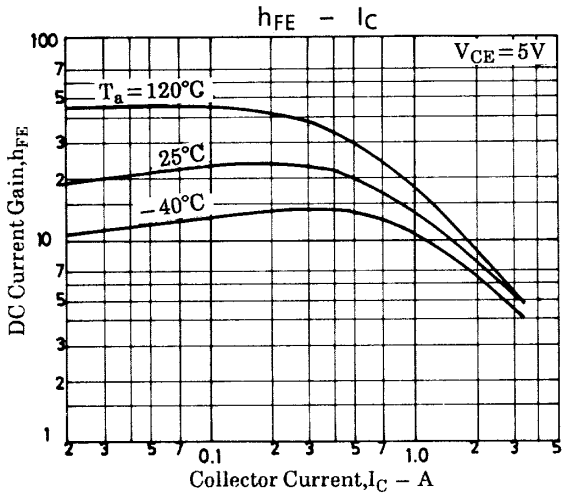
Switching Time Test Circuit

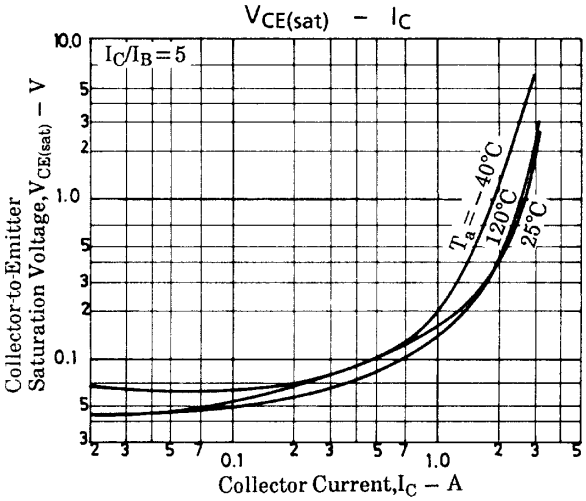


Unit (resistance : Ω, capacitance : F)

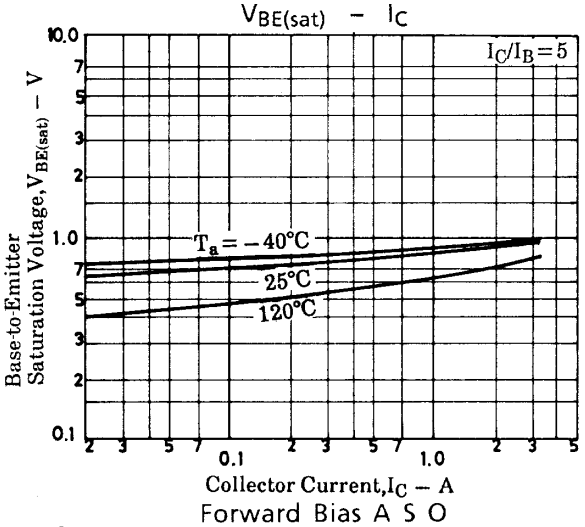




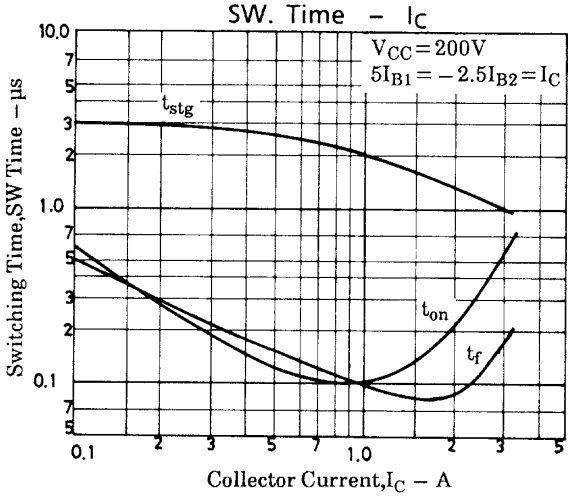




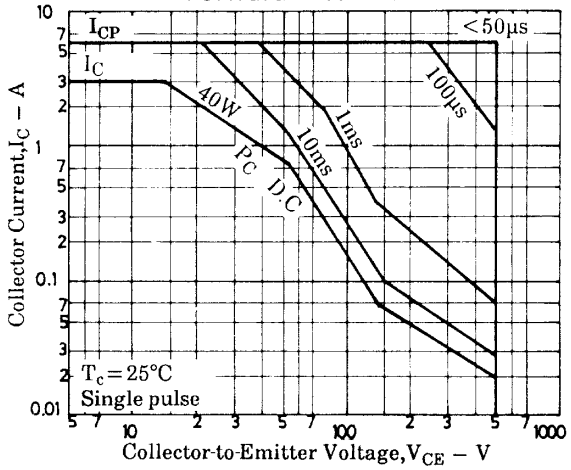
$V_{BE(sat)}$ – I_C



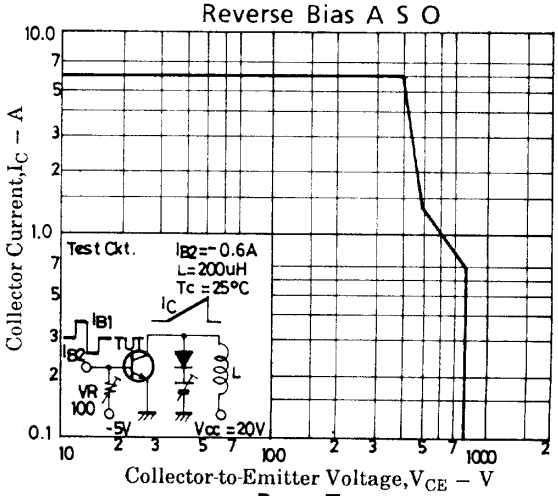
SW. Time – I_C



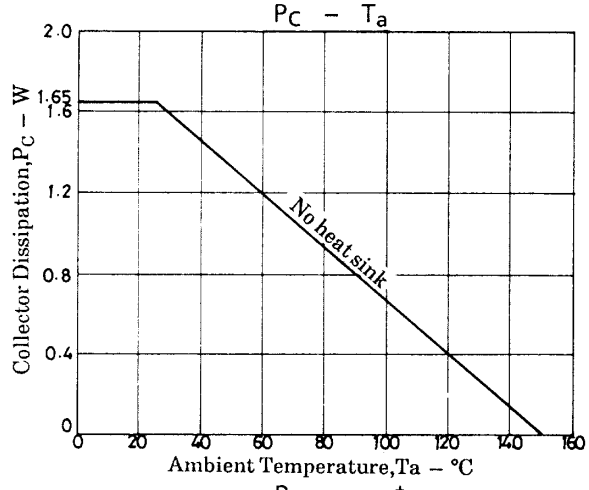
Forward Bias A S O



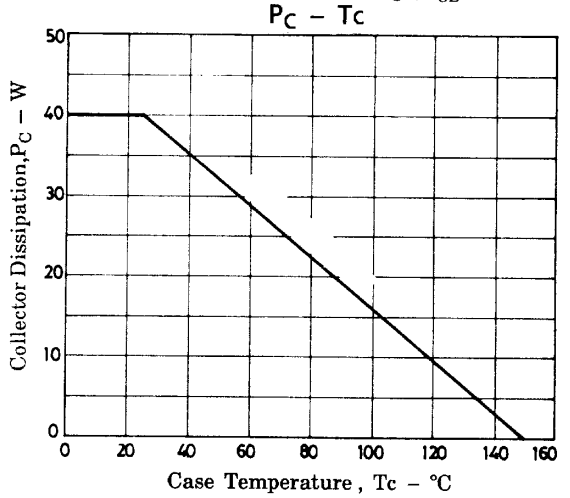
Reverse Bias A S O



P_C – T_a



P_C – Tc



$R_{th(t)}$ – t