Ordering number:ENN3880A

NPN Epitaxial Planar Silicon Transistor

2SC4737

50V/2A Driver Applications

Applications

· Suitable for use in switching of L load (motor drivers, printer hammer drivers, relay drivers).

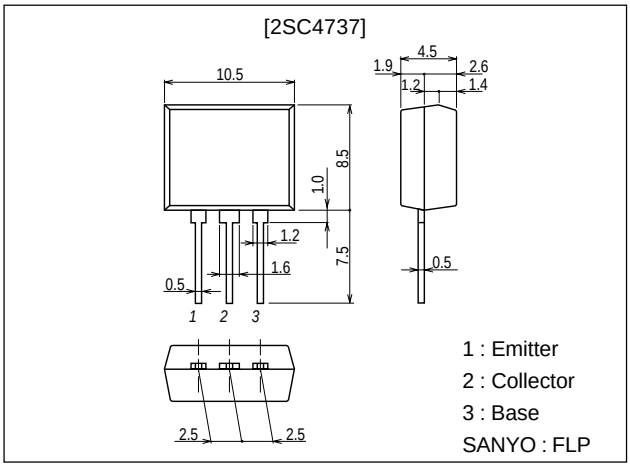
Features

· High DC current gain.
· Wide ASO.
· On-chip Zener diode of 60±10V between collector and base.
· Uniformity in collector-to-base breakdown voltage.
· High inductive load handling capability.

Package Dimensions

unit:mm

2084B



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}	With a low-voltage diode (60±10V)	50	V
Collector-to-Emitter Voltage	V_{CEO}	With a low-voltage diode (60±10V)	50	V
Emitter-to-Base Voltage	V_{EBO}		6	V
Collector Current	I_C		2	A
Collector Current (Pulse)	I_{CP}		4	A
Collector Dissipation	P_C		1.5	W
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=40V, I_E=0			10	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=5V, I_C=0			2	mA
DC Current Gain	h_{FE}	V_{CE}=5V, I_C=1A	1000	4000		
Gain-Bandwidth Product	f_T	V_{CE}=5V, I_C=1A		180		MHz
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=1A, I_B=4mA		1.0	1.5	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=1A, I_B=4mA			2.0	V
Inductive Load Handling Capability	Es/b	L=100mH, R_{BE}=100Ω	25			mJ

Continued on next page.

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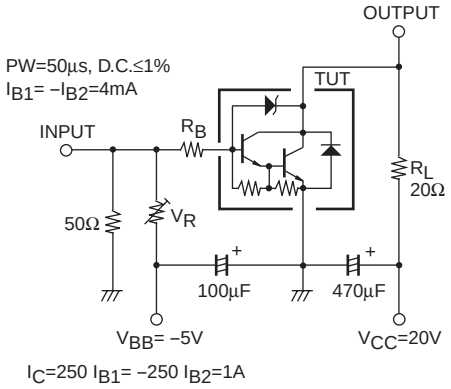
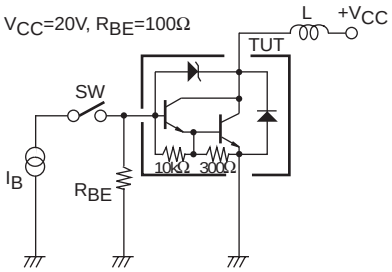
Continued from preceding page.

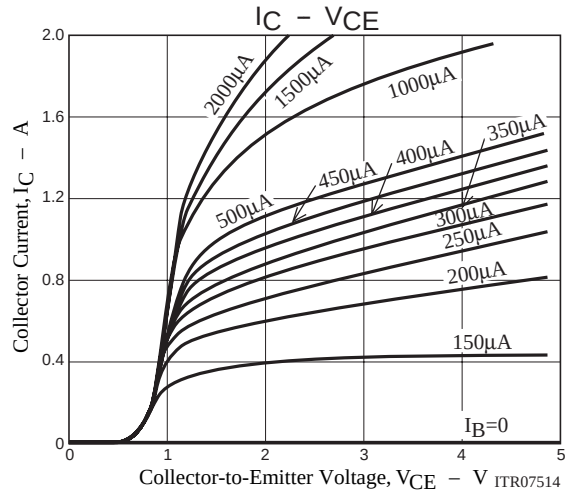
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	50	60	70	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, R_{BE}=∞	50	60	70	V
Turn-on Time	t_{on}	See specified Test Circuit.		0.2		μs
Storage Time	t_{stg}	See specified Test Circuit.		3.5		μs
Fall Time	t_f	See specified Test Circuit.		0.5		μs

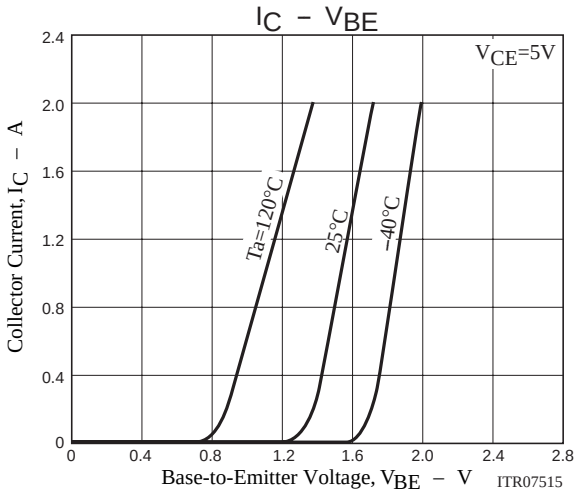
Switching Time Test Circuit

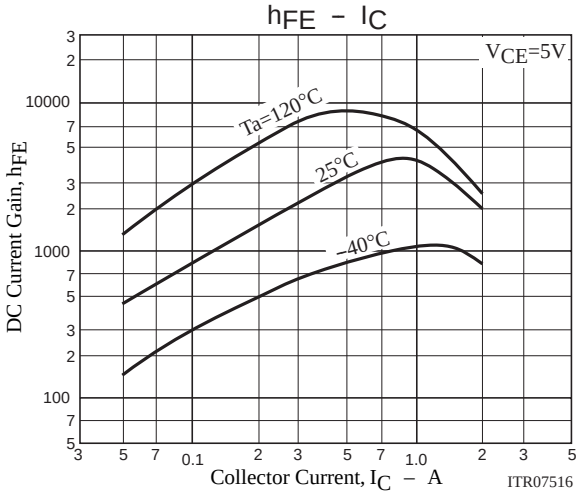


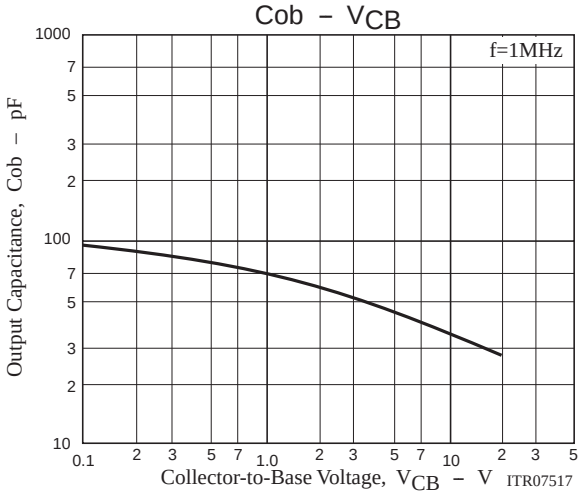
Es/b Test Circuit



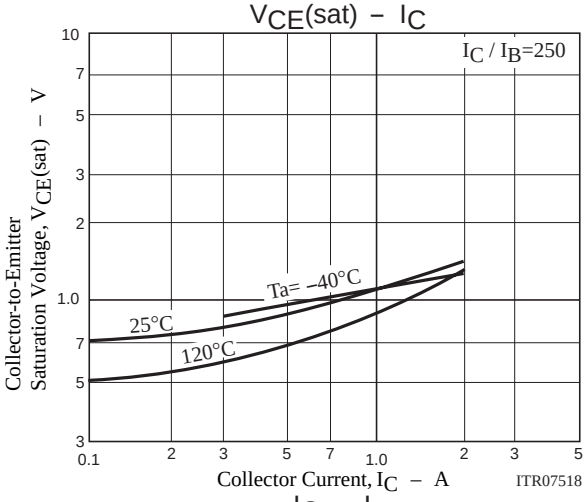




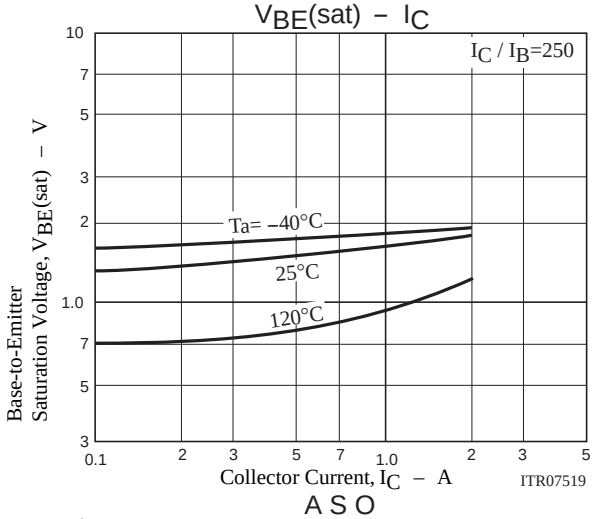




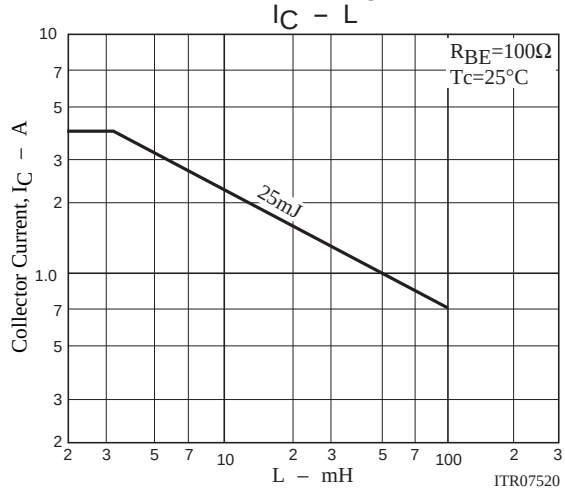
$V_{CE}(sat)$ – I_C



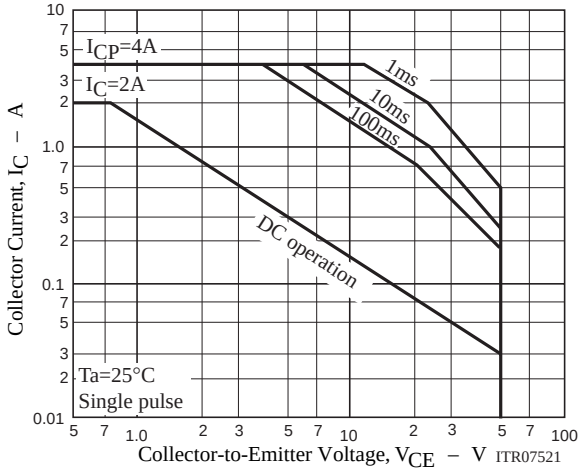
$V_{BE}(sat)$ – I_C



I_C – L



A S O



P_C – Ta