NEC Electronics Inc.

ANALOG MASTER BIPOLAR LINEAR ARRAYS CHS, V-CHS, M-CHS Series

March 1993

Description

NEC's Analog Master families (CHS, V-CHS, M-CHS Series) are bipolar linear arrays for developing analog circuits operating up to radio frequencies (RF). Analog Masters allow integrating numerous analog functions onto a single chip. This is accomplished by means of connecting up, in series or parallel, arrays of NPN/PNP transistors, on-chip resistors and MOS capacitors to form useful analog functions. These ASIC circuits are ideal for applications in multimedia, telecommunications or test and measurement where low power, compact and high speed circuits are desired.

Analog Master products are fully supported by NEC's advanced ASIC design technology. Various dedicated design and development tools and services available fof designing these circuits. The CHS, V-CHS, M-CHS libraries provide various and commonly used analog functions at various power and drive levels.

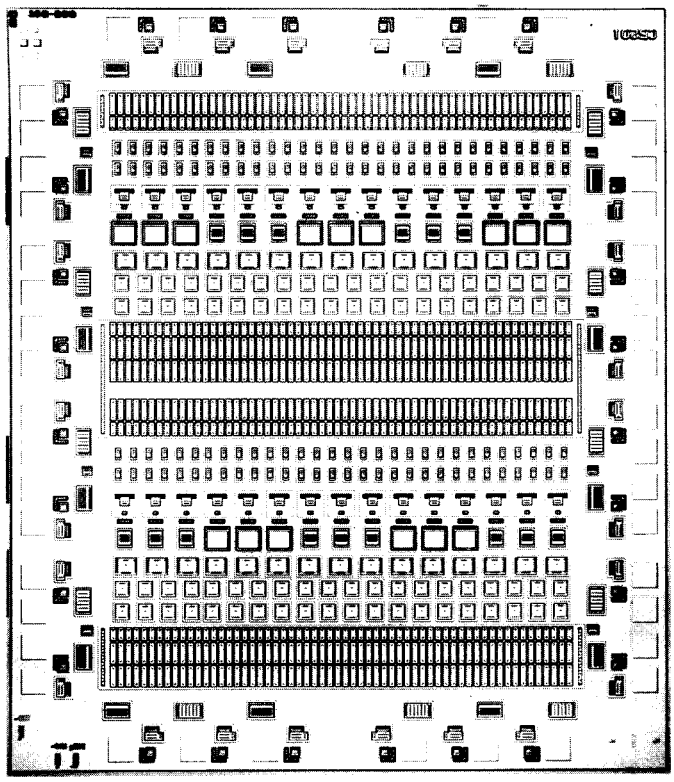
Features

- Analog signal processing up to RF frequencies
- High frequency operations:
  f_T up to 7 GHz for NPN transistors;
  f_T up to 1 GHz for PNP transistors (V-CHS)
- Excellent h_{FE} characteristics
- High frequency bipolar process technology
- On-chip polysilicon resistors and low parasitic capacitances
- Powerful block library of analog functions
- High voltage operation up to 44V (M-CHS)
- DIP, S-DIP, SOP and QFP packages available
- Hardware simulation using TEG (Test Element Group) basic blocks

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CHS, V-CHS and M-CHS Analog Master families. Additional design information is available in the CHS Block Library (TBD) and Design Manual (Doc. No. 70162); V-CHS Design Manual (Doc. No. 70135); and M-CHS Block Library (TBD) and Design Manual (Doc. No. 70164). Contact your local NEC Design Center or the NEC Literature Center for further Analog Master design information; see the back of this data sheet for locations and phone numbers.

Figure 1. Typical Analog Master Die



Analog Master Sizes

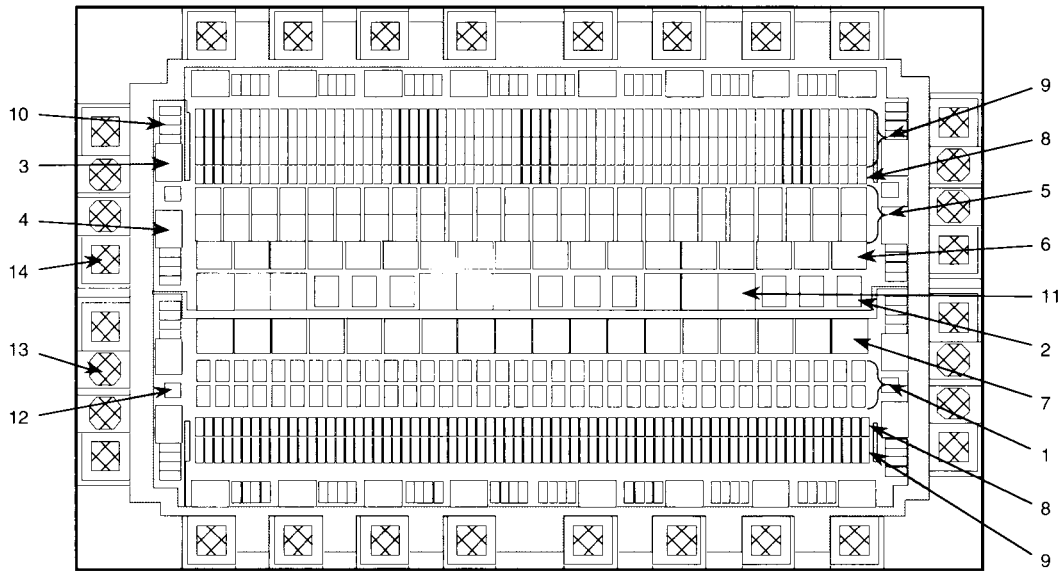
Device (μPC)	Total Elements	Maximum Available* Transistors	Resistors	Capacitors	I/O Pads (Max.)
CHS Devices					
5020	1628	484	1116	28	28
5021	2328	688	1600	40	32
5022	3042	892	2098	52	50
5023	727	245	468	14	22
5024	6152	1508	4560	84	80
V-CHS Devices					
5102	1367	251	1090	26	24
M-CHS Devices					
5200	658	189	456	9	24
5201	1038	303	712	15	28
5202	1799	535	1225	27	40
5203	3104	932	2108	48	52
5204	4578	1382	3108	72	62

*An Analog Master circuit should be designed so that no more than 70% of the elements are used. Even with 70% usage, routing may not be able to be completed, depending on the layout of the chip and the number of pin-pairs used.

Circuit Architecture

Analog Master products are built with NEC's high frequency, precision bipolar process technology. As shown in figure 2, bipolar array master chips are divided into pad and internal areas. The pad area contains pads and protection circuits that isolate the internal elements from high-energy external signals. The internal area is an array of pre-diffused basic elements, NPN transistors, PNP transistors, resistors and capacitors. The circuit is configured by connecting desired elements together with automated CAD tools, using a design flow similar to gate arrays.

Figure 2. Analog Master Chip with Major Elements Defined



1	NPN transistor	(HDT1)
2	NPN transistor	(HTW4)
3	NPN transistor	(HEW4)
4	NPN transistor	(HTT5)
5	Lateral PNP transistor	(HLP2)
6	Lateral PNP transistor	(HLP2A)
7	Vertical PNP transistor	(HVP3)
8	P^+ resistor	(500 Ω)
9	P^- resistor	(10 kΩ)
10	Polysilicon resistor	(500 Ω)
11	MOS capacitor	(5 pF)
12	Zener zap diode for trimming	
13	Pads for trimming	
14	Bonding pads	

83FM-9321B

Absolute Maximum Ratings

Parameters	Symbol	Ratings	Unit	Family
Supply voltage	V_{cc}	14	V	CHS
		44	V	M-CHS
		11	V	V-CHS
Operating temperature	T_{OPT}	-30 to +85	°C	
Storage temperature	T_{STG}	-55 to +125	°C	

Capacitor Characteristics

Family	Unit Capacitor	Absolute Accuracy	Relative* Accuracy
CHS	5 pF	±15%	±2%
V-CHS	5 pF	±15%	±2%
M-CHS	5 pF	±15%	±2%

*In close juxtaposition

Resistor Characteristics

Family	Unit Resistor	Resistor Type	Absolute Accuracy	Relative* Accuracy
CHS	500	ion-injected	±15%	±2%
	5K	ion-injected	±15%	±2%
	2.5k	ion-injected	±20%	±3%
	3k	ion-injected	±20%	±3%
V-CHS	500	ion-injected	±15%	±2%
	5k	ion-injected	±15%	±2%
	200	ion-injected	±20%	±3%
	1k	ion-injected	±20%	±3%
M-CHS	500	ion-injected	±15%	±2%
	10k	ion-injected	±15%	±2%
	500	ion-injected	±20%	±3%

*In close juxtaposition

Analog Master CHS Family

Table 1 Product Outline

CHS Master Slice			μPC5020	μPC5021	μPC5022	μPC5023	μPC5024	Conditions
Process			High Frequency Bipolar					CHS-process
Max Supply Voltage			14V					
Number of Pads			28	32	50	22	80	
Total Number of Elements			1628	2328	3042	727	6125	
	Transistor Elements		484	688	892	245	1508	
	NPN Type	CHT1	224	320	416	112	672	I_C max. = 2 mA*
		CTW4	28	40	52	13	84	I_C max. = 18 mA
		CEW4	8	8	8	4	80	I_C max. = 18 mA
	PNP Type	CLP1	168	240	312	84	504	I_C max. = 0.05 mA, lateral
		CVP1	56	80	104	32	168	I_C max. = 0.5 mA, vertical
	Number of Resistors		1116	1600	2098	468	4560	
	Ohmic value	500 ohms	544	784	1024	224	1664	Ion-injected resistor (P^+)
		5k ohms	544	784	1024	200	2496	Ion-injected resistor (P^-)
		2.5k ohms	28	32	50	–	–	Polysilicon resistor
		3k ohms	–	–	–	44	400	Polysilicon resistor
	Capacitors (5 pF)		28	40	52	14	84	MOS Capacitor

*$I_{C\,MAX}$: Collector current value at which the DC amplification factor (h_{FE}) drops 30% from the peak

Table 2 Typical CHS Transistor Electrical Characteristics

Parameter		Symbol	NPN Transistors			PNP Transistors		Conditions
			CHT1	CTW4	CEW4	CLP1	CVP1	T_A = 25°C
Absolute Maximum Ratings	Collector-Base Voltage	V_{CBO}	25 V	25 V	25 V	–25 V	–25 V	
	Collector-Emitter Voltage	V_{CEO}	14 V	14 V	14 V	–14 V	–14 V	
	Emitter-Base Voltage	V_{EBO}	3 V	2 V	2 V	–25 V	–6 V	
	Collector Current	I_C	4 mA	18 mA	18 mA	–4 mA	–1 mA	
Electrical Characteristics	DC Amplification Factor	h_{FE}	100	100	100	250	75	NPN: I_C = 500 μA PNP: I_C = 10 μA
	Collector Current	I_{CMAX}	2 mA	18 mA	18 mA	–50 μA	–0.5 mA	h_{FE} is 30 % down
	Gain Bandwidth Product	f_T	4.5 GHz	6 GHz	6 GHz	7 MHz	280 MHz	V_{CE} = 3.0 V
	DC Emitter-Base Voltage	V_{BE}	0.81 V	0.75 V	0.71 V	–0.66 V	–0.69 V	NPN: I_C = 500 μA PNP: I_C = 10 μA
	Input Voltage Noise (nV / $\sqrt{Hz}$)	e_N	3.1	1.9	2.4	5.5	6.0	NPN: I_C = 100 μA PNP: I_C = 10 μA
			2.8	0.95	2.4	3.1	3.2	NPN: I_C = 1 mA PNP: I_C = 50 μA
	Input Current Noise (pA / $\sqrt{Hz}$)	i_N	0.67	0.63	0.45	0.2	0.26	NPN: I_C = 100 μA PNP: I_C = 10 μA
			2.8	2.0	2.0	0.9	1.0	NPN: I_C = 1 mA PNP: I_C = 50 μA

Analog Master V-CHS Family

Table 3 Product Outline

V-CHS Master Slice			μPC5102				Conditions
Process			High Frequency Bipolar				V-CHS
Max Supply Voltage			11V				
Number of Pads			24				
Configuration			Total	Blocks			
				High Freq.	Power	Other Types	
Elements			1367	218 x 5	251	26	
Transistors			251	38 x 5	61		
	NPN	FDT2	115	17 X 5	30		I_C max. = 1.6 mA[Note 1]
		FDT4	30	6 X 5	0		I_C max. = 3.2 mA
		FTT4	37	6 X 5	7		I_C max. = 6.4 mA
		FEW5	4	0	4		I_C max. = 18 mA[Note 2]
	PNP	FLP1	20	0	20		I_C max. = 32 μA, lateral
		FVP1	45	9 X 5	0		I_C max. = 1.0 mA, vertical
Resistors			1090	180 X 5	190		
	500 ohms		200	28 X 5	60		Ion-injected resistor (P^+)
	5 k ohms		330	42 X 5	120		Ion-injected resistor (P^-)
	200 ohms		360	70 X 5	10		Polysilicon resistor
	1 k ohms		200	40 x 5	0		Polysilicon resistor
Capacitors (5 pF)			26	0	0	26	MOS Capacitor

Notes: 1. $I_{C\,MAX}$: Collector current value at which the DC amplification factor (h_{FE}) drops 30% from the peak
2. In addition to these transistors, two diodes are also connected near each bonding pad for absorbing static electricity

Table 4 Typical V-CHS Transistor Electrical Characteristics

Parameter		Symbol	NPN Transistors				PNP Transistors		Conditions
			FDT2	FDT4	FTT4	FEW5	FLP1	FVP1	T_A = 25°C
Absolute Maximum Ratings	Collector-Base Voltage	V_{CBO}	20 V	20 V	20 V	20 V	–20 V	–20 V	
	Collector-Emitter Voltage	V_{CEO}	11 V	11 V	11 V	11 V	–11 V	–11 V	
	Emitter-Base Voltage	V_{EBO}	2.5 V	2.5 V	2 V	2 V	–22 V	–8 V	
	Collector Current	I_C	3.2mA	3.2mA	6.4mA	18mA	–3.2mA	–1.5mA	
Electrical Characteristics	DC Amplification Factor	h_{FE}	100	100	100	100	100	50	NPN: I_C = 500 μA PNP: I_C = 1 μA (FLP1) I_C = 10 μA (FVP1)
	Collector Current	I_{CMAX}	1.6mA	3.2mA	6.4mA	18mA	–32mA	–1.0mA	h_{FE} is 30 % down
	Gain Bandwidth Product	f_T	6 GHz	7 GHz	6.5 GHz	6.5 GHz	7 MHz	1 GHz	V_{CE} = 3.0 V
	DC Emitter-Base Voltage	V_{BE}	0.82 V	0.78 V	0.76 V	0.76 V	–0.67 V	–0.68 V	NPN: I_C = 500 μA PNP: I_C = 10 μA
	Input Voltage Noise ($nV/\sqrt{Hz}$)	e_N	2.0	1.8	1.6	2.1	5.0	5.0	NPN: I_C = 100 μA PNP: I_C = 10 μA
			1.8	0.95	0.8	1.7	3.3	3.0	NPN: I_C = 1 mA PNP: I_C = 50 μA
	Input Current Noise ($pA/\sqrt{Hz}$)	i_N	0.55	0.55	0.55	0.55	0.21	0.33	NPN: I_C = 100 μA PNP: I_C = 10 μA
			2.5	2.5	2.5	2.5	0.8	1.2	NPN: I_C = 1 mA PNP: I_C = 50 μA

Analog Master M-CHS Family

Table 5 Product Outline

M-CHS Master Slice			μPC5200	μPC5201	μPC5202	μPC5203	μPC5204	Conditions
Process			High Frequency, High Breakdown Bipolar					M-CHS-process
Max Supply Voltage			44V					
Number of Pads			24	28	40	52	62	
Total Number of Elements			658	1038	1799	3104	4578	
	Transistor Elements		189	303	535	932	1382	
	NPN Type	HDT1	72	120	216	384	576	I_C max. = 1 mA*
		HTW4	9	15	27	48	72	I_C max. = 10 mA
		HEW4	12	14	20	26	31	I_C max. = 10 mA
		HTT5	12	14	20	26	31	I_C max. = 18 mA
	PNP Type	HLP2	48	80	144	256	384	I_C max. = 0.12 mA
		HLP2A	18	30	54	96	144	I_C max. = 0.12 mA
		HVP3	18	30	54	96	144	I_C max. = 0.12 mA
	Number of Resistors		456	712	1225	2108	3108	
	Ohmic value	500 ohms	144	240	426	760	1144	Ion-injected resistor (P^+)
		10k ohms	216	360	639	1140	1716	Ion-injected resistor (P^-)
		500 ohms	91	112	160	208	248	Polysilicon resistor
	Capacitors (5 pF)		9	15	27	48	72	MOS Capacitor
	Trimming (Zap) diodes		4	8	12	16	16	Zener diodes

*$I_{C\ MAX}$: Collector current value at which the DC amplification factor (h_{FE}) drops 30% from the peak

Table 6 Typical M-CHS Transistor Electrical Characteristics

Parameter		Symbol	NPN Transistors				PNP Transistors			Conditions
			HDT1	HDW4	HEW4	HTT5	HLP2	HLP2A	HVP3	T_A = 25°C
Absolute Maximum Ratings	Collector-Base Voltage	V_{CBO}	44 V	44 V	44 V	44 V	−44 V	−44 V	−44 V	
	Collector-Emitter Voltage	V_{CEO}	44 V	44 V	44 V	44 V	−44 V	−44 V	−44 V	
	Emitter-Base Voltage	V_{EBO}	5 V	5 V	5 V	5 V	−16.5 V	−16.5 V	−16.5 V	
	Collector Current	I_C	4 mA	18 mA	18 mA	18 mA	−1 mA	−1 mA	−1 mA	
Electrical Characteristics	DC Amplification Factor	$h_{FE\ (MIN)}$ $h_{F(TYP)}$ $h_{FE(MAX)}$	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	50 100 200	NPN: I_C = 500 μA PNP: I_C = 10 μA
	Collector Current	I_{CMAX}	1 mA	10 mA	10 mA	18 mA	−0.12mA	−0.12mA	−1mA	h_{FE} is 30 % down
	Gain Bandwidth Product	f_T	2 GHz	2 GHz	2 GHz	2 GHz	2 MHz	2 MHz	50 MHz	V_{CE} = 3.0 V
	DC Emitter-Base Voltage	V_{BE} V_{BE} V_{BE}	0.74 V 0.76 V 0.78 V	0.67 V 0.69 V 0.71 V	0.67 V 0.69 V 0.71 V	0.65 V 0.67 V 0.69 V	0.67 V 0.69 V 0.71 V	0.67 V 0.69 V 0.71 V	0.64 V 0.66 V 0.68 V	NPN: I_C = 100 μA PNP: I_C = 10 μA
	Input Voltage Noise (nV / √Hz)	e_N	3.8	1.6	2.2	1.5	5	5	5	NPN: I_C = 100 μA PNP: I_C = 10 μA
			3.8	1.2	2.0	1.0	3.4	2.2	2.7	NPN: I_C = 1 mA PNP: I_C = 50 μA
	Input Current Noise (pA / √Hz)	i_N	0.7	0.5	0.6	0.5	0.26	0.26	0.3	NPN: I_C = 100 μA PNP: I_C = 10 μA
			3.8	1.8	2.0	2.3	0.7	0.7	0.7	NPN: I_C = 1 mA PNP: I_C = 50 μA

Package Plan

Analog Master Family		CHS					V-CHS	M-CHS				
	μPCxxxx	-5020	-5021	-5022	-5023	-5024	-5102	-5200	-5201	-5202	-5203	-5204
Dual in Line (DIP)												
8-pin	(300 mil)	A	A	–	A	–	A	A	–	–	–	–
14-pin	(300 mil)	–	–	–	A	–	A	A	–	–	–	–
16-pin	(300 mil)	–	–	–	A	–	A	A	–	–	–	–
18-pin	(300 mil)	–	–	–	A	–	A	A	–	–	–	–
22-pin	(400 mil)	–	–	A	–	–	–	A	A	A	–	–
24-pin	(600 mil)	–	–	–	–	–	–	–	A	–	A	–
28-pin	(600 mil)	–	–	–	–	–	–	–	–	A	–	–
42-pin	(600 mil)	–	–	–	–	–	–	–	A	–	A	A
Dual in Line (S-DIP)												
14-pin	(300 mil)	A	A	–	–	–	–	A	–	–	–	–
18-pin	(300 mil)	A	A	–	A	–	–	–	–	–	–	–
20-pin	(300 mil)	–	–	–	A	–	A	A	–	–	–	–
22-pin	(300 mil)	–	A	–	A	–	A	–	–	–	–	–
24-pin	(300 mil)	A	A	–	–	–	–	–	–	–	–	–
24-pin	(400 mil)	–	–	–	–	–	–	A	A	–	–	–
28-pin	(400 mil)	–	A	A	–	–	–	–	–	A	A	–
30-pin	(400 mil)	–	A	A	–	–	–	–	–	A	–	–
42-pin	(600 mil)	–	–	A	–	–	–	–	A	A	–	A
48-pin	(600 mil)	–	–	–	–	A	–	–	–	–	A	A
Small Outline Package (SOP)												
8-pin	(225 mil)	–	–	–	A	–	–	–	–	–	–	–
8-pin	(300 mil)	–	–	–	–	–	A	–	–	–	–	–
14-pin	(225 mil)	–	–	–	A	–	–	–	–	–	–	–
16-pin	(225 mil)	–	–	–	A	–	–	–	–	–	–	–
16-pin	(300 mil)	A	–	–	–	–	A	A	–	–	–	–
16-pin	(375 mil)	–	A	–	–	–	–	–	–	–	–	–
20-pin	(300 mil)	A	A	–	A	–	A	A	–	–	–	–
24-pin	(300 mil)	A	A	–	A	–	A	A	A	–	–	–
24-pin	(375 mil)	–	–	A	–	–	–	–	–	A	–	–
28-pin	(375 mil)	A	A	A	–	–	–	–	A	A	–	–
Small Outline Package (S-SOP)												
14-pin	(225 mil)	–	–	–	A	–	A	–	–	–	–	–
16-pin	(225 mil)	–	–	–	A	–	A	–	–	–	–	–
20-pin	(300 mil)	A	–	–	–	–	A	A	E	–	–	–
24-pin	(300 mil)	–	–	–	–	–	–	E	E	–	–	–
36-pin	(300 mil)	A	–	–	–	–	A	A	–	–	–	–
Quad Flat Pack												
48-pin	(7 x 7)	–	A	A	–	–	–	–	A	–	–	–
48-pin	(10 x 14)	–	–	A	–	A	–	A	–	–	A	–
48-pin	(10 x 10)	–	–	A	–	–	–	–	–	A	–	–
64-pin	(14 x 20)	–	–	–	–	–	–	–	–	–	A	–
68-pin	(10 x 14)	–	–	–	–	A	–	–	–	–	–	–
80-pin	(14 x 20)	–	–	–	–	A	–	–	–	–	–	–
80-pin	(14 x 14)	–	–	–	–	–	–	–	–	–	–	A

A = Available; "–" = Unavailable; E = under consideration or evaluation

NOTE: NEC reserves the right to alter the package plan based on the results of qualification.
For current package availability, please contact your local NEC Design Center.

NEC's Analog Master Design System

Analog Master bipolar arrays are fully supported by NEC's network of ASIC Design Centers, listed on the back of this data sheet.

Design flow for CHS, V-CHS, and M-CHS ASIC products is shown in figure 4. Users can enlist Design Center support at any step in the design flow before actual manufacturing. The first step is to create the block diagram of a circuit. Next, each block at the element level is designed. A package then must be selected at this stage.

Other considerations in the design are DC, AC transient analysis, analysis of element characteristics for temperature and variation of supply voltage, and dealing with static electric destruction. This is followed by determining the pinouts on the chip and the package selected.

NEC supports its ASIC products with a comprehensive CAD system, described below in Table 8, that significantly reduces the time and expense usually associated with the development of semi-custom analog devices. The system supports schematic entry, simulation, and advanced place-and-route algorithms. These advanced CAD tools ensure accurate designs.

Sample design kits are available at no charge to qualified users: contact an NEC ASIC Design Center for more information. (Software licensing required—NEC reserves the right to prioritize support based on user requirements.)

Figure 4. Analog Workbench Design Flow

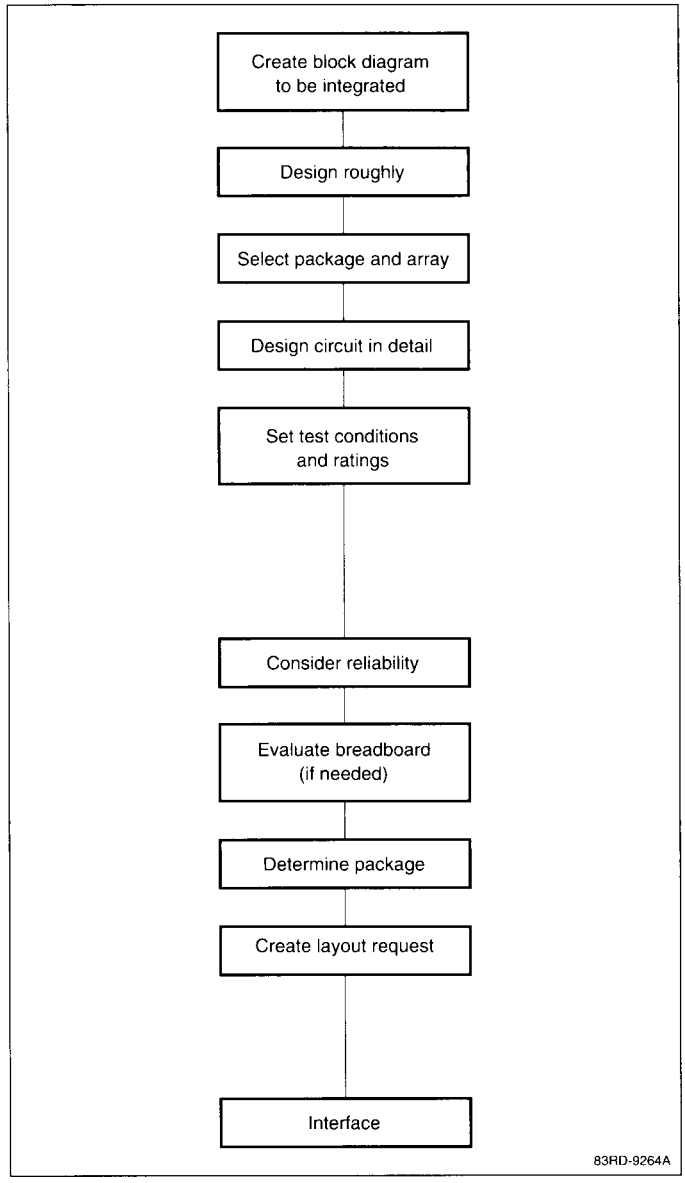


Table 8 Analog Master Design Tools

Hardware / Software	Vendor	Cadence	Zuken	Viewlogic	Micro Sim.	OrCAD	Mentor	Media		
Vendor	Product	AWBIIc	CR-3000/ AWS*	Workview	PSPICE	OrCAD/* SDT III	IDEA Station (MSPICE)	1/4 in. Cartridge	3.5 in. FD	5 in. FD
NEC	EWS4800	—	√	—		—	—	—	√	—
	PC9801	—	—	√		√	—	—	√	—
SUN Microsystems	SUN3/SUN4	√	—	—		—	—	√	√	—
	SPARC	√	√	—		—	—	√	√	—
IBM	PC/XT or /AT	—	—	√		—	—	—	√	√
HP	HP9000 300/400	√	√	—		—	—	√	—	—
	DN3000/4000	—	—	—		—	√	√	—	√
	HP-Apollo-400	—	—	—		—	√	√	—	—

*This is to be used with the software entitled Analog Master Developing Support Software.

Block Library List

The Analog Master families offer a variety of analog macros, such as operational amplifiers, comparators, voltage regulators and switches to build analog functions.

Macro Library (CHS)

Block List

Macro Name	Description
Operational Amplifiers	
OA01A	General Purpose operational amplifier
OA02	Single supply operational amplifier
OA03A	Micro-power operational amplifier
OA04A	High impedance input Op Amp
OA05	High speed, wide bandwidth, Op Amp
OA06A/-06B	Single supply operational amplifier
OA07A/-07B	High speed operational amplifier
Comparators	
CP01	Single supply comparator
CP02	High speed comparator
Regulators	
RG01A	Voltage regulator (1.3 - 9V)
RG02A	Voltage regulator (2.5 - 9.5V)
Switches	
SW01A	Bi-directional switch (Active- high)
SW01B	Bi-directional switch (Active-low)
ECL	
EL01	ECL OR
EL02	ECL NOR
Filters	
FL01 – 04	Audio filter (400 Hz f_C 200 kHz)
FL05 – 08	Video filter (200 kHz f_C 5 MHz)

Macro Library (M-CHS)

Block List

Macro Name	Description
Operational Amplifiers	
OA201	General Purpose operational amplifier
OA202	Single supply operational amplifier
OA203	Micro-power operational amplifier
OA206	Low noise operational amplifier
Comparators	
CP201	Single supply comparator
CP202	High speed comparator
Regulators	
RG201	Voltage regulator (1.3 - 36V)
RG202	High accuracy voltage regulator (5V ± 2.5%)
Switches	
SW201A	Bi-directional switch (H-active)
SW201B	Bi-directional switch (L-active)

NEC ASIC DESIGN CENTERS

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