Data Sheet, V1.3, Dec. 2000

C505CA-4RC Step BB

8-bit Single-Chip Microcontroller (Bare Die Delivery)

Microcontrollers

Infineon technologies

Never stop thinking.

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Revision History:	**2000-12**	V1.3
Previous Version:	V1.2, V1.1	

Page	Subjects (major changes since last revision)
14	Reference of Data Sheet version is updated

Controller Area Network (CAN): License of Robert Bosch GmbH

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Advance Information

- Fully compatible to standard 8051 microcontroller
- Superset of the 8051 architecture with 8 datapointers
- Up to 20 MHz operating frequency
  - 375 ns instruction cycle time @16 MHz
  - 300 ns instruction cycle time @20 MHz (50% duty cycle)
- On-chip program memory (with optional memory protection)
  - 32K byte on-chip Mask ROM
  - alternatively up to 64k byte external program memory
- 256 byte on-chip RAM
- 1K byte On-chip XRAM

(more features on next page)

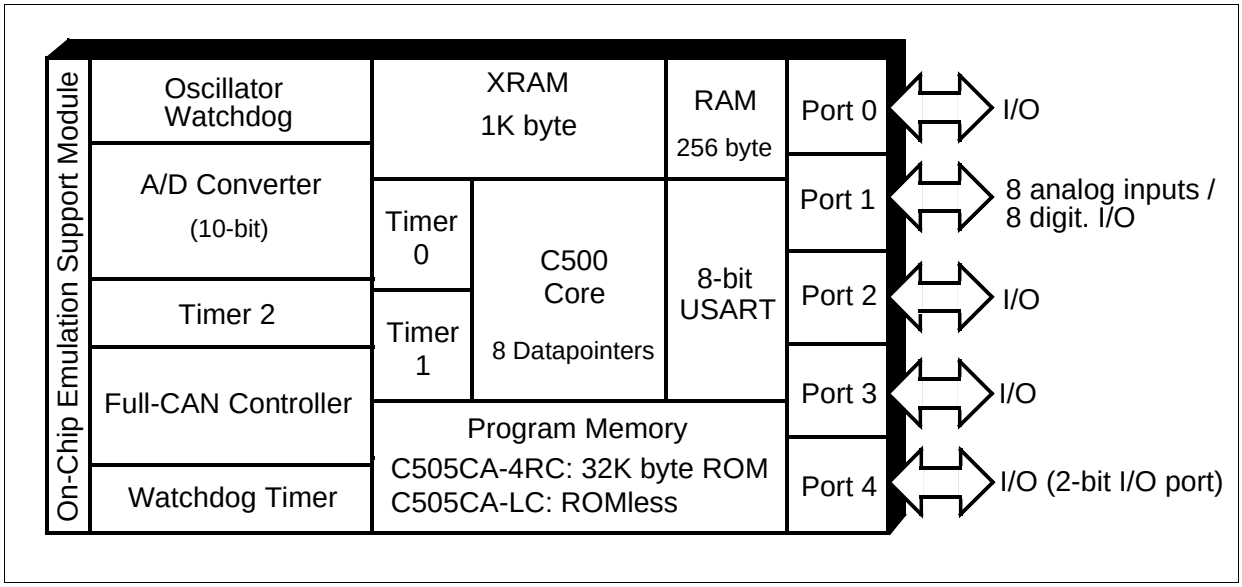

Figure 1 C505CA-4RC Functional Units

Features(continued) :

- 32 + 2 digital I/O lines
  - Four 8-bit digital I/O ports
  - One 2-bit digital I/O port (port 4)
  - Port 1 with mixed analog/digital I/O capability
- Three 16-bit timers/counters
  - Timer 0 / 1 (C501 compatible)
  - Timer 2 with 4 channels for 16-bit capture/compare operation
- Full duplex serial interface with programmable baudrate generator (USART)
- Full CAN Module, version 2.0 B compliant
  - 256 register/data bytes located in external data memory area
  - 1 MBaud CAN baudrate when operating frequency is equal to or above 8 MHz
  - internal CAN clock prescaler when input frequency is over 10 MHz
- On-chip A/D Converter
  - up to 8 analog inputs
  - 10-bit resolution
- Twelve interrupt sources with four priority levels
- On-chip emulation support logic (Enhanced Hooks Technology ™[1])
- Programmable 15-bit watchdog timer
- Oscillator watchdog
- Fast power on reset
- Power Saving Modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake up capability through P3.2/$\overline{\text{INT0}}$ or P4.1/ RXDC pin
- Temperature ranges:

SAB-C505 versions	T_D = 0 to 70 °C
SAF-C505 versions	T_D = -40 to 85 °C
SAK-C505 versions	T_D = -40 to 125 °C
SAA-C505 versions	T_D = -40 to 150 °C

[1] "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

Ordering Information

Table 1 Bare Die Ordering Information

Type	Ordering Code	Wafers	Comments
SAK-C505CA-LC	TBD	Whole/Sawn	8-bit microcontroller with Temperature range: -40 °C to +125 °C (max. operating frequency: 20 MHz with 50% duty cycle)
SAA-C505CA-LC	TBD	Whole/Sawn	8-bit microcontroller with Temperature range: -40 °C to +150 °C (max. operating frequency: 20 MHz with 50% duty cycle)
SAK-C505CA-4RC	TBD	Whole/Sawn	8-bit microcontroller with 32K bytes ROM Temperature range: -40 °C to +125 °C (max. operating frequency: 20 MHz with 50% duty cycle)
SAA-C505CA-4RC	TBD	Whole/Sawn	8-bit microcontroller with 32K bytes ROM Temperature range: -40 °C to +150 °C (max. operating frequency: 20 MHz with 50% duty cycle)

Note: The ordering codes for the Mask-ROM versions (DXXXX extension) are defined for each product after verification of the respective ROM code.

Note: Versions for the temperature range 0 °C to 70 °C (SAB-C505) and -40 °C to 85 °C (SAF-C505) are available on request.

Introduction

The C505CA-xC derivatives, which refer to C505CA-4RC and C505CA-LC in this document, are high performance derivatives of the Infineon C500 family of 8-bit microcontrollers. The C505CA-xC derivatives are fully compatible to the standard 8051 microcontroller. Additionally the C505CA-xC provides extended power save provisions, on-chip RAM, 1K byte XRAM, on-chip ROM, 10-bit A/D converter, and RFI related improvements.

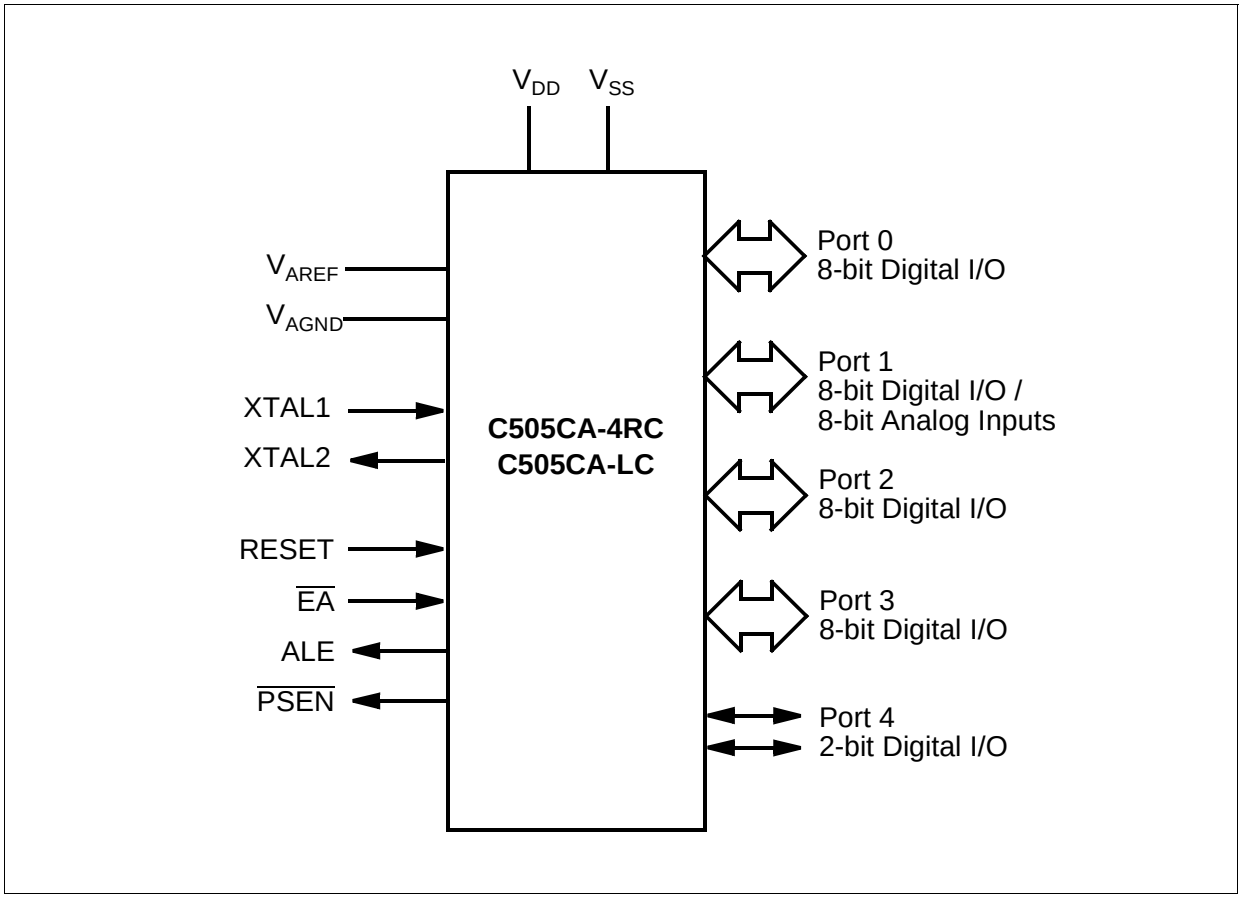

Figure 2 Logic Symbol

Pad Configuration

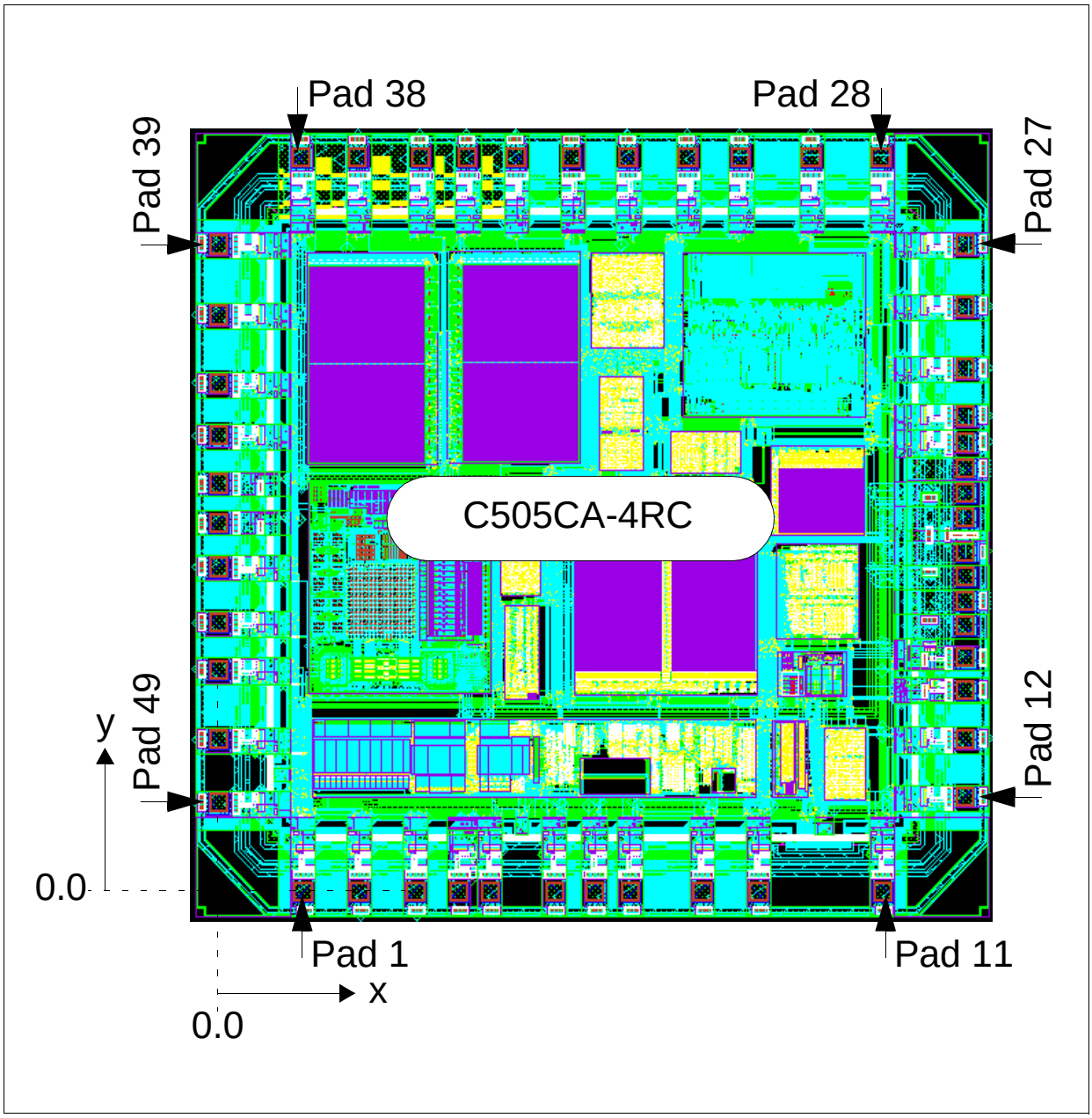

Figure 3 C505CA-4RC Pad Configuration (Top View)

Table 2 Pad Definition and Functions

Symbol	Pad Num.	In/ Out (I/O)	Position [µm]		Function
			x	y	
P1.5	1	I/O	453	0	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 5 / Timer 2 external reload / trigger input
P1.6	2	I/O	753	0	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 6 / system clock output
P1.7	3	I/O	1053	0	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 7 / counter 2 input
RESET	4	I	1284	0	RESET input
P3.0	5	I/O	1451	0	Port 3 general Input/Output (quasi-bidirectional)/ Receiver data input (asynch.) or data input/ output (synch.) of serial interface
P4.0	6	I/O	1796	0	Port 4 general Input/Output (quasi-bidirectional)/ Transmitter output of CAN controller
P3.1	7	I/O	2012	0	Port 3 general Input/Output (quasi-bidirectional)/ Transmitter data output (asynch.) or clock output (synch.) of serial interface
P3.2	8	I/O	2201	0	Port 3 general Input/Output (quasi-bidirectional)/ External interrupt 0 input / timer 0 gate control input
P3.3	9	I/O	2586	0	Port 3 general Input/Output (quasi-bidirectional)/ External interrupt 1 input / timer 1 gate control input
P3.4	10	I/O	2886	0	Port 3 general Input/Output (quasi-bidirectional)/ Timer 0 counter input
P3.5	11	I/O	3547	0	Port 3 general Input/Output (quasi-bidirectional)/ Timer 1 counter input
P3.6	12	I/O	3991	484	Port 3 general Input/Output (quasi-bidirectional)/ $\overline{WR}$ control output
P3.7	13	I/O	3991	778	Port 3 general Input/Output (quasi-bidirectional)/ $\overline{RD}$ control output
XTAL2	14	O	3991	1028	Output of the inverting oscillator amplifier.

Table 2 Pad Definition and Functions

Symbol	Pad Num.	In/ Out (I/O)	Position [µm]		Function
			x	y	
XTAL1	15	I	3991	1193	Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
NC	16	-	3991	1355	Not connected
V_{SS}	17	-	3991	1480	Ground (0V)
V_{SS}	18	-	3991	1605	Ground (0V)
V_{SS}	19	-	3991	1730	Ground (0V)
V_{DD}	20	-	3991	1904	Power Supply (+5V)
V_{DD}	21	-	3991	2029	Power Supply (+5V)
V_{DD}	22	-	3991	2155	Power Supply (+5V)
P2.0	23	I/O	3991	2289	Port 2 general Input/Output (quasi-bidirectional)/ High-order address byte line A8
P2.1	24	I/O	3991	2423	Port 2 general Input/Output (quasi-bidirectional)/ High-order address byte line A9
P2.2	25	I/O	3991	2664	Port 2 general Input/Output (quasi-bidirectional)/ High-order address byte line A10
P2.3	26	I/O	3991	2980	Port 2 general Input/Output (quasi-bidirectional)/ High-order address byte line A11
P2.4	27	I/O	3991	3295	Port 2 Input/Output (quasi-bidirectional)/ High-order address byte line A12
P2.5	28	I/O	3537	3739	Port 2 general Input/Output (quasi-bidirectional)/ High-order address byte line A13
P2.6	29	I/O	3165	3739	Port 2 general nput/Output (quasi-bidirectional)/ High-order address byte line A14
P2.7	30	I/O	2785	3739	Port 2 general Input/Output (quasi-bidirectional)/ High-order address byte line A15
$\overline{PSEN}$	31	O	2505	3739	Program Store Enable
ALE	32	O	2186	3739	Address Latch Enable
P4.1	33	I/O	1886	3739	Port 4 general Input/Output (quasi-bidirectional)/ Receiver input of CAN controller
$\overline{EA}$	34	I	1588	3739	External Access Enable

Table 2 Pad Definition and Functions

Symbol	Pad Num.	In/ Out (I/O)	Position [µm]		Function
			x	y	
P0.7	35	I/O	1327	3739	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A7/D7
P0.6	36	I/O	1078	3739	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A6/D6
P0.5	37	I/O	744	3739	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A5/D5
P0.4	38	I/O	444	3739	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A4/D4
P0.3	39	I/O	0	3295	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A3/D3
P0.2	40	I/O	0	2936	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A2/D2
P0.1	41	I/O	0	2586	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A1/D1
P0.0	42	I/O	0	2322	Port 0 general Input/Output (open-drain)/ Multiplexed low-order address and data bus line A0/D0
V_{AREF}	43	-	0	2078	Reference voltage for the A/D converter.
V_{AGND}	44	-	0	1878	Reference ground for the A/D converter.
P1.0	45	I/O	0	1652	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 0 / interrupt 3 input / capture/compare channel 0 I/O
P1.1	46	I/O	0	1370	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 1 / interrupt 4 input / capture/compare channel 1 I/O

Table 2 Pad Definition and Functions

Symbol	Pad Num.	In/ Out (I/O)	Position [µm]		Function
			x	y	
P1.2	47	I/O	0	1129	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 2 / interrupt 5 input / capture/compare channel 2 I/O
P1.3	48	I/O	0	776	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 3 /interrupt 6 input / capture/compare channel 3 I/O
P1.4	49	I/O	0	453	Port 1 general Input/Output (quasi-bidirectional)/ Analog input channel 4

Note: All V_{SS} pads and all V_{DD} pads must be connected to the system ground and the power supply, respectively.
The pad definitions and locations in this table are only valid for the indicated device and design step.

Handling Of Unconnected Pads

Signal input stages may generate undesired switching noise and cross-current when left open. Respect the following precautions for unconnected (not bonded) pads:

Table 3 Precautions for Unconnected Pads

Pad Type	Recommended Action	Related Pads
Power Supply	Always connect!	V_{DD}, V_{SS}, V_{AREF}, V_{AGND}
Standard I/O pads(except P0)	Can be left	P1[1)], P2, P3, P4
Port 0	Set the corresponding pad latches to ’0’s	P0
Required control lines	Always connect!	RESET, XTAL1,$\overline{EA}$
Optional control lines	Can be left open	ALE, $\overline{PSEN}$, XTAL2

1) Avoid to set unconnected P1 pad as analog input if left open. However, P1 is set as digital I/O by default after reset.

Functional Description

As the standard packaged devices are made from this silicon the C505CA-xC dies provide exactly the same functionality and behaviour. Also the DC characteristics and AC characteristics are compatible with those of the packaged devices.

For a description of the functionality and the DC and AC parameters please refer to the following documents (or later versions thereof):

- C505/C505C/C505A/C505CA Data Sheet 2000-12
- C505/C505C User's Manual 08.97
- C505A/C505CA User's Manual 09.97 (Addendum to C505/C505C)

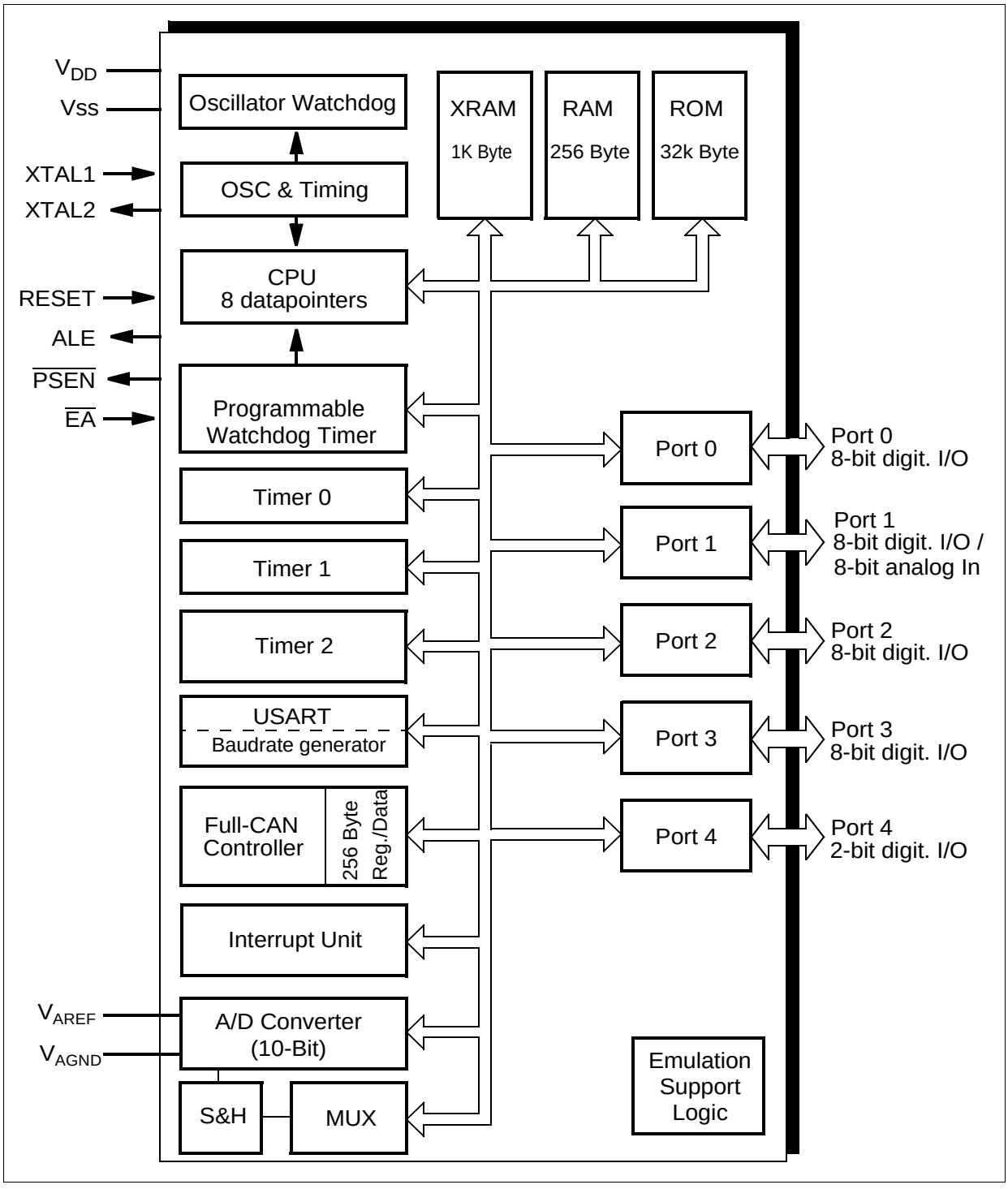

Figure 4 Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	– 65	150	°C	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	– 0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	– 0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition		– 10	10	mA	–
Absolute sum of all input currents during overload condition			| 100 mA |	mA	–
Power dissipation	P_{DISS}		1	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operatinon of the C505CA-xC. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.25	5.5	V	Active mode
		2	5.5	V	PowerDown mode
Ground voltage	V_{SS}	0		V	Reference voltage
Temperature of the bottom side of the die				°C	–
SAB-C505	T_D	0	70		
SAF-C505	T_D	-40	85		
SAK-C505	T_D	-40	125		
SAA-C505	T_D	-40	150		
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} – 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND} -0.2	V_{AREF} +0.2	V	–
XTAL clock	f_{osc}	2	20 (with 50% duty cycle)	MHz	–

Storage Conditions

The C505CA-xC dies may be stored for a certain time under the conditions described below.

Table 4 Bare Die Storage Conditions and Duration

Packing	Environment	Temperature	Rel. Humidity	Storage Time
Vacuum pack	Air	15...30 °C	< 60 %	< 4 Months

Power Supply Currents

The power supply currents for the bare die are compatible with those of the packaged devices with the following exceptions:

- The maximum Power down current (I_{PD}) for bare die is: $I_{PD\ MAX.}$ = 35 uA

Bare Die Outline

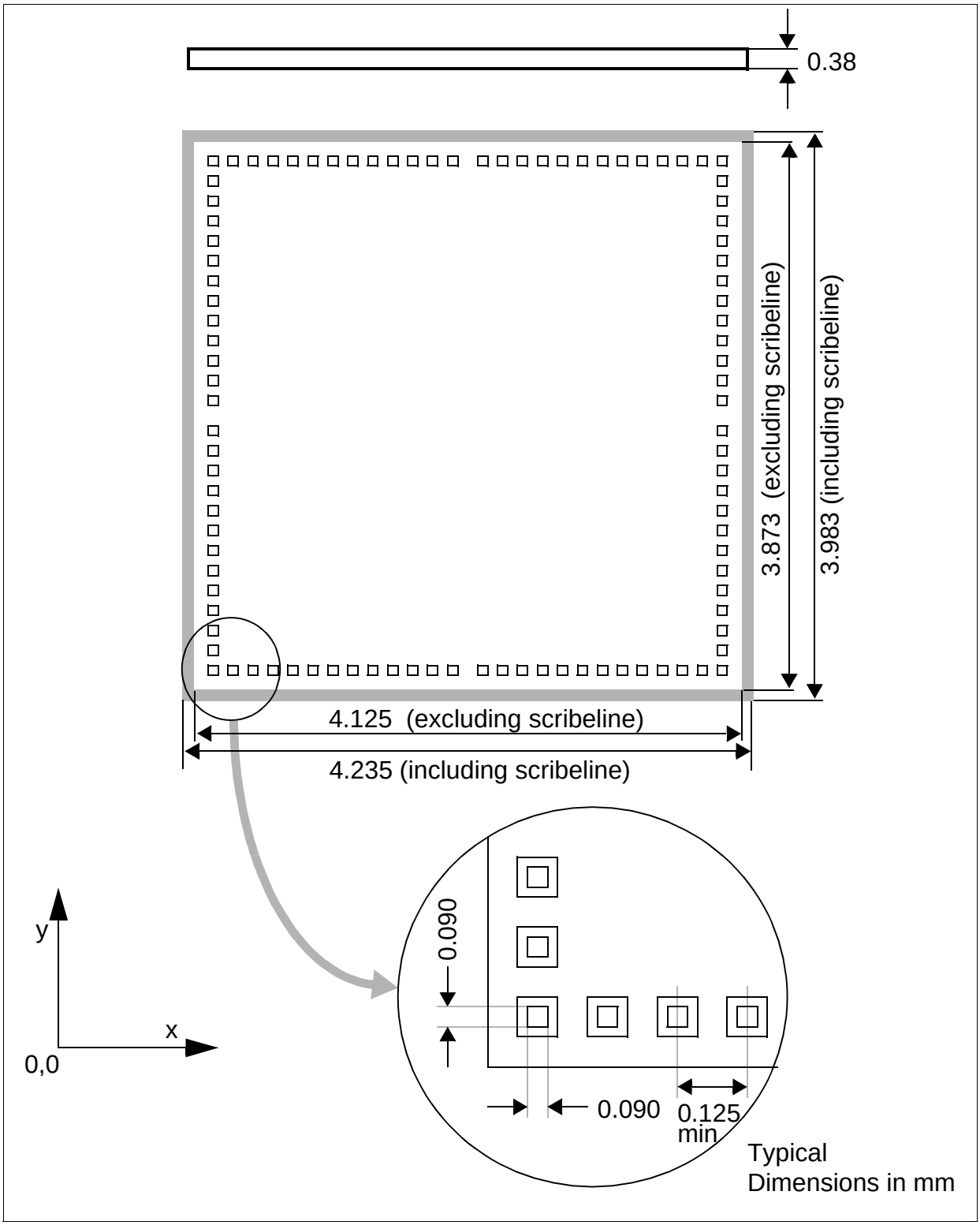

Figure 5 Bare Die Outline

Table 5 Wafer Characteristics

Item	Characteristic
Chips per wafer	820
Metallization layers	2
Metallization material	AlCu
Metallization thickness	Met1: 450 nm, Met2: 800 nm
Metallization barrier material	Ti/Tin
Metallization isolation	FLOW-FILL
Metallization material on pads	AlCu (Al 99.5% - Cu 0.5%)
Passivation	Si-Oxide (310 nm) + Si-Nitride (510 nm)
Backside metallization	None (silicon)
Inkdot diameter	1.0-1.3 mm (typical)

The wafers are glued to a plastic tape which is fixed within a plastic ring (see figure below).

Wafers can be shipped in one piece or sawn into individual dies.

Wafer Outline

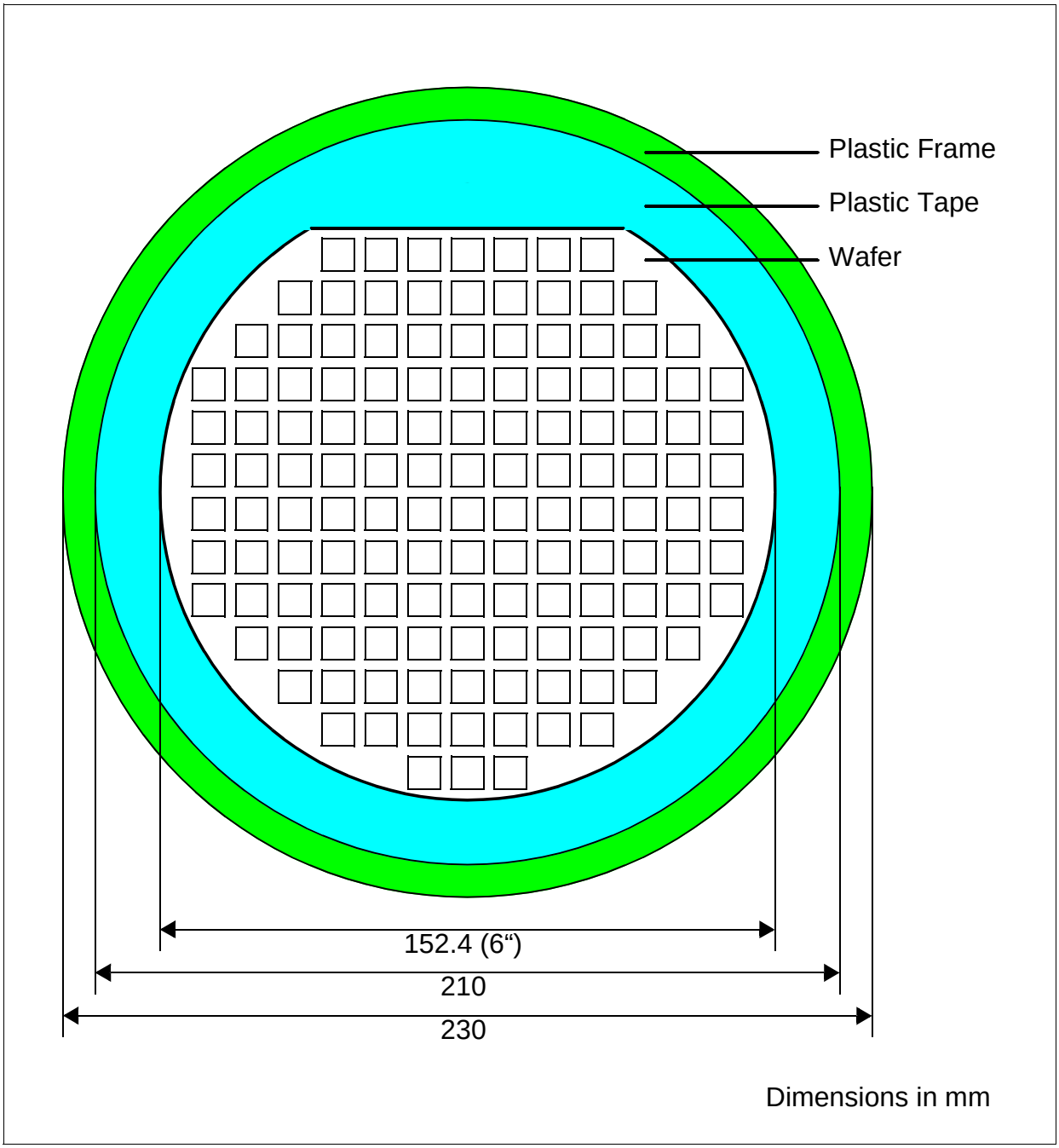

Figure 6 Wafer Outline

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Dr. Ulrich Schumacher

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