Ordering number : ENA1149

SANYO Semiconductors

DATA SHEET

2SC6144 — NPN Epitaxial Planar Silicon Transistor
High-Current Switching Applications

Applications

- Relay drivers, lamp drivers, motor drivers.

Features

- Adoption of MBIT process.
- High current capacitance.
- Low collector-to-emitter saturation voltage.
- High-speed switching.

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		60	V
Collector-to-Emitter Voltage	V_{CEO}		50	V
Emitter-to-Base Voltage	V_{EBO}		5	V
Collector Current	I_C		10	A
Collector Current (Pulse)	I_{CP}		13	A
Base Current	I_B		2	A
Collector Dissipation	P_C		2	W
		Tc=25°C	25	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		−55 to +150	°C

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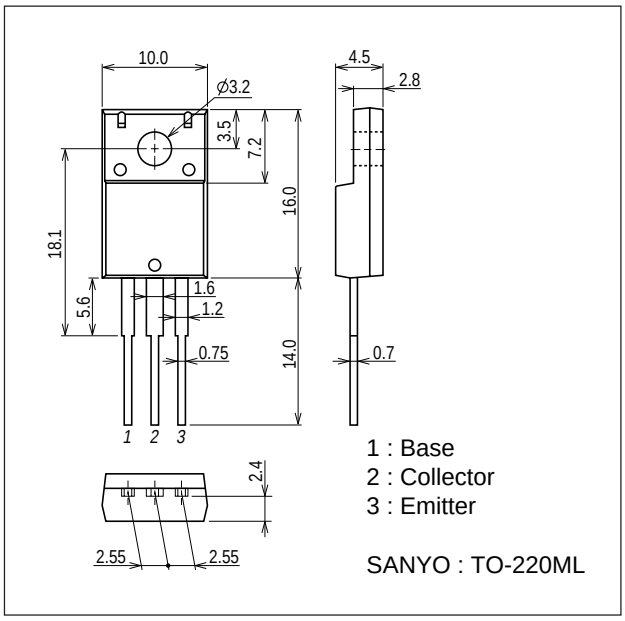
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=40V, I_E=0A			10	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=4V, I_C=0A			10	μA
DC Current Gain	h_{FE}	V_{CE}=2V, I_C=270mA	200		560	
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=3A		330		MHz
Output Capacitance	Cob	V_{CB}=10V, f=1MHz		60		pF
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C=6A, I_B=300mA		180	360	mV
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=6A, I_B=300mA			1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0A	60			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, R_{BE}=∞	50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=100μA, I_C=0A	5			V
Turn-ON Time	t_{on}	See specified Test Circuit.		62		ns
Storage Time	t_{stg}	See specified Test Circuit.		350		ns
Fall Time	t_f	See specified Test Circuit.		25		ns

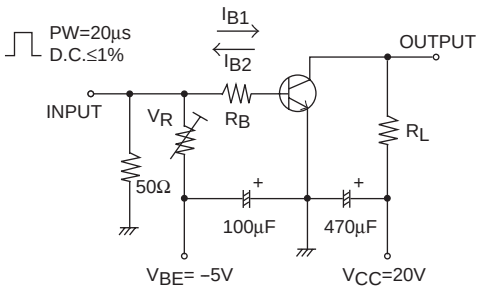
Package Dimensions

unit : mm (typ)

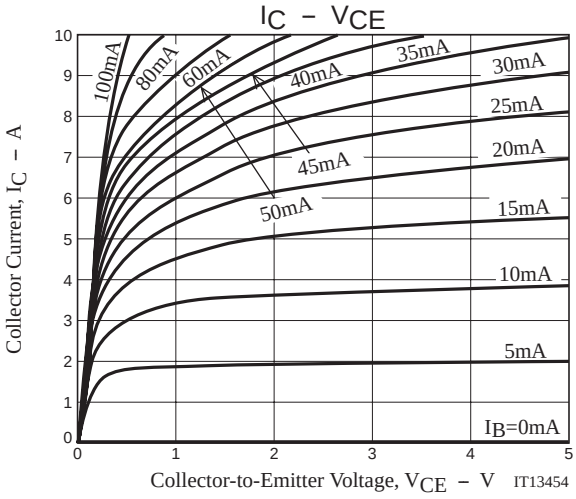
7508-002

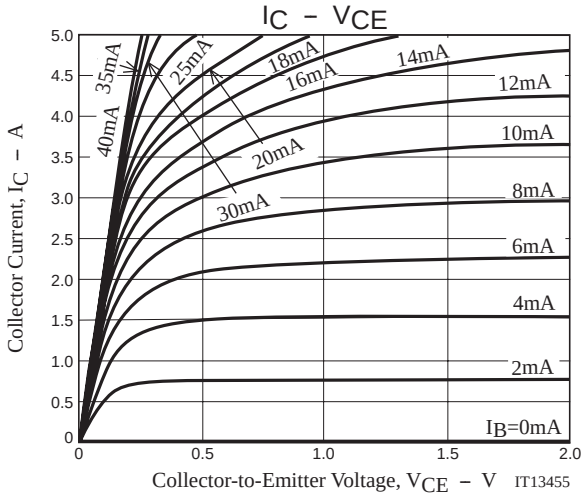


Switching Time Test Circuit

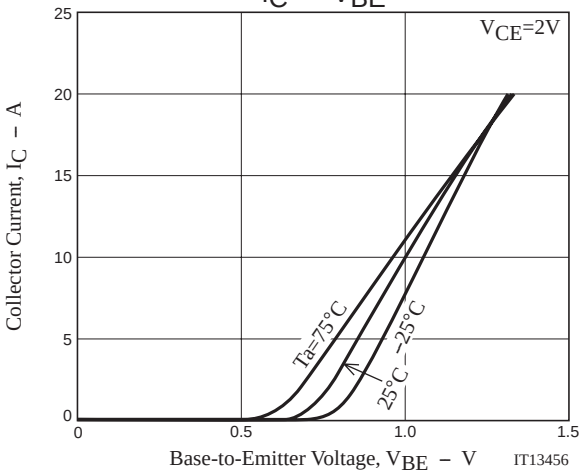


I_C=20I_{B1}= −20I_{B2}=5A

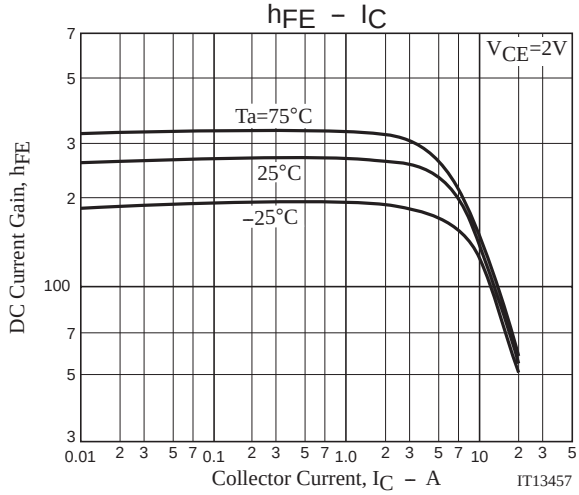




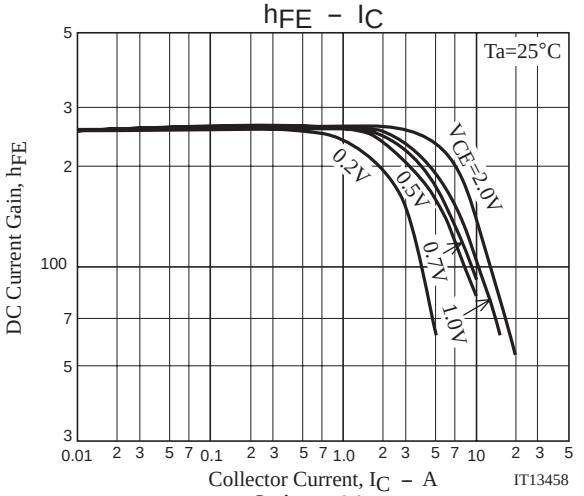
I_C – V_{BE}



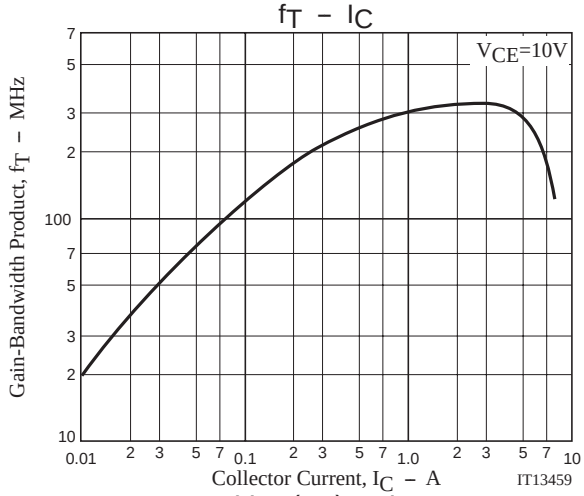
h_{FE} – I_C



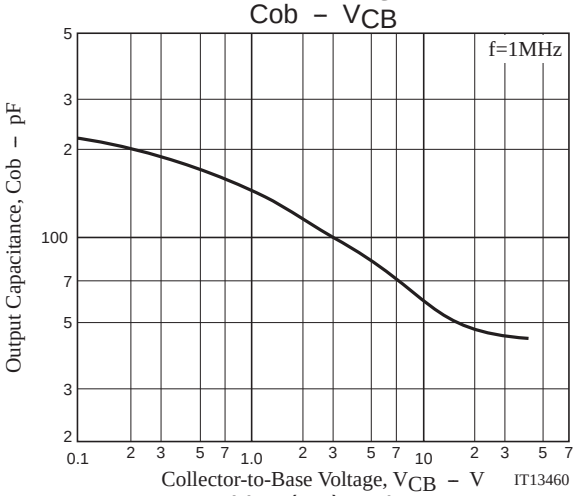
h_{FE} – I_C



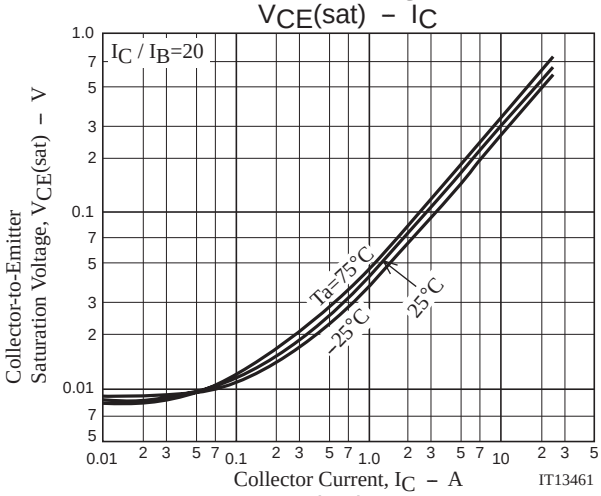
f_T – I_C



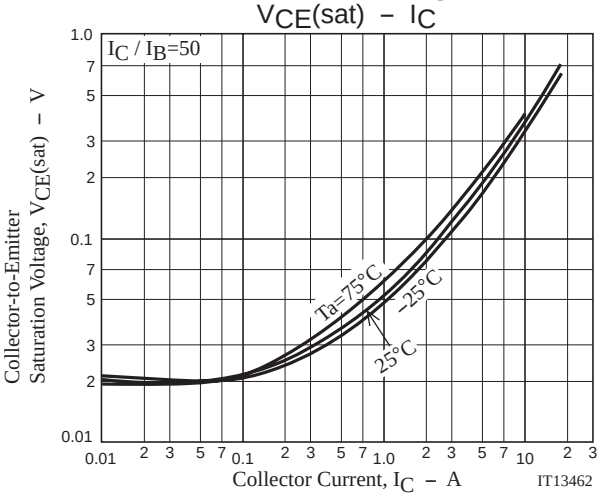
Cob – V_{CB}



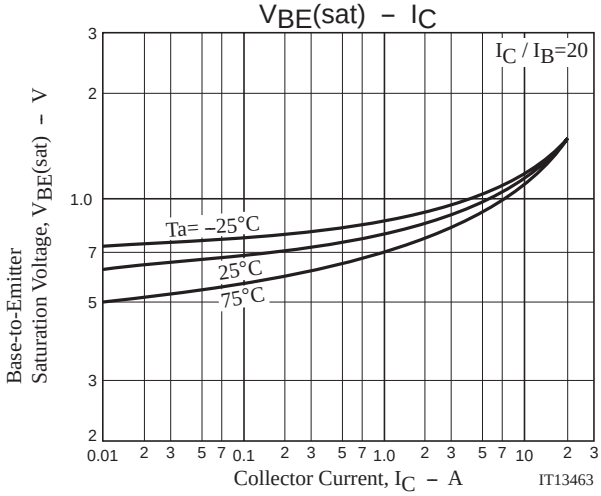
V_{CE}(sat) – I_C



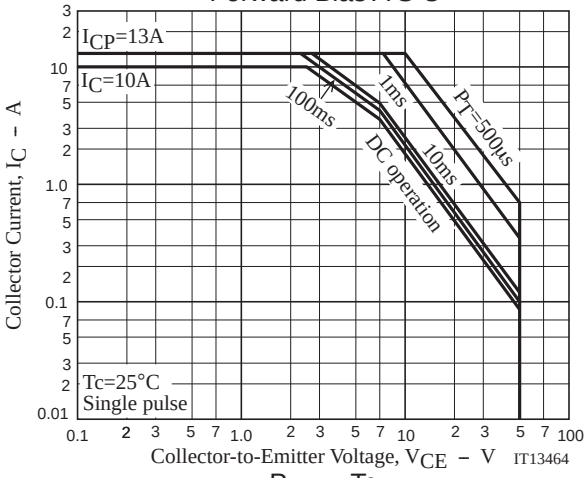
V_{CE}(sat) – I_C



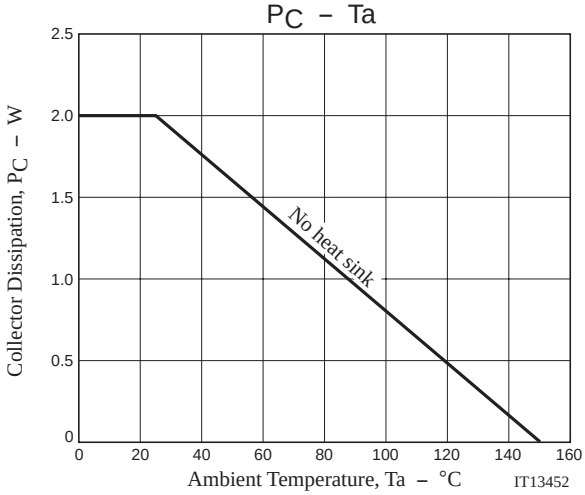
V_{BE}(sat) – I_C



Forward Bias A S O



PC – Ta



PC – Tc