# C6845
# CRT Controller Megafunction



## General Description

The C6845 Cathode Ray Tube Controller (CRTC) interfaces a microprocessor to a raster-scan CRT display. The C6845 is a synchronous, synthesizable VHDL megafunction, functionally equivalent to the Motorola MC6845 CRT Controller.

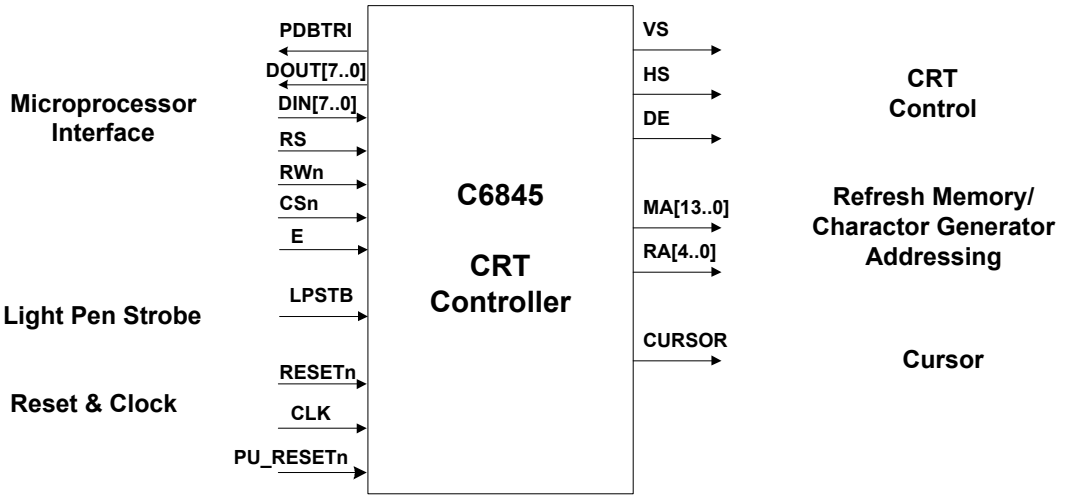
The microprocessor access 19 registers (1 Address and 18 Data Registers) within the C6845 in order to provide video timing, refresh memory addresses, cursor, and light pen strobe signals. CRT video timing signals include Vertical Sync (VS), Horizontal Sync (HS), and Display Enable (DE) output signals. Refresh memory addressing includes Memory Address (MA[13:0]) and Row Address (RA[4:0]) output buses.

The C6845 microprocessor interface consist of unidirectional data input (DIN[7:0]) and data output (DOUT[7:0]) buses and control signals RS, RWn, CSn, and E. Optionally, an available bus wrapper converts the unidirectional data buses into an 8-bit bi-directional data bus (D[7:0]). This is the pin equivalent to the MC6845.

## Features

- Fully-synchronous, synthesizable VHDL Megafunction, functionally equivalent to Motorola MC6845
- Capable of driving alphanumeric, semi-graphic, or bit-mapped graphics displays
- Wide range of programmable alphanumeric screen formats
- Programmable registers controlling output signals Vertical Sync (VS), Horizontal Sync (HS), and Display Enable (DE) signals
- Programmable horizontal line rate and sync pulse width
- Programmable vertical frame rate
- Programmable registers controlling Memory Address (MA[13:0]) start address
- Programmable Start Address Register for Hardware Scrolling
- Programmable registers controlling Row Address (RA[4:0]) size, yielding a character row
- Programmable register controlling Normal Sync (Non-Interlace), Interlace Sync, or Interlace Sync & Video Mode
- Programmable registers for control and format of Cursor
- Light Pen Register
- Microprocessor 8-bit Data Bus and Control Interface

## Symbol






## Pin Description

| Name | Type | Polarity | Description |
|---|---|---|---|
| **Microprocessor Interface** | | | |
| DIN[7..0] | IN | - | Data Bus Input |
| DOUT[7..0] | OUT | - | Data Bus Output |
| PDBTRI | OUT | (See Description) | Processor Data Bus Tri-state Control<br>H= Processor Reads<br>L= Processor Writes |
| RS | IN | Low | Address Register Select |
| | | High | Data Register Select |
| RWn | IN | Low | Write to Internal Register |
| | | High | Read Internal Register |
| CSn | IN | Low | Chip Select |
| E | IN | High | Enable Data Bus Output During Microprocessor Reads |
| | | Falling Edge | Register Data During Microprocessor Writes |
| **Light Pen Strobe Interface** | | | |
| LPSTB | IN | Rising Edge | Light Pen Strobe |
| **Reset and Clock Interface** | | | |
| RESETn | IN | Low | Reset/Test Mode |
| CLK | IN | Falling Edge | Synchronous Clock (Except for Micro-processor Interface) |
| PU_RESETn | IN | Low | Asynchronous Power-up Reset |
| **CRT Control Interface** | | | |
| DE | OUT | High | Display Enable |
| HS | OUT | High | Horizontal Sync |
| VS | OUT | High | Vertical Sync |
| **Refresh Memory/Character Generator Addressing Interface** | | | |
| MA[13..0] | OUT | - | Refresh Memory Address |
| RA[4..0] | OUT | - | Row Address |
| **Cursor Interface** | | | |
| CURSOR | OUT | High | Cursor |

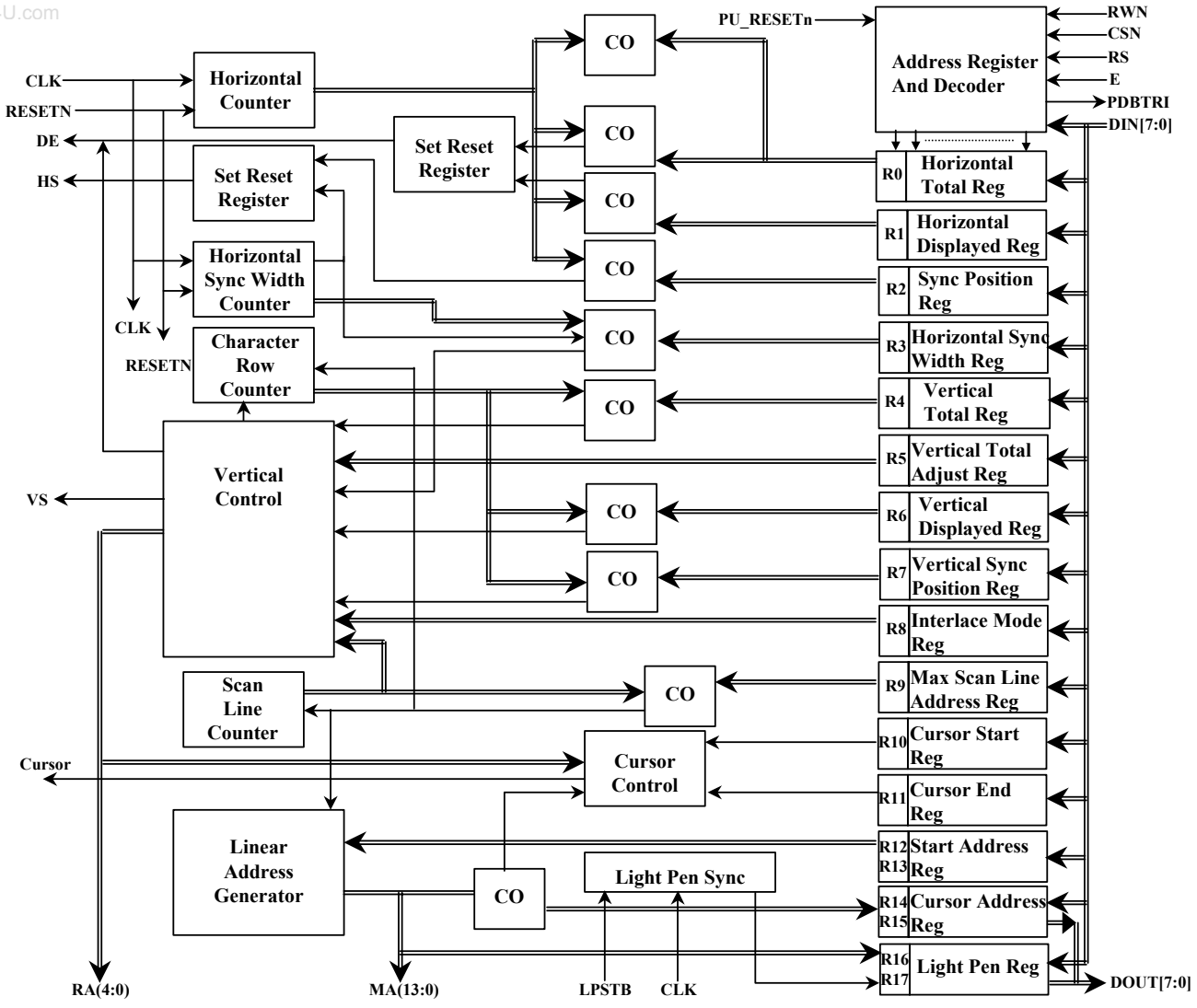
## Applications

- Point-of-contact Kiosk

- Medical instrumentation
- Test & Measurement Instrumentation
- Industrial Equipment
- Avionics
- Gaming & Amusement Machines

## Block Diagram






## Functional Description

This section describes the Block Diagram above. A description of each of the blocks in the diagram is given here.

## Horizontal Timing

The Horizontal Timing section consist of the Horizontal Counter, Horizontal Sync Width Counter, Registers R0 through R3, and associated synchronous Set/Reset Flip-Flops and Coincidence Circuits.

The Horizontal Counter counts from zero until coincidence with Register R0 synchronously resets the counter. This represents the horizontal line rate and enabling of the Display Enable (DE) for a new line takes place.

Coincidence of the Horizontal Counter with Register R1 marks the end of the active display portion of a horizontal line with Display Enable (DE) going inactive.

Coincidence of the Horizontal Counter with Register R2 marks the beginning of horizontal retrace with Horizontal Sync (HS) going active high.

Coincidence of the Horizontal Sync Width Counter with Register R3 marks the end of horizontal retrace with Horizontal Sync (HS) going inactive low.

## Vertical Timing

The Vertical Timing section consists of the Scan Line Counter, Character Row Counter, Registers R4 through R9, the Vertical Control logic block, and associated Coincidence Circuits.

The Scan Line Counter counts from zero until coincidence with Register R9 synchronously resets the Scan Line Counter and synchronously increments the Character Row Counter. The Scan Line Counter counts the Scan Lines composing a character row, and the Character Row Counter counts the character rows comprising a vertical frame.

The Character Row Counter coincidence with R4 and the residual Scan Line count represented by R5 marks the end of a vertical frame.

The Character Row Counter coincidence with Register R6 marks the end of the active display portion of the vertical frame measured in character rows.

The Character Row Counter coincidence with Register R7 marks the beginning of vertical retrace with Vertical Sync (VS) going active high. VS remains high for a fixed period of 16 scan lines.

Register R8, Interlace Mode Register, effects the Vertical Timing according to its programming. Normal Sync (Non-Interlace) mode displays the same field each frame. Interlace Sync Mode splits a frame into even and odd fields. Vertical Sync (VS) active high is delayed one-half scan line at the end of even fields. For Interlace Sync & Video Mode, in addition to the VS delay on even fields, the Row Address counter sequences on even fields through 0,2,4,… counter values while on odd fields, through 1,3,5,… counter values.

## Cursor

The Cursor section consist of the Cursor Control, Cursor Start Register R10, Cursor End Register R11, Cursor Address Registers R14 and R15, and associated Interlace Mode Register settings and Refresh Memory Address and Row Address buses as well as associated Coincidence Circuits.

As a first condition for activating the cursor, Cursor Address Registers R14 and R15 signify the character in linear address space the cursor can be active. Then, Cursor Start Register R10 and Cursor End Register R11 select the scan lines within the designated character space the cursor will be active.

In addition, Cursor Start Register R10 contains a 2-bit field indicating whether the cursor is active or not, and, if so, whether it should blink or not, and, if blink, at $1/16^{th}$ or $1/32^{nd}$ the field rate.

### Start Address

Start Address Register R12 and R13 indicate the first address the Linear Address Generator puts on the Refresh Memory Address bus at the start of a vertical frame. Whenever the microprocessor writes to R12 and R13, the Linear Address Generator is updated at the start of the next vertical frame.

### Light Pen Register

On the rising edge of the LPSTB input, after synchronization by two CLK cycles, the value of the Refresh Memory Address bus is captured by the Light Pen Registers R16 and R17. These registers are readable by-way-of the microprocessor interface.

### Linear Address Generator



The Linear Address Generator generates the Refresh Memory Address. The Linear Address Generator initializes to the value of the Start Address Registers R12 and R13 at the start of each vertical frame. The Linear Address Generator remains active during horizontal and vertical retrace, for refresh of dynamic RAMs.

## Device Utilization & Performance

| Supported Family | Device Tested | Utilization | | | Performance $F_{max}$ |
|---|---|---|---|---|---|
| | | LEs | Memory | Memory bits | |
| Cyclone | EP1C20-6 | 399 | 0 | 0 | 186 MHz |
| Stratix | EP1S20-5 | 399 | 0 | 0 | 194 MHz |
| Stratix-II | EP2S60-3 | 330 | 0 | 0 | 221 MHz |

## Deliverables

### Encrypted Netlist License

- Post synthesis EDIF netlist
- Assignment & Configuration
- Symbol & Include files
- Testbench
- Vectors for testing the functionality of the megafunction
- Place & Route Scripts
- Documentation

### VHDL Source License

- VHDL RTL source code
- Testbenches
- Vectors for testing functionality
- Expected results
- Synthesis scripts
- Simulation scripts
- Documentation



## Related Information

**MC6845 CRT Controller**

Contact:
Motorola Semiconductors
3501 ED Bluestein Blvd.
Austin, Texas 78721
Phone: 512-933-6000
800-201-0399 (literature)
URL: www.motorola.com

To obtain a copy of the MC6845 CRT Controller Data Sheet, contact CAST.

## Contact Information

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This core developed by the peripheral controller experts at Digital Blocks, Inc.