

**C717DB**

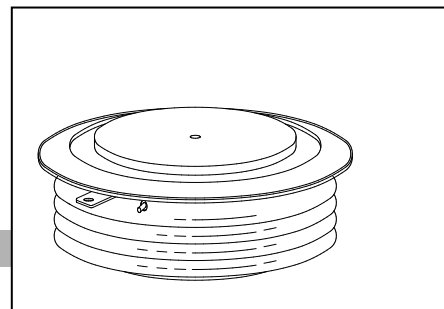
**- Power Thyristor  
4200 V<sub>DRM</sub>;**

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**HIGH POWER THYRISTOR PHASE CONTROL APPLICATIONS**

**Features:**

- . All Diffused Structure
- . Spoke Amplifying Gate Configuration
- . Blocking capability up to 4200 volts
- . Guaranteed Maximum Turn-Off Time
- . High dV/dt Capability
- . Pressure Assembled Device



**ELECTRICAL CHARACTERISTICS AND RATINGS**

**Blocking - Off State**

Device Type	V <sub>RRM</sub> (1)	V <sub>DRM</sub> (1)	V <sub>RSM</sub> (1)
C717	4200	4200	4300

- V<sub>RRM</sub> = Repetitive peak reverse voltage
- V<sub>DRM</sub> = Repetitive peak off state voltage
- V<sub>RSM</sub> = Non repetitive peak reverse voltage (2)

Repetitive peak reverse leakage and off state leakage	I <sub>RRM</sub> /I <sub>DRM</sub>	75 mA (3)
Critical rate of voltage rise	dV/dt (4)	1000 V/μsec

**Conducting - on state**

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Average value of on-state current	I <sub>T(AV)</sub>		800		A	Sinewave, 180° conduction, T <sub>C</sub> =70°C
Peak one cpstcle surge (non repetitive) current	I <sub>TSM</sub>		8000		A	10.0 msec (50Hz), sinusoidal wave-shape, 180° conduction, T <sub>j</sub> = 125 °C
I square t	I <sup>2</sup> t		0.31x10 <sup>6</sup>		A <sup>2</sup> s	10.0msec
Latching current	I <sub>L</sub>		500		mA	V <sub>D</sub> = 24 V; R <sub>L</sub> = 12 ohms
Holding current	I <sub>H</sub>		500		mA	V <sub>D</sub> = 24 V; I = 2.5 A
Peak on-state voltage	V <sub>TM</sub>		1.90		V	I <sub>TM</sub> = 1000 A; T <sub>j</sub> = 125 °C
Critical rate of rise of on-state current (5, 6)	di/dt		100		A/μs	Switching from V <sub>DRM</sub> ≤ 1000 V, non-repetitive
Critical rate of rise of on-state current (6)	di/dt		50		A/μs	Switching from V <sub>DRM</sub> ≤ 1000 V

Notes:

- All ratings are specified for T<sub>j</sub>=25 °C unless otherwise stated.
- (1) All voltage ratings are specified for an applied 50Hz/60zHz sinusoidal waveform over the temperature range -40 to +125 °C.
- (2) 10 msec. max. pulse width
- (3) Maximum value for T<sub>j</sub> = 125 °C.
- (4) Minimum value for linear and exponential waveshape to 80% rated V<sub>DRM</sub>. Gate open. T<sub>j</sub> = 125 °C.
- (5) Non-repetitive value.
- (6) The value of di/dt is established in accordance with EIA/NIMA Standard RS-397, Section 5-2-2-6. The value defined would be in addition to that obtained from a snubber circuit, comprising a 0.2 μF capacitor and 20 ohms resistance in parallel with the thristor under test.

**ELECTRICAL CHARACTERISTICS AND RATINGS**  
**Thyristor**

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**Gating**

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Peak gate power dissipation	$P_{GM}$		200		W	$t_p = 40 \mu s$
Average gate power dissipation	$P_{G(AV)}$		5		W	
Peak gate current	$I_{GM}$		20		A	
Gate current required to trigger all units	$I_{GT}$		300 200 125		mA mA mA	$V_D = 6 V; R_L = 3 \text{ ohms}; T_j = -40 \text{ }^\circ\text{C}$ $V_D = 6 V; R_L = 3 \text{ ohms}; T_j = +25 \text{ }^\circ\text{C}$ $V_D = 6 V; R_L = 3 \text{ ohms}; T_j = +125 \text{ }^\circ\text{C}$
Gate voltage required to trigger all units	$V_{GT}$	0.30	5 4		V V V	$V_D = 6 V; R_L = 3 \text{ ohms}; T_j = -40 \text{ }^\circ\text{C}$ $V_D = 6 V; R_L = 3 \text{ ohms}; T_j = 0-125 \text{ }^\circ\text{C}$ $V_D = \text{Rated } V_{DRM}; R_L = 1000 \text{ ohms}; T_j = +125 \text{ }^\circ\text{C}$
Peak negative voltage	$V_{GRM}$		20		V	

**Dynamic**

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Delay time	$t_d$		2.0		$\mu s$	$I_{TM} = 50 \text{ A}; V_D = 67\% V_{DRM}$ Gate pulse: $V_G = 30 \text{ V}; R_G = 10 \text{ ohms}; t_r = 0.1 \mu s; t_p = 20 \mu s$
Turn-off time (with $V_R = -50 \text{ V}$ )	$t_q$		250		$\mu s$	$I_{TM} > 2000 \text{ A}; di/dt = 10 \text{ A}/\mu s;$ $V_R \geq -50 \text{ V};$ Re-applied $dV/dt = 20 \text{ V}/\mu s$ linear to $67\% V_{DRM};$ $T_j = 125 \text{ }^\circ\text{C};$ Duty cycle $\geq 0.01\%$
Reverse recovery current	$I_{rr}$		150		A	$I_{TM} > 2000 \text{ A}; di/dt = 10 \text{ A}/\mu s;$ $V_R \geq -50 \text{ V}$

**THERMAL AND MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Operating temperature	$T_j$	-40	+125		$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-40	+150		$^\circ\text{C}$	
Thermal resistance - junction to case	$R_{\theta(j-c)}$		0.025 0.050		$^\circ\text{C}/\text{W}$	Double sided cooled Single sided cooled
Thermal resistance - case to sink	$R_{\theta(c-s)}$		0.010 0.020		$^\circ\text{C}/\text{W}$	Double sided cooled * Single sided cooled *
Mounting force	P	5500 24.5	6000 26.7		lb. kN	
Weight	W			16 460	oz. g	

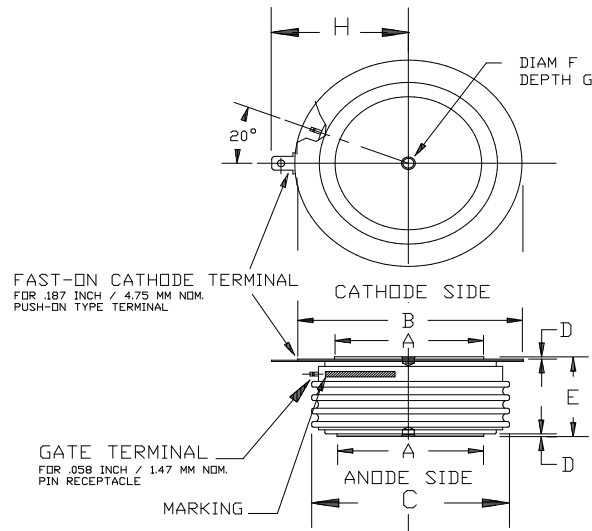
\* Mounting surfaces smooth, flat and greased

Note : for case outline and dimensions, see case outline drawing in page 3 of this Technical Data

CASE OUTLINE AND DIMENSIONS.

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Thyristor



STRIKE DISTANCE = .58 INCH / 14.7 MM MIN.  
 CREEPAGE DISTANCE = 1.00 INCH / 25.4 MM MIN.

OUTLINE DIMENSIONS - CASE 4T				
DIMENSIONS	Min. mm	Max. mm	Min. In.	Max. In.
DIAM A	43.18	48.26	1.70	1.90
DIAM B	63.50	75.18	2.50	2.96
DIAM C	--	67.31	--	2.65
D	0.76	--	0.03	--
E	25.40	27.18	1.00	1.07
F	3.30	3.81	0.13	0.15
G	1.78	2.03	0.07	0.08
H	--	44.20	--	1.74