PRELIMINARY

C9851

Clock Generator for Pentium®III Server and Workstation Applications

Product Features

- Six pairs of current referenced differential clocks
- Two 3V 180° displaced Mref clocks for DRCG
- One 66.6 MHz reference output
- One 14.318 MHz reference output
- Select logic for Differential Swing Control, Test mode, Hi-Z, Power-down, Spread spectrum, and limited frequency select
- Cypress Spread Spectrum for EMI reduction
- 48 Pin SSOP Package

Product Description

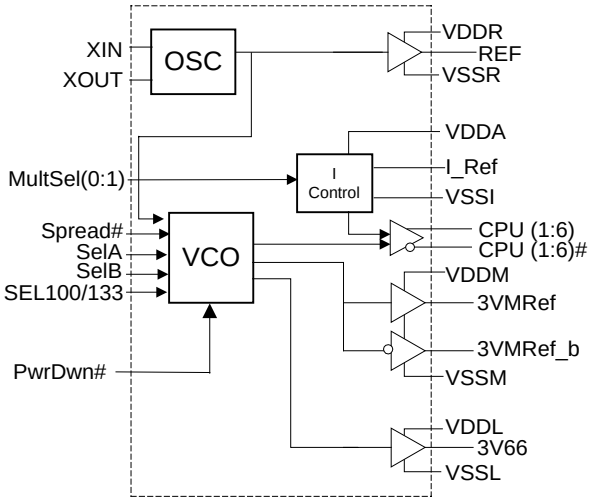
This device provides the necessary clocks for a differential host bus system in multi-processor servers and workstations. It also generates a 66.6MHz hub clock for interfacing with a complimentary part, the Cypress B9852. The 2 Mref clock outputs are 180 degrees out of phase and are used for interfacing with the Direct Rambus Clock Generator (DRCG), C9820, C9821, or C9822. This device integrates the Cypress spread spectrum technology for optimum EMI reduction.

Frequency Selection Table

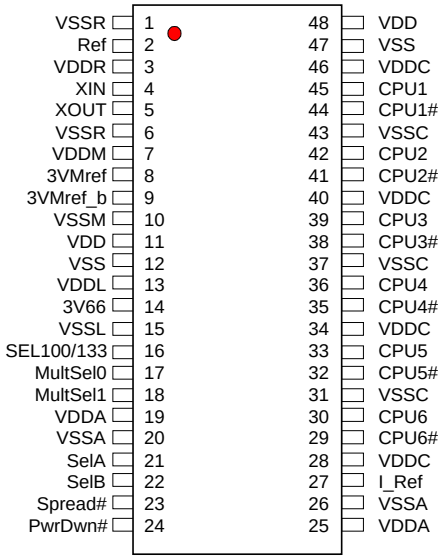
SEL 100/133	SELA	SELB	CPU(1:6), CPU#(1:6)	3VMref, 3Vmref_b	3V66	REF
0	0	0	100 MHz	50 MHz	66.67 MHz	14.318 MHz
0	0	1	100 MHz	Low	Low	Low
0	1	0	200 MHz	50 MHz	66.67 MHz	14.318 MHz
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	133.3 MHz	66.67 MHz	66.67 MHz	14.318 MHz
1	0	1	25 MHz	50 MHz	66.67 MHz	14.318 MHz
1	1	0	200 MHz	66.7 MHz	66.67 MHz	14.318 MHz
1	1	1	REF/2	REF/4	REF	REF

Table 1

Block Diagram



Pin Configuration



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Pin Description

PIN No.	Pin Name	I/O	Description
8	3VMref	O	Output clock for driving the DRCG device. See table 1, page1 for frequency selection.
9	3VMref_b	O	Output clock for driving the DRCG device. See table 1, page1 for frequency selection. It is 180 degrees out of phase (inverted) from the 3VMref clock.
23	Spread#	PU	When asserted low, this pin invokes Spread Spectrum functionality. Spread spectrum is applicable to CPU(1:6), CPU(1:6)#, 3VMref, 3VMref_b, and 3V66 clocks. This pin has a 250KΩ internal Pull-up.
45,42,39,36, 33,30	CPU(1:6)	O	Differential host clock outputs. These outputs are used in pairs, (CPU1-1#, CPU2-2#, CPU3-3#, CPU4-4#, CPU5-5#, and CPU6-6#) for differential clocking of the host bus. CPU(1:6)# are 180 degrees out of phase with their complements, CPU(1:6). See table 1, page 1 for frequency selection.
44,41,38,35, 32,29	CPU(1:6)#		
27	I_Ref	P	This pin establishes the reference current for the internal current steering buffers of the CPU clocks. A resistor is connected from this pin to ground to set the value of this current. See applications data on page 9 of this data sheet for details.
14	3V66	O	Fixed 66.67 MHz clock output for driving the IMI B9852 buffer device.
24	PwrDwn#	PU	When asserted low, this pin Invokes power-down mode by shutting off all the clocks, disabling all internal circuitry, and shutting down the crystal oscillator. The 3VMref, 3VMref_B, 3V66, REF and CPU clocks are driven low during this condition. It has a 250KΩ internal Pull-up.
22, 21	SelA, SelB	PD	Input select pins. See table 1, page 1. Each pin has a 250KΩ internal Pull-down
16	SEL100/133	PU	Input select pin. See table 1, page 1. It has a 250KΩ internal Pull-up
5	XOUT	O	Crystal Buffer output pin. Connects to a crystal only. When an external signal other than a crystal is used or when in Test mode, this pin is kept unconnected.
4	XIN	I	Crystal Buffer input pin. Connects to a crystal, or an external single ended input clock signal.
2	REF	O	A buffered output clock of the signal applied at Xin. Typically, 14.31818MHz.
18, 17	MultSel (0,1)	I	These input select pins configure the LOH current (and thus the VOH swing amplitude) of the CPU clock output pairs. Each pin has a 250KΩ internal Pull-up. See the table 5 for current and resistor values.
3	VDDR	P	3.3V power supply pins for Ref clock and crystal buffer.
46,40,34,28	VDDC	P	3.3V power supply pins for CPU(1:6) / CPU(1:6)# outputs.
11, 48	VDD	P	3.3V power supply pins for common supply to the core.
13	VDDL	P	3.3V power supply pins for 3V66 output.
19, 25	VDDA	P	3.3V power supply pins for internal current reference circuitry and internal PLL.
7	VDDM	P	3.3V power supply pin for 3Vmref and 3Vmref_b outputs
1, 6	VSSR	P	Ground pins for the Ref clock and crystal buffer.
31, 37, 43	VSSC	P	Ground pins for the CPU(1:6)/CPU(1:6)# outputs.
12, 47	VSS	P	Ground pins for common supply to the core.
15	VSSL	P	Ground pin for the 3V66 output.
20, 26	VSSA	P	Ground pin for internal current reference circuitry and internal PLL.
10	VSSM	P	Ground pin for 3Vmref and 3Vmref_b outputs.

Note: Definition of I/O column pneumonic on pin description table above:
I = Input pin, O = output pin, P = power supply pin, PU = This indicated that a bi-directional pin contains a device internal pull-up resistor. This will insure that this pin of the device will be seen by the internal logic as a logic 1 level. Likewise pins with a PD designation are guaranteed to be seen as a logic 0 level if no external level setting circuitry is present at power up.

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.5V
Maximum Input Voltage Relative to VSS: VDD + 0.7V
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: 0ºC to +70ºC
Maximum ESD protection 2000V
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters (VDDI = VDD = VDDR = VDDL = VDDM = VDDC = 3.3V ±5%, TA = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	0.8	Vdc	Note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Current (@Vin = VSS)	IIL	-16		-4	µA	For internal Pull up resistors, Note 1 and Note 2
Input High Current (@Vin = VDD)	IIH	0		5	µA	-
Input Low Current (@Vin = VSS)	IIL	0		-	µA	For internal Pull down resistors, Note 1 and Note 2
Input High Current (@Vin = VDD)	IIH	4		16	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Static Supply Current	Idd	-	-	30	mA	PwrDwn=Low
Dynamic Supply Current	Isdd	-	-	200	mA	133 MHz CPU, Note 3
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin Inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	34	36	38	pF	Measured from Pin to Ground. See crystal specification section presented later in this data sheet.
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
Internal Pull-up and Pull-down resistor value	Rpi	200	250	500	KΩ	

Note1: Applicable to input signals: Sel100/133, Sel(A:B)), Spread#, PWRDN#, MultSel(0:1)
Note2: Although internal pull-up or Pull-Down resistors have a typical value of 250K, this value may vary between 200K and 500K.
Note3: All outputs loaded as per the maximum capacitive table in this data sheet.

AC Parameters (VDDI = VDD = VDDR = VDDL = VDDM = VDDC = 3.3V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	133 MHz Host		100 MHz Host		Units	Notes
		Min	Max	Min	Max		
TPeriod	CPU[(1:6), (1:6)#] period -	7.35	7.65	9.85	10.2	nS	1, 2
Tr / Tf	CPU[(1:6), (1:6)#] rise and fall times	175	450	175	450	pS	2, 3
TSKEW1	skew from any CPU pair to any CPU pair	-	150	-	150	pS	2, 4, 5
TSKEW2	skew from package to package	-	100	-	100	pS	2, 4, 5
TCCJ	CPU[(1:6), (1:6)#] Cycle to Cycle Jitter	-	150	-	150	pS	2, 4, 5
Vover	CPU[(1:6), (1:6)#] Overshoot		Voh+0.2		Voh+0.2	V	2,10
Vunder	CPU[(1:6), (1:6)#] Undershoot		-0.2		-0.2	V	2, 10
Vcrossover	CPU(1:6) to CPU(1:6)# crossover point	45%Voh	55%Voh	45%Voh	55%Voh	V	2, 4
Tduty	Duty Cycle	45	55	45	55	%	2, 4
TPeriod	3V(MREF, MREF_B) period	15.0	15.3	20.0	20.4	nS	4, 5
THIGH	3V(MREF, MREF_B) high time	5.25	-	7.5	-	nS	2, 6
TLOW	3V(MREF, MREF_B) low time	5.05	-	7.3	-	nS	2, 7
Tr / Tf	3V(MREF, MREF_B) rise and fall times	0.4	1.6	0.4	1.6	nS	2, 3
TSKEW	3VMREF to 3VMREF_B skew	-	250	-	250	pS	2, 4, 5, 11
TCCJ	3V(MREF, MREF_B) Cycle to Cycle Jitter	-	250	-	250	pS	2, 4, 5
Tduty	Duty Cycle	45	55	45	55	%	2, 4
TPeriod	3V66 period	15.0	16.0	15.0	15.2	nS	1, 2, 4
THIGH	3V66 high time	5.25	-	5.25	-	nS	2,6
TLOW	3V66 low time	5.05	-	5.05	-	nS	2, 7
Tr / Tf	3V66 rise and fall times	0.5	2.0	0.5	2.0	nS	2, 3
TCCJ	3V66 Cycle to Cycle Jitter	-	300	-	300	pS	2, 4, 5
Tduty	Duty Cycle	45	55	45	55	%	2, 4
TPeriod	REF period	69.8413	71.0	69.8413	71.0	nS	1, 2, 4
Tr / Tf	REF rise and fall times	1.0	4.0	1.0	4.0	nS	2, 3
TCCJ	REFCycle to Cycle Jitter	-	1000	-	1000	pS	2, 4
Tduty	Duty Cycle	45	55	45	55	%	2, 4
tpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	nS	9
tpLZ, tpZH	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	nS	9
tstable	All clock Stabilization from power-up		3		3	mS	

Group Limits and Parameters (applicable to all settings: Sel133/100# = x) continued

Note 1: This parameter is measured at the crossing points of the differential signals, and acquired as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 2: All outputs loaded as per table 2 below.
Note 3: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and at 20% and 80% for CPU[(1:6), (1:6)#] signals. (see Figs.7A & 7B)
Note 4: Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals and at crossing points for CPU clocks (see Figs.7A & 7B).
Note 5: This measurement is applicable with Spread ON or Spread OFF.
Note 6: Probes are placed on the pins, and measurements are acquired at 2.4V (see Figs. 7A & 7B)
Note 7: Probes are placed on the pins, and measurements are acquired at 0.4V. (see Figs. 7A & 7B)
Note 9: As this function is available through SEL(A,B), therefore, the time specified is guaranteed by design.
Note 10: Determined as a fraction of 2*(Trp-Trn) / (Trp+Trn) where Trp is a rising edge and Trn is an intersecting falling edge.
Note 11: 3VMref and 3VMref_b are 180 degrees out of phase, therefore, the skew is measured between the rising edge of one and the falling edge of the other.

Group Limits and Parameters (applicable to all settings: Sel133/100# = x) (Continued)

Output name	Max Load
CPU[(1:6), (1:6)#]	Rs = 33.2Ω, Rp = 49.9Ω
3VMref, 3VMref_b	30 pF
REF	20 pF
3V66	30 pF

Table 2.

Lumped Test Load Configurations

The following shows lumped test load configurations for the differential Host Clock Outputs. (MULTsel1 = 0, MULTsel0 = 1)

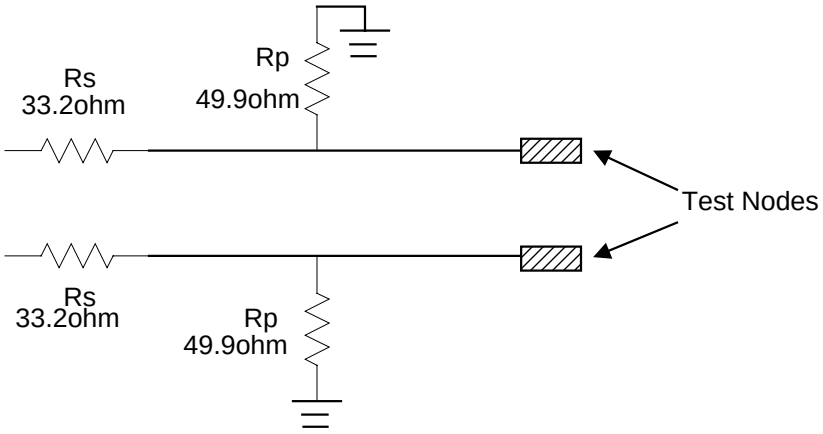
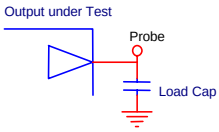


Fig.1A

Lumped Test Load Configurations (Cont.)



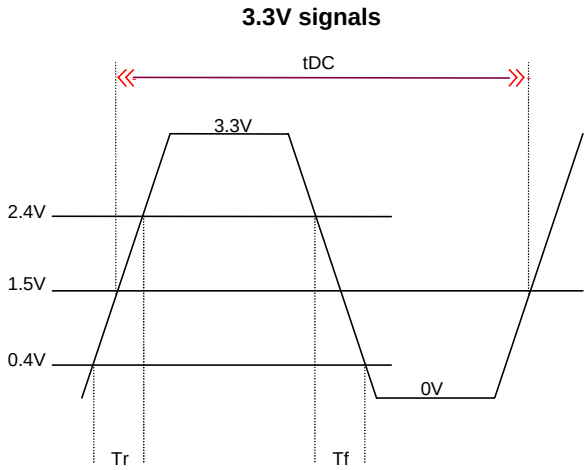


Fig. 1B

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from (Fig.2) its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). The default of the device at power up keeps the Spread Spectrum disabled, therefore, in order to enable this function pin23, Spread#, must be connect to ground (a low state.). See table 3 for Spread bandwidth description.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by -0.25%. (ex.: assuming the center frequency is 100MHz in non-spread mode; when down spread is enabled, the center frequency shifts to 99.75MHz.).

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Spread Spectrum Clock Generation (SSCG) (Cont.)

Down Spread

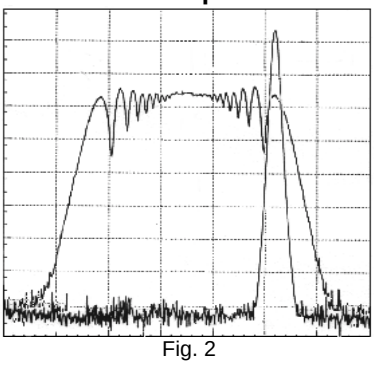


Fig. 2

Spectrum Spreading Selection Table

Unspread Frequency in MHz	Spread Spectrum Parameter			
	Down Spreading			
	F Min (MHz)	F Center (MHz)	F Max (MHz)	Spread (%)
100	99.5	99.75	100	- 0.5%
133.3	132.66	132.67	133	- 0.5%

Table 3.

Power Management Functions

Host Swing Select Functions

MultSel0	MultSel1	Board Target Trace/TermZ	Reference Rr, Iref = Vdd/(3*Rr) *Note2*	Output Current	Voh @Z, Iref = 2.32mA
0	**0**	**60 Ohms**	**Rf = 475 1%, Iref = 2.32mA**	**Ioh = 5*Iref**	**0.7V @ 60**
0	0	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6*Iref	0.85V @ 60
0	**1**	**50 Ohms**	**Rr = 475 1%, Iref = 2.32mA**	**Ioh = 6*Iref**	**0.71V @ 50**
1	0	60 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	1	60 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50

Note1: The entries in boldface are the primary system configurations of interest. The outputs should be optimized for these configurations.
Note2: Rr refers to the resistance placed in series with the Iref input and Vss.

Table 4

Buffer Characteristics

Current Mode CPU Clock Buffer Characteristics

The current mode output buffer detail and current reference circuit details are contained elsewhere in this datasheet. The following parameters are used to specify output buffer characteristics:

1. Output impedance of the current mode buffer circuit - Ro (see Figure 3).
2. Minimum and maximum required voltage operation range of the circuit – Vop (see Figure 3).
3. Series resistance in the buffer circuit – Ros (see Figure 3).
4. Current accuracy at given configuration into nominal test load for given configuration.

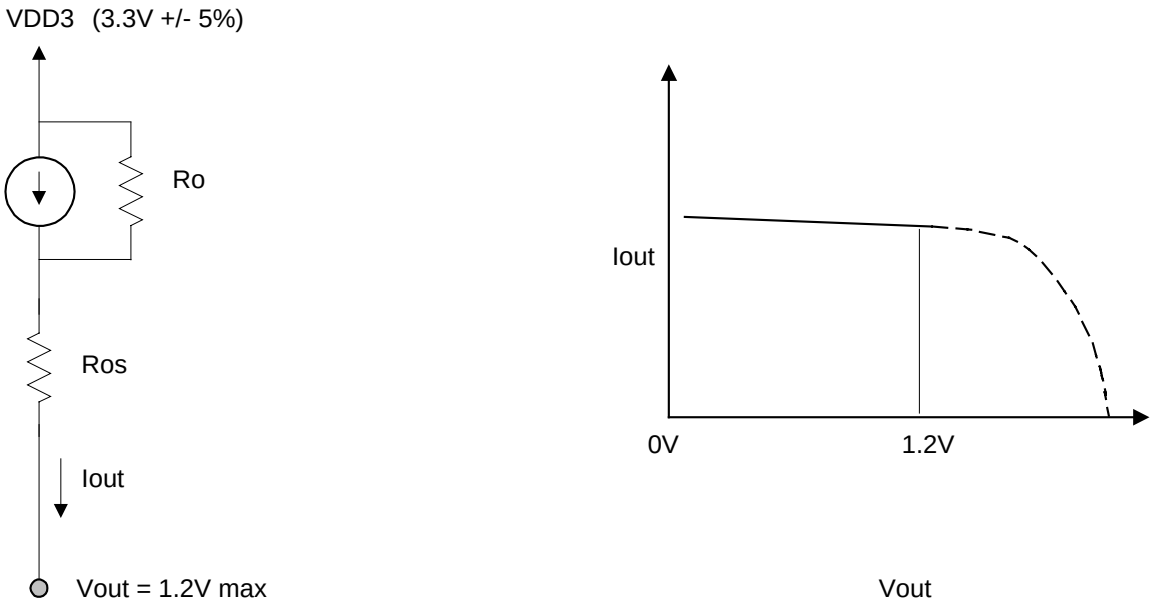


Figure 3

Host Clock (HCSL) Buffer Characteristics

Characteristic	Minimum	Maximum
Ro	3000 Ohms (recommended)	N/A
Ros	Unspecified	Unspecified
Vout	N/A	1.2 Volt

Iout is selectable depending on implementation. The parameters above apply to all configurations. Vout is the voltage at the pin of the device.

The various output current configurations are shown in the host swing select functions table. For all configurations, the deviation from the expected output current is +/- 7% as shown in the table current accuracy (page 12).

Current Accuracy

	Conditions	Configuration	Load	Min	Max
Iout	VDD = nominal (3.30V)	All combinations of M0, M1 and Rr shown in host Swing Select Function Table 5, p. 8	Nominal test load for given configuration	-7% Inom	+ 7% Inom
Iout	VDD = 3.30 +/- 5%	All combinations of M0, m1 and Rr shown in Host Swing Select Function Table 5, p. 8	Nominal test load for given configuration	-12% Inom	+ 12% Inom

Note: Inom refers to the expected current based on the configuration of the device.

Buffer Characteristics for REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-12		-53	mA	VOH=VDDmin-0.5V (2.64V)
Pull-Up Current Max	IOH_{max}	-27		-92	mA	VOH=VDDmin/2 (1.56V)
Pull-Down Current Min	IOL_{min}	9		27	mA	VOL=0.4V
Pull-Down Current Max	IOL_{max}	26		79	mA	VOL=VDDmin/2 (1.56V)
3.3V Output Rise Edge Rate	Trh	0.5	-	2.0	V/nS	3.3V +/- 5% @ 0.4V – 2.4 V
3.3V Output Fall Edge Rate	Tfh	0.5	-	2.0	V/nS	3.3V +/- 5% @ 2.4V – 0.4 V

Buffer Characteristics for 3V66, Mref, Mref_b

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-11		-83	mA	VOH=VDD-0.5V (2.64V)
Pull-Up Current Max	IOH_{max}	-30		-184	mA	V OH=VDD/2 (1.56V)
Pull-Down Current Min	IOL_{min}	9		38	mA	VOL=0.4V
Pull-Down Current Max	IOL_{max}	28		148	mA	VOL=VDD/2 (1.56V)
3.3V Output Rise Edge Rate	Trh	1/1	-	4/1	V/nS	3.3V +/- 5% @ 0.4V – 2.4 V
3.3V Output Fall Edge Rate	Tfh	1/1	-	4/1	V/nS	3.3V +/- 5% @ 2.4V – 0.4 V

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	14.17	14.31818	14.46	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
Frequency Stability	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

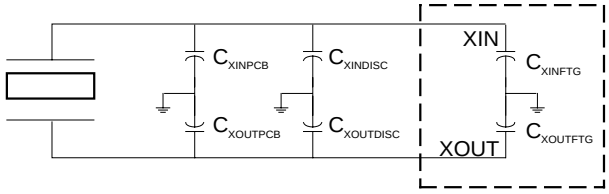
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit trace capacitance (C_{PCB}), and any onboard discrete load capacitance (C_{DISC}).

The following formula and schematic illustrates the application of the loading specification of a crystal (C_{XTAL})for a design.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground



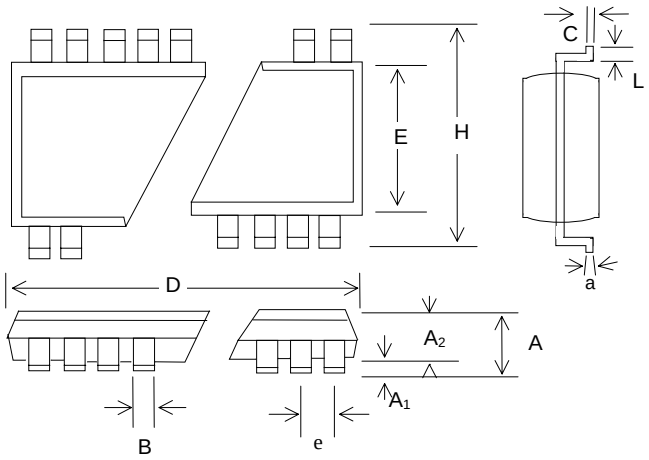
Clock Generator

As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 4pF (typical value) would calculate as:

$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF

Package Drawing and Dimensions (48 Pin TSSOP)



48 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.236	0.240	0.244	6.00	6.10	6.20
e	0.02 BSC			0.50 BSC		
H	0.315	0.319	0.323	8.00	8.10	8.20
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

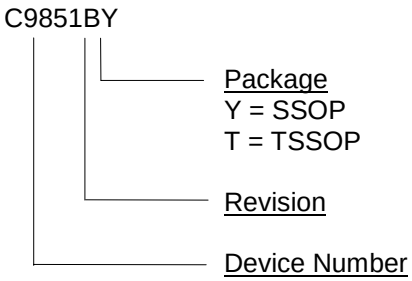
48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9851BY	48 Pin SSOP	Commercial, 0ºC to +70ºC
C9851BT	48 Pin TSSOP	Commercial, 0ºC to +70ºC

Marking: Example: Cypress
C9851
Date Code, Lot #



Notice

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**	107104	06/12/01	IKA	Convert from IMI to Cypress