CA-IF43232E 3V to 5.5V Two-Channel RS-232 Transceiver With ±15kV ESD Protection

1 Key Features

- Meets or Exceeds the Requirements of the TIA/EIA-232-F and ITU V.28 Standards
- Bus Pins (RINx and DOUTx) ESD Protection
  - ±15kV HBM ESD
  - ±8kV IEC 61000-4-2 Contact Discharge
  - ±15kV IEC 61000-4-2 Air-gap Discharge
- Operates With 3-V to 5.5-V VCC Supply
- Two Drivers and Two Receivers
- Maximum Data Rate: 250kbps
- Low Supply Current: 1mA (typical)
- Two Charge Pumps With External Capacitors: 4 × 0.1µF (VCC = 3.3V)
- Accepts 5-V Logic Input With 3.3-V Supply
- Extended Industrial Temperature Range: –40°C to 125°C

2 Applications

- Wired Networking
- Data center and Enterprise Computing
- Battery-Powered Systems
- Computer
- Printer

3 Description

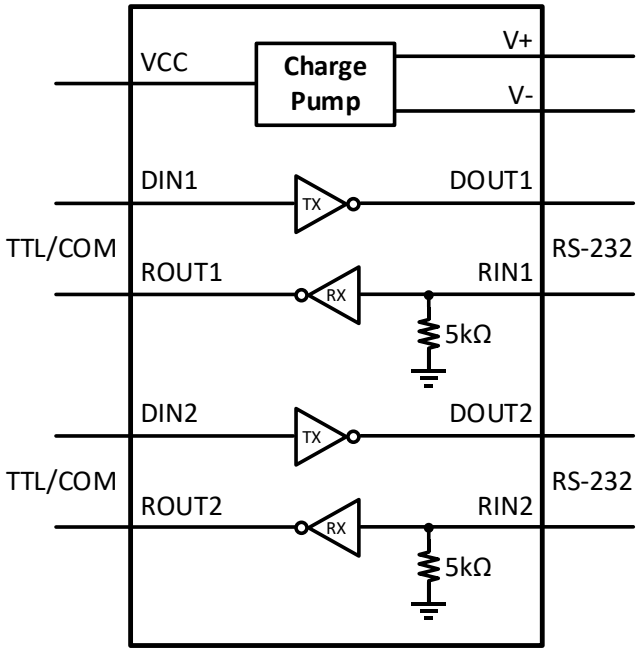
The CA-IF43232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit, which meets the requirements of the TIA/EIA-232-F and ITU V.28 standards and provides the electrical interface between an asynchronous communication controller and the serial-port connector. These devices have internal charge pumps with external capacitors could operate with 3-V to 5.5-V VCC supply. The CA-IF43232E devices operate at data signaling rates up to 250kbps and a maximum of 30-V/µs driver output (DOUT1/DOUT2) slew rate.

These devices could provide standard narrow-body SOIC16 and small-footprint TSSOP16 packages, and are specified over extended industrial temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IF43232EN	SOIC16-NB (N)	10.0mm × 3.9mm
CA-IF43232ETB	TSSOP16 (TB)	5mm × 4.4mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Number of Channels	Date Rate (kbps)	Package
CA-IF43232EN	2	250	SOIC16-NB (N)
CA-IF43232ETB	2	250	TSSOP16 (TB)

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5 Revision History

Revision	Description	Date	Page
Version 1.01	First English edition.	2024/12/06	All

6 Pin Descriptions and Functions

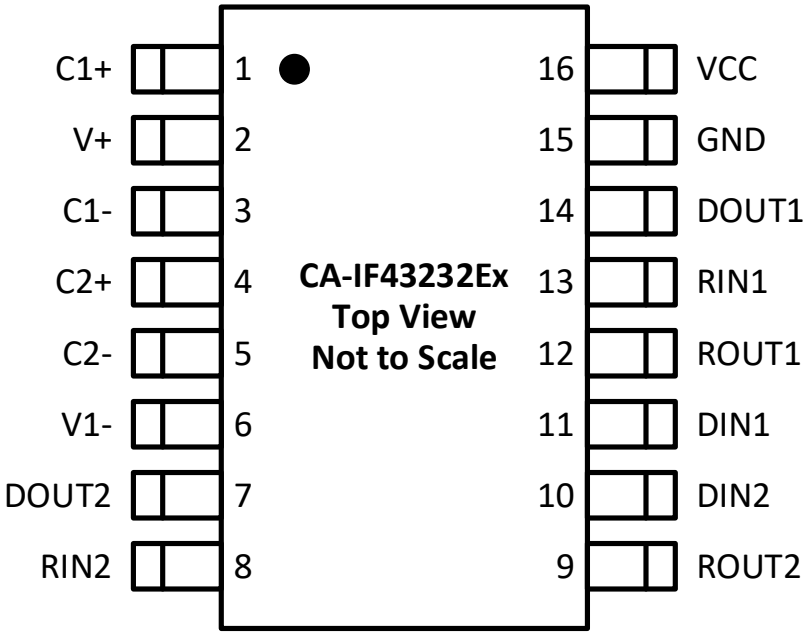


Figure 6-1 Pin Configuration

Table 6-1 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
C1+	1	Input/Output	Positive lead of C1 capacitor
V+	2	Output	Positive charge pump output for storage capacitor only
C1-	3	Input/Output	Negative lead of C1 capacitor
C2+	4	Input/Output	Positive lead of C2 capacitor
C2-	5	Input/Output	Negative lead of C2 capacitor
V-	6	Output	Negative charge pump output for storage capacitor only
DOUT2	7	Output	Second RS-232 line data output, cable side
RIN2	8	Input	Second RS-232 line data input, cable side
ROUT2	9	Output	Second logic data output, logical side
DIN2	10	Input	Second logic data input, logical side
DIN1	11	Input	First logic data input, logical side
ROUT1	12	Output	First logic data output, logical side
RIN1	13	Input	First RS-232 line data input, cable side
DOUT1	14	Output	First RS-232 line data output, cable side
GND	15	Ground	Ground
VCC	16	Supply	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER			MIN	MAX	UNIT
VCC	Supply voltage[2]		–0.3	6	V
V+	Positive charge pump output supply voltage[2]		–0.3	7	V
V+	Negative charge pump output supply voltage[2]		0.3	–7	V
(V+) –(V–)	Supply voltage difference[2]			13	V
V_I	Input voltage	DIN1, DIN2	–0.3	6	V
		RIN1, RIN2	–25	25	V
V_O	Output voltage	DOUT1, DOUT2	–13.2	13.2	V
		ROUT1, ROUT2	–0.3	V_{CC} + 0.3	
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature		–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the ground terminal (GND).

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins (RINx, DOUTx)	±15	kV
			All other pins	±2	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±1.5	
		Contact discharge, per IEC 61000-4-2	Bus pins (RINx, DOUTx[1, 2])	±8	kV
		Air-gap discharge, per IEC 61000-4-2		±15	

NOTE:

1. Minimum of 1-µF capacitor between VCC and GND is required to meet the specified IEC 61000-4-2 rating.
2. Place 150-pF capacitor between DOUTx and GND to meet the specified IEC 61000-4-2 rating.

7.3 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
VCC	Supply voltage, with respect to GND	VCC = 3.3V	3.0	3.3	3.6	V
		VCC = 5V	4.5	5.0	5.5	
V_I	Input voltage of RINx		–25		25	V
$1/t_{UI}$	Data Rate				250	kbps
T_A	Ambient Temperature		–40		125	°C
T_J	Junction Temperature		–40		150	°C

7.4 Thermal Information

THERMAL METRIC		PACKAGE		UNIT
		SOIC16-NB (N)	TSSOP16 (TB)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.2	115	°C/W

7.5 Electrical Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
I_{CC}	Supply current[1]	No load, VCC = 3.3V or 5V		1	2	mA
Driver						
V_{IH}	High-level input voltage on DINx	VCC = 3.3V	2		5.5	V
V_{IL}	Low-level input voltage on DINx		0		0.8	V
V_{IH}	High-level input voltage on DINx	VCC = 5V	2.4		5.5	V
V_{IL}	Low-level input voltage on DINx		0		0.8	V
I_{IH}	High-level input current on DINx	DINx = VCC		±0.01	±1	μA
I_{IL}	Low-level input current on DINx	DINx = GND		±0.01	±1	μA
V_{OH}	High-level output voltage on DOUTx	DOUT at R_L = 3kΩ to GND, DINx = GND	5	5.4		V
V_{OL}	Low-level output voltage on DOUTx	DOUT at R_L = 3kΩ to GND, DINx = VCC	–5	–5.4		V
I_{OS}	Short-circuit output current on DOUTx	VCC = 3.6V, DOUTx connects to GND		±35	±60	mA
		VCC = 5.5V, DOUTx connects to GND				
R_O	Output resistance on DOUTx	VCC = V+ = V– = 0V, V_O = ±2V	300	3M		Ω
Receiver						
V_{OH}	High-level output voltage on ROUTx	I_{OH} = –1mA	VCC – 0.6	VCC– 0.1		V
V_{OL}	Low-level output voltage on ROUTx	I_{OL} = 1.6mA		0.15	0.4	V
V_{IH}	Input threshold high voltage on RINx	VCC = 3.3V		1.6	2.2	V
		VCC = 5V		1.9	2.4	
V_{IL}	Input threshold low voltage on RINx	VCC = 3.3V	0.6	1.1		V
		VCC = 5V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IH} – V_{IL}) on RINx			0.5		V
R_I	Intput resistance on RINx	V_I = ±3V to ±25V	3	5	7	kΩ

NOTE:

1. Test conditions refer to the recommended configuration of charge pump capacitors in Application and Implementation.

7.6 Timing Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
t_{DPLH}	Driver propagation delay time, low- to high-level output	R_L = 7kΩ, C_L = 150pF, VCC = 3.3V, see Figure 8-1		380		ns
		R_L = 3kΩ, C_L = 1000pF, VCC = 3.3V, see Figure 8-1		680		
t_{DPHL}	Driver propagation delay time, high- to low-level output	R_L = 7kΩ, C_L = 150pF, VCC = 3.3V, see Figure 8-1		620		ns
		R_L = 3kΩ, C_L = 1000pF, VCC = 3.3V, see Figure 8-1		1080		
$t_{sk(p)}$	Driver pulse skew, $\lvert t_{DPLH} - t_{DPLH} \rvert$[1]	R_L = 3kΩ, C_L = 1000pF, VCC = 3.3V, see Figure 8-1		400		ns
SR(t_f/t_r)	Driver output slew rate	R_L = 3kΩ to 7kΩ, C_L = 150pF to 1000pF, VCC = 3.3V, see Figure 8-2	6	12	30	V/µs
		R_L = 3kΩ to 7kΩ, C_L = 150pF to 2500pF, VCC = 3.3V, see Figure 8-2	4	7	30	
Receiver						
t_{DPLH}	Receiver propagation delay time, low- to high-level output	C_L = 150pF, see Figure 8-3		150		ns
t_{DPHL}	Receiver propagation delay time, high- to low-level output			150		ns
$t_{sk(p)}$	Receiver pulse skew, $\lvert t_{RPLH} - t_{RPLH} \rvert$[1]			5		ns

NOTE:

1. For each channel of the same device.

8 Parameter Measurement Information

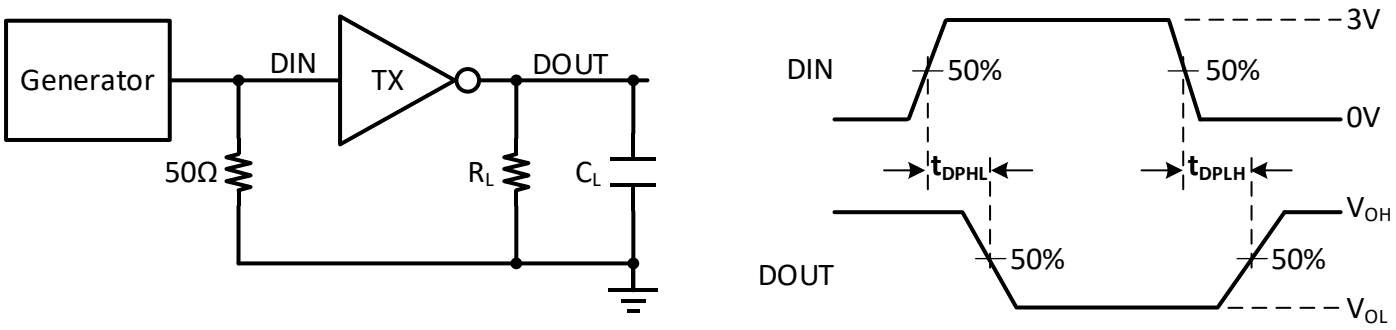


Figure 8-1 Measurement of Driver Propagation Delay

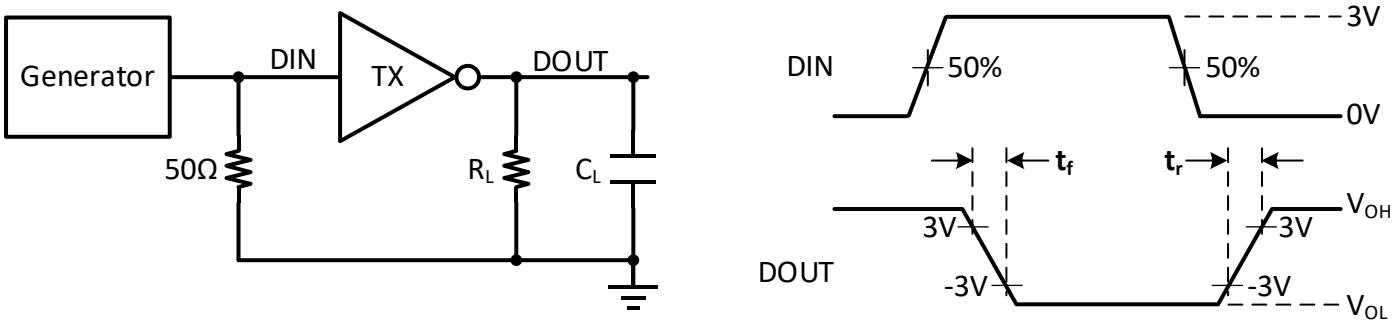


Figure 8-2 Measurement of Driver Output Rise/Fall Time

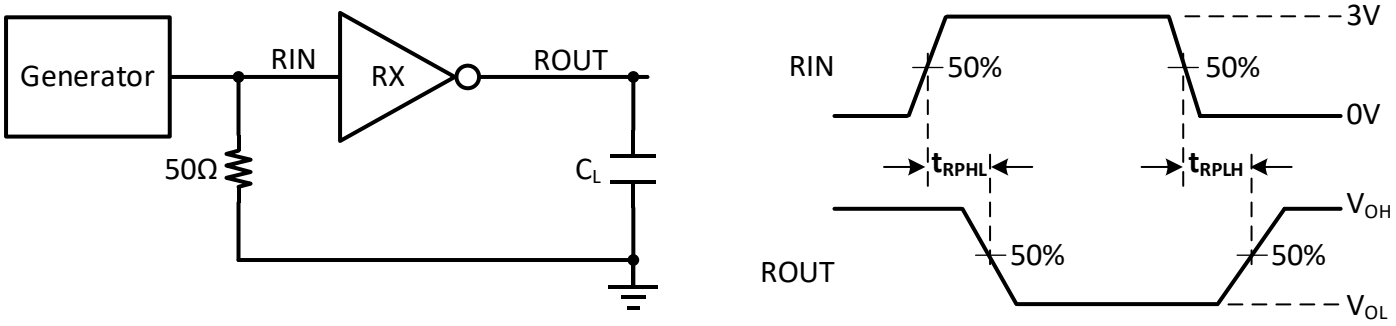


Figure 8-3 Measurement of Receiver Propagation Delay

NOTE:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 250kbps, 50% duty cycle, tr ≤ 10ns, tf ≤ 10ns. Since the output impedance of the signal generator (Zout) is 50Ω, the 50-Ω resistor in the figures is used to match and is not needed in practical applications.
2. C_L includes probe and fixture capacitance. Since the load capacitance affects the output rise/fall time, it is a key factor in the measurement of timing characteristics.

9 Detailed Description

9.1 Device Feature Description

The CA-IF43232E device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The device consists of two line drivers, two line receivers, and a dual charge-pump circuit.

The driver of CA-IF43232E converts TTL logic levels to the electrical levels compatible with the EIA/TIA-232 standard. The driver's input DINx does not have pull-up or pull-down resistor. Please connect DINx to GND or VCC when the driver is unused. It is forbidden to leave DINx floating.

The CA-IF43232E device have two independent receivers which convert RS-232 levels to standard logic levels. The typical value of receiver's input internal pull-down resistor is 5kΩ, thus ROUTx is logical high when the corresponding input of RINx is floating.

9.2 Device Function Mode

The truth table of driver is shown in Table 9-1. The truth table of receiver is shown in Table 9-2.

Table 9-1 Truth Table of Driver[1]

INPUT	OUTPUT
DINx[2]	DOUTx
L	H
H	L

NOTE:
1. H = high level, L = low level.
2. It is forbidden to leave DINx floating.

Table 9-2 Truth Table of Receiver[1]

INPUT	OUTPUT
RINx[2]	ROUTx
L	H
H	L
Open	H

NOTE:
1. H = high level, L = low level, Open = input disconnected or connected driver off.
2. RINx is internally pulled down to GND.

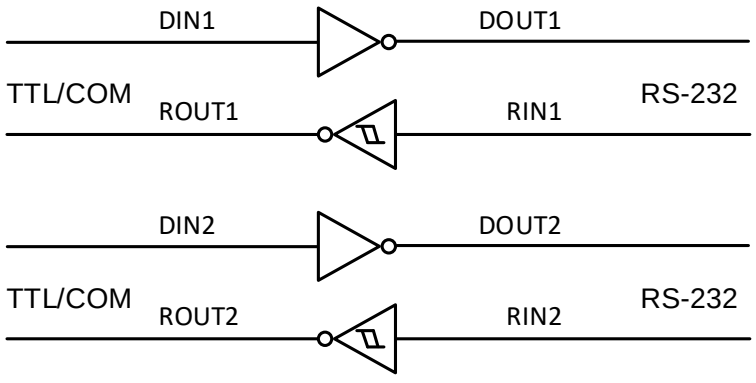


Figure 9-1 Logic Diagram of Driver and Receiver

10 Application and Implementation

ROUTx and DINx connect to logic lines from a UART or microcontroller. RINx and DOUTx connect to RS-232 connectors or cable. The typical application circuit is shown in Figure 10-1.

The CA-IF43232E has two internal charge pumps to support the level translation. The two charge pumps generate output voltages of+5.4V and –5.4V respectively when VCC ranges from 3.0V to 5.5V. Each charge pump requires a flying capacitor (C1/C2) and an energy storage capacitor (C3/C4) to generate stable V+ and V– with small ripples.

When VCC is 3.3V, the value of C1~C4 ranges from 0.1μF to 1μF and the recommended value is 0.1μF. When VCC is 5V, the value of C1 ranges from 0.047μF to 1μF and the recommended value is 0.1μF, while the value of C2~C4 ranges from 0.1μF to 2.2μF and the recommended value is 1μF.

Place the external capacitors as close to the corresponding pins as possible and keep the external capacitor traces short, specifically for C1 and C2.

The internal circuit and input threshold on DINx pin supports 5-V logic input with 3.3-V supply.

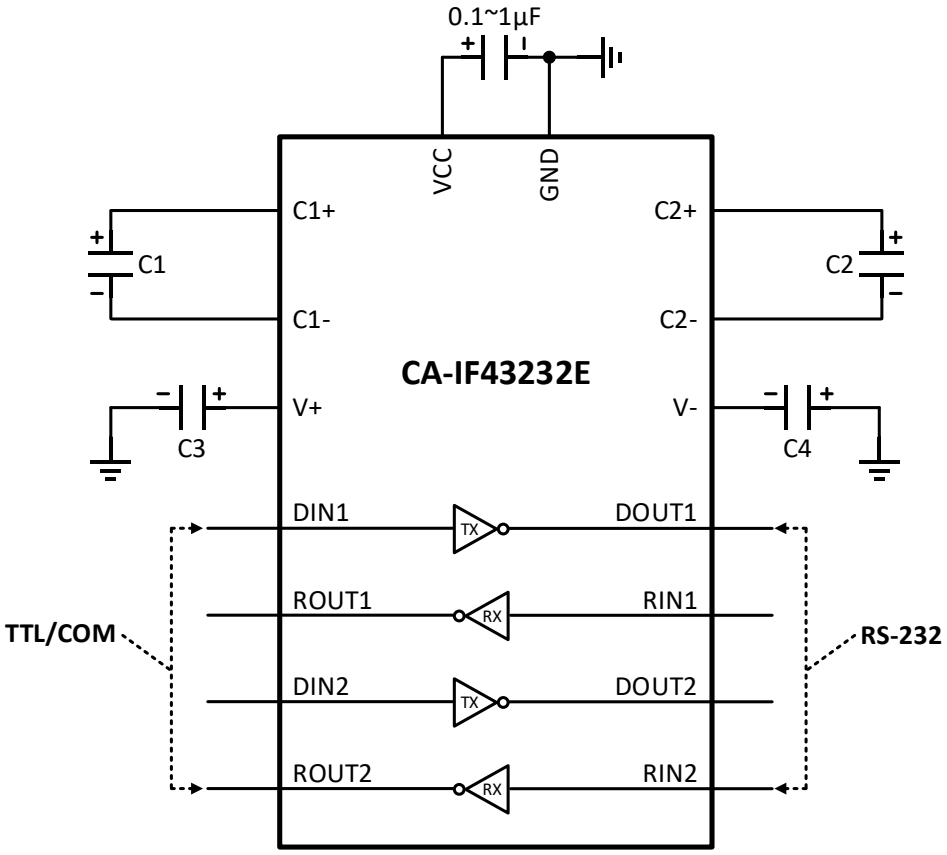


Figure 10-1 Typical Application Circuit

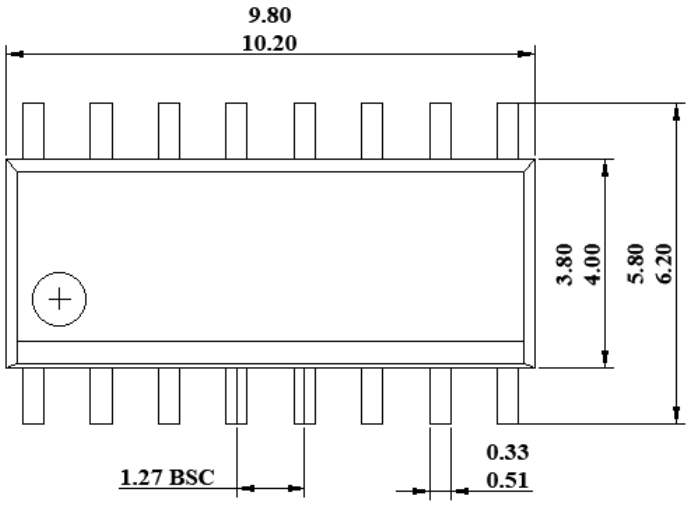
Table 10-1 Recommended Value for Charge Pump Capacitors

VCC	C1	C2~C4
3~3.6V	0.1μF	0.1μF
4.5~5.5V	0.1μF	1μF

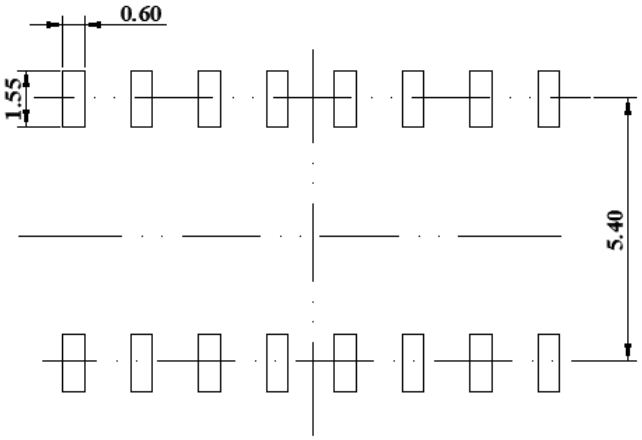
11 Package Information

11.1 SOIC16-NB Package

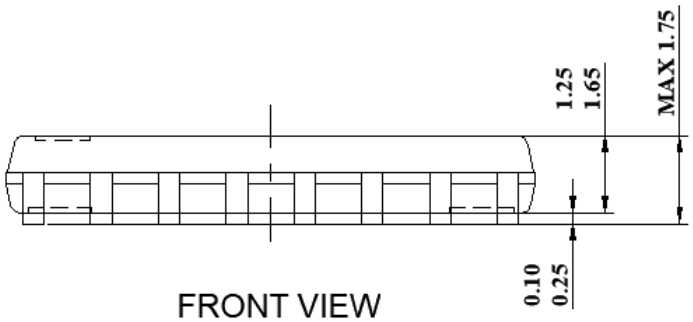
The values for the dimensions are shown in millimeters.



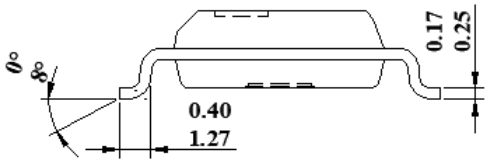
TOP VIEW



RECOMMENDED LAND PATTERN



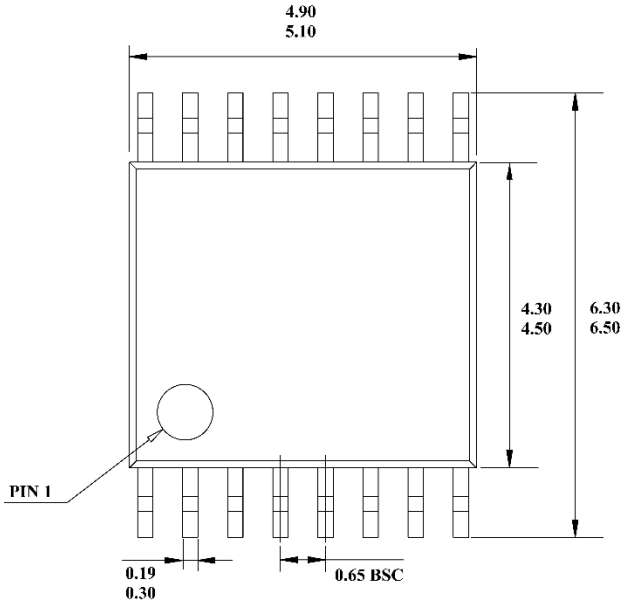
FRONT VIEW



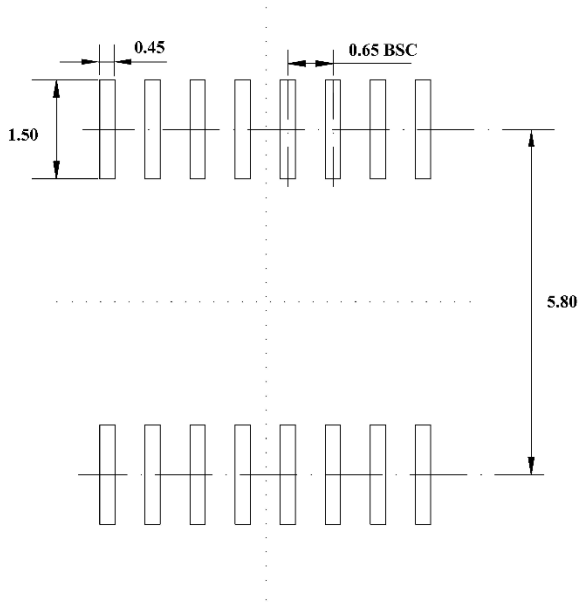
SIDE VIEW

11.2 TSSOP16 Package

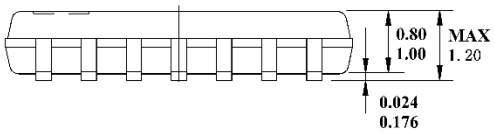
The values for the dimensions are shown in millimeters.



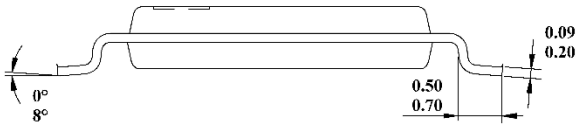
TOP VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW



LEFT VIEW

12 Soldering Information

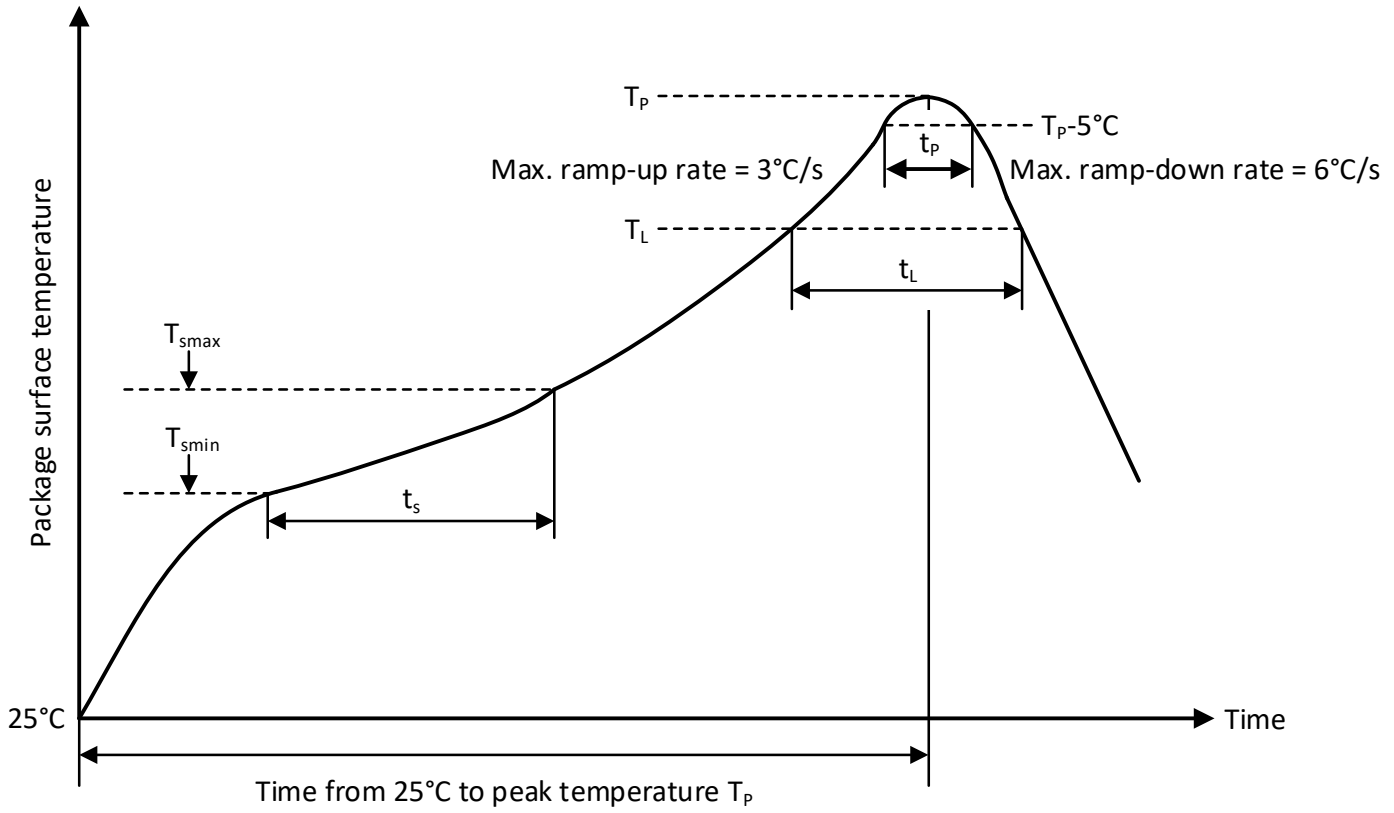


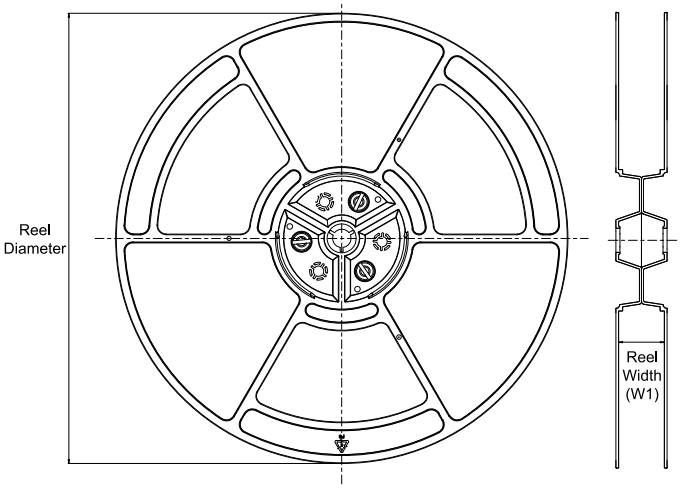
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

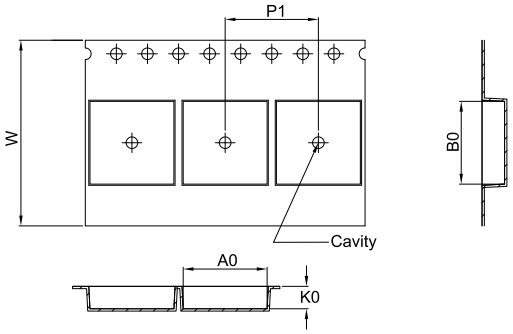
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

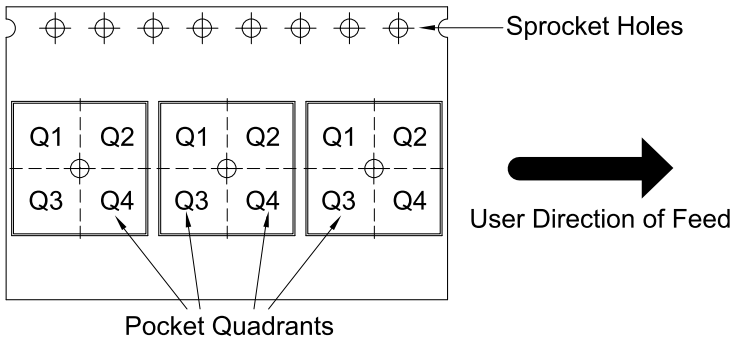


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF43232EN	SOIC	N	16	2500	330	16.4	6.4	10.3	2.1	8.0	16.0	Q1
CA-IF43232ETB	TSSOP	TB	16	4000	330	12.4	6.8	5.4	1.5	8.0	12.0	Q1

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