3.0V to 5.5V RS485/RS422 Transceivers with ±30kV ESD Protection

1. Features

- **High-Performance and Compliant with RS-485 EIA/ TIA-485 Standard**
  - Low EMI 500kbps Data Rate (CA-IF4805) and up to 50Mbps (CA-IF4850), 20Mbps (CA-IF4820) High-Speed Data Rates
  - 1/8 Unit Load Enables up to 256 Nodes on the Same Bus
- **Integrated Protection for Robust Communication**
  - ±30V Fault Protection Range on Driver Outputs/Receiver Inputs
  - ±15V Common-Mode Voltage Range
  - ±15kV Human Body Model ESD Protection for the Full-duplex Devices (CA-IF48xxFS/FM/FD)
  - ±30kV Human Body Model ESD Protection for the Half-duplex Devices (CA-IF48xxHS/HM/HD)
  - Short-Circuit Protection
  - Thermal Shutdown
  - True Fail-Safe Guarantees Known Receiver Output State
- **Low Power**
  - 960µA (max.) @ Receive Mode
  - Shutdown Current < 5µA
- **3V to 5.5V Supply Voltage Range**
- **Wide Operating Temperature Range: –40°C to 125°C**
- **8 pin SOIC, 8 pin MSOP and 8 pin DFN Packages**

2. Applications

- Motor Drive
- Factory Automation & Control
- Grid Infrastructure
- Home and Building Automation
- Video Surveillance
- Process Control
- Telecommunication Equipment

3. General Description

The CA-IF48xx family of devices are low-power transceivers for RS-485/RS-422 communications in harsh environments. All devices have ±30V fault protection for overvoltage conditions on the bus lines that ensure robust protection for the communication interface. They also feature ±15V wide common-mode range (CMR), this feature was specifically designed for systems where there is a large common-mode voltage present due to either nearby electrically noisy equipment or large ground differences due to different earth grounds or long distance transmission. The bus pins of these devices are protected against ±15kV (for the full-duplex transceivers) and ±30kV (for the half-duplex transceivers) electro-static discharge (ESD) shocks, eliminating the need for additional system level protection components.

The CA-IF48xx family of devices contains one driver(TX) and one receiver(RX), operates over the +3V to +5.5V supply range, making these devices convenient for designers to use one part with either +3.3V or +5V supply systems. The CA-IF48xxHS/HM/HD devices provide half-duplex transceivers, and the CA-IF48xxFS/FM/FD devices provide full-duplex transceivers. The CA-IF4820 and CA-IF4850 can transmit and receive at data rates up to 20Mbps and up to 50Mbps respectively, while the CA-IF4805 is specified for data rates up to 500kbps. These devices also include fail-safe circuitry, guaranteeing a logic-high receiver output when the receiver inputs are shorted or open.

All devices are specified over the -40°C to +125°C wide operating temperature range and are available in small 8-pin MSOP, 8-pin DFN packages for space constrained applications and 8-pin SOIC for drop-in compatibility.

Device Information

Part number	Package	Package size (NOM)
CA-IF48xxxS	SOIC8	3.9mm*4.9mm
CA-IF48xxxM	MSOP8	3mm*3mm
CA-IF48xxxD	DFN8	3mm*3mm

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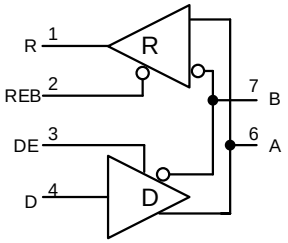
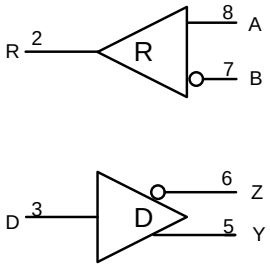
CA-IF4805H Simplified Block Diagram



CA-IF4820F Simplified Block Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part #	Full/Half-Duplex	Data Rate(Mbps)	Number of Nodes on Bus	Package
CA-IF4805HS	Half-Duplex	0.5	256	SOIC8
CA-IF4805FS	Full-Duplex	0.5	256	SOIC8
CA-IF4820HS	Half-Duplex	20	256	SOIC8
CA-IF4820FS	Full-Duplex	20	256	SOIC8
CA-IF4850HS	Half-Duplex	50	256	SOIC8
CA-IF4850FS	Full-Duplex	50	256	SOIC8
CA-IF4805HM	Half-Duplex	0.5	256	MSOP8
CA-IF4805FM	Full-Duplex	0.5	256	MSOP8
CA-IF4820HM	Half-Duplex	20	256	MSOP8
CA-IF4820FM	Full-Duplex	20	256	MSOP8
CA-IF4850HM	Half-Duplex	50	256	MSOP8
CA-IF4850FM	Full-Duplex	50	256	MSOP8
CA-IF4805HD	Half-Duplex	0.5	256	DFN8
CA-IF4805FD	Full-Duplex	0.5	256	DFN8
CA-IF4820HD	Half-Duplex	20	256	DFN8
CA-IF4820FD	Full-Duplex	20	256	DFN8
CA-IF4850HD	Half-Duplex	50	256	DFN8
CA-IF4850FD	Full-Duplex	50	256	DFN8

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Table of Contents

1. Features....1
2. Applications....1
3. General Description....1
4. Ordering Information....2
5. Revision History....3
6. Pin Configuration and Descriptions....4
6.1. CA-IF48xxHS/CA-IF48xxHD/CA-IF48xxHM half-duplex transceivers....4
6.2. CA-IF48xxFS/CA-IF48xxFD/CA-IF48xxFM full-duplex transceivers....5
7. Specification....6
7.1. Absolute Maximum Ratings[1]....6
7.2. ESD Ratings....6
7.3. Recommended Operating Conditions....6
7.4. Thermal Information....6
7.5. Electrical Characteristics....7
7.6. Switching Characteristics....9
7.7. Typical Characteristics: all devices....11
7.8. Typical Characteristics for the CA-IF4805....13
7.9. Typical Characteristics for the CA-IF4820 and CA-IF4850 14
8. Parameter Measurement Information....15
9. Detailed Description....17
9.1. Overview....17
9.2. Device Functional Modes....17
9.2.1. Device Function Modes for the CA-IF48xxHS/HM/HD....17
9.2.2. Device Function Modes for the CA-IF48xxFS/FM/FD....18
10. Application Information....19
11. Package Information....20
11.1. SOIC8 Package Outline....20
11.2. MSOP8 Package Outline....21
11.3. DFN8 Package Outline....22
12. Soldering Temperature (reflow) Profile....23
13. Tape and Reel Information....24
14. Important statement....25

5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	Update the Package ,Tape and Reel Information	22,24

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6. Pin Configuration and Descriptions

6.1. CA-IF48xxHS/CA-IF48xxHD/CA-IF48xxHM half-duplex transceivers

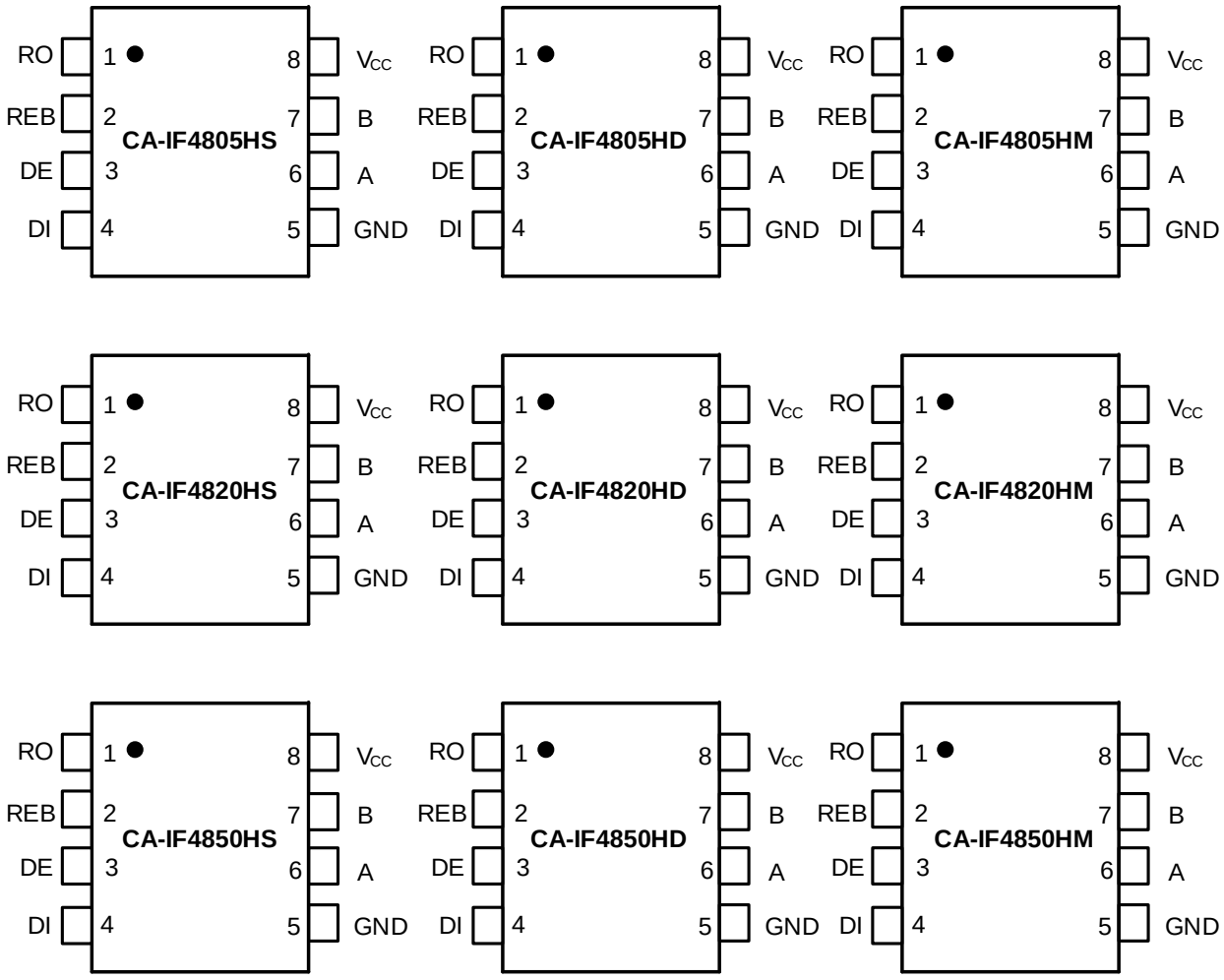

Figure 6-1. CA-IF48xxHS/ CA-IF48xxHD/CA-IF48xxHM pin configuration

Table 6-1 CA-IF48xxHS/ CA-IF48xxHD/ CA-IF48xxHM pin description

Pin Name	Pin Number	Description
RO	1	Receiver data output. With REB low, RO is high when (V_A –V_B) > V_{TH+} and is low when (V_A – V_B) < V_{TH-}. RO is high impedance when REB is high. See *Table 9-2* for details.
REB	2	Receiver output enable. Drive REB low or connect to GND to enable RO. Drive REB high to disable the receiver and put RO in high impedance. Drive REB high and DE low to force the IC into low-power shutdown mode.
DE	3	Driver output enable. Drive DE high to enable the driver. Drive DE low or connect to GND to disable the driver. Drive REB high and DE low to force the IC into low-power shutdown mode.
DI	4	Driver data input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low. See *Table 9-1* for details.
GND	5	Ground.
A	6	Noninverting RS-485/RS-422 driver output/receiver input.
B	7	Inverting RS-485/RS-422 driver output/receiver input.
V_{CC}	8	Power supply input. Bypass V_{CC} to GND with at least 0.1μF capacitor as close to the device as possible.

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6.2. CA-IF48xxFS/CA-IF48xxFD/CA-IF48xxFM full-duplex transceivers

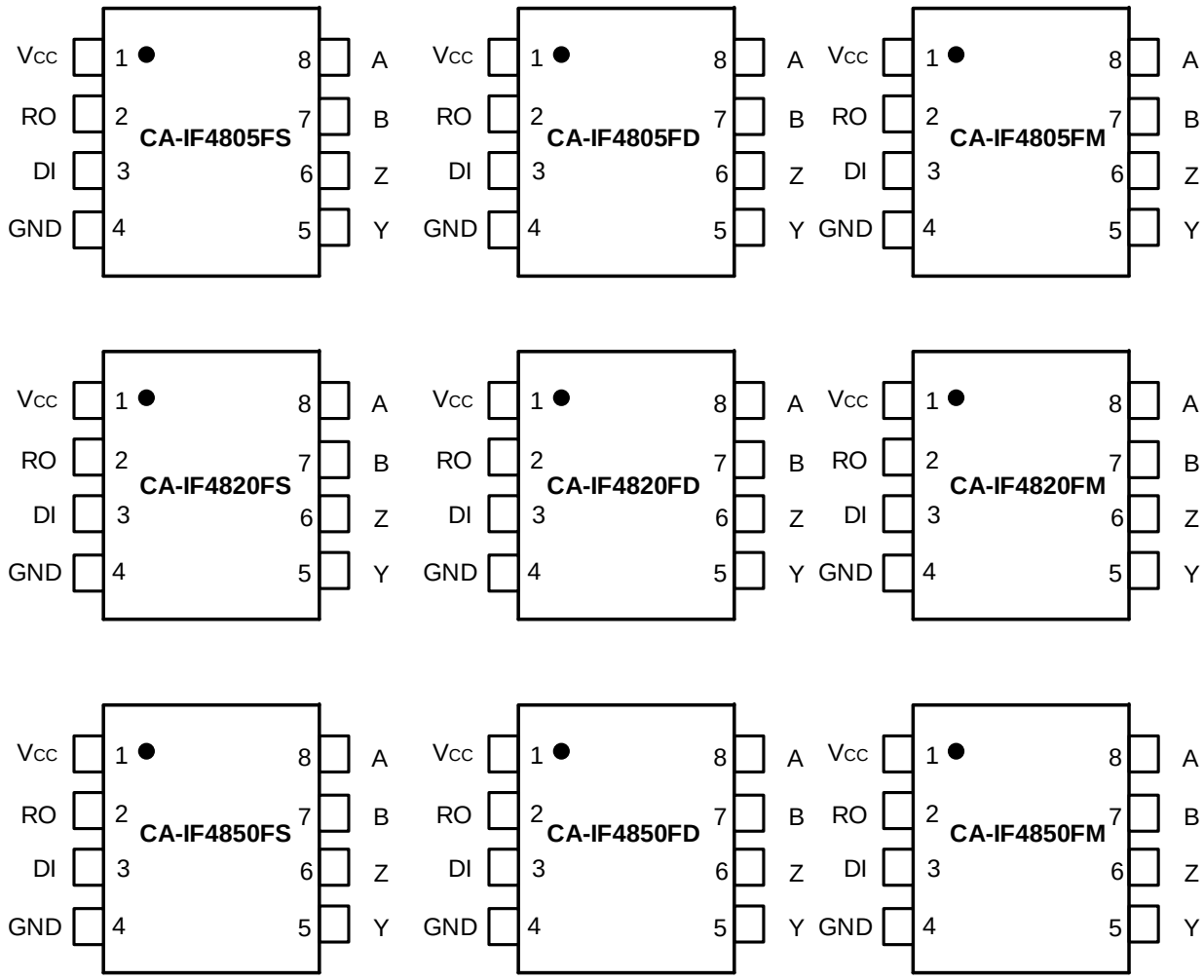

Figure 6-2. CA-IF48xxFS/CA-IF48xxFD/CA-IF48xxFM pin configuration

Table 6-2. CA-IF48xxFS/CA-IF48xxFD/CA-IF48xxFM pin description

Pin Name	Pin Number	Description
V_{CC}	1	Power supply input. Bypass V_{CC} to GND with at least 0.1μF capacitor as close to the device as possible.
RO	2	Receiver data output. RO is high when (V_A –V_B) > V_{TH+} and is low when (V_A – V_B) < V_{TH-}. See *Table 9-4* for details.
DI	3	Driver data input. A logic low on DI forces the noninverting output (Y) low and the inverting output (Z) high; a logic high on DI forces the noninverting output high and the inverting output low. See *Table 9-3* for details.
GND	4	Ground.
Y	5	Noninverting RS-485/RS-422 driver output.
Z	6	Inverting RS-485/RS-422 driver output.
B	7	Inverting RS-485/RS-422 receiver input.
A	8	Noninverting RS-485/RS-422 receiver input.

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7. Specification

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{CC}	Power supply voltage	-0.3	7.0	V
A, B, Y, Z	Voltage on the bus	-30	30	V
DE, DI, REB	Logic control voltage	-0.3	7.0	V
RO	Logic voltage at RO	-0.3	V_{CC}+0.3	V
T_J	Junction temperature	150		℃
T_{STG}	Storage temperature range	-65	150	℃

Note:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

Parameters			Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, bus pins[1]	CA-IF48xxF Full-duplex devices	±15	kV
		CA-IF48xxH Half-duplex devices	±30	kV
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins[1]		±6	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]		±2	kV

Note:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

	Parameters	Minimum value	Typical value	Maximum value	Unit
V_{CC}	Power supply	3	3.3/5.0	5.5	V
V_{IN}	Input voltage at any bus terminal	-15		15	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2		V_{CC}	V
R_L	Differential load resistance	54			Ohm
$1/t_{UI}$	Signaling rate：CA-IF4805			500	kbps
$1/t_{UI}$	Signaling rate：CA-IF4820			20	Mbps
$1/t_{UI}$	Signaling rate：CA-IF4850			50	Mbps
T_A	Operating ambient temperature	-40		125	℃
T_J	Junction temperature	-40		150	℃

7.4. Thermal Information

THERMAL METRIC		CA-IF48xxHS/FS SOIC8	CA- IF48xxHM/FD MSOP8	CA- IF48xxHM/FD DFN8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	160	45	℃/W

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7.5. Electrical Characteristics

All typical specs are at V_{CC} = 5V, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions		Minimum value	Typical value	Maximum value	Unit
Driver							
$\|V_{OD}\|$	Differential output voltage	V_{CC}=3.3V, R_L =60 Ω, -15 V ≤ V_{test} ≤ 15 V (see Figure 8-1)(1)		1.5	2.4		V
		R_L =60 Ω, -15 V ≤ V_{test} ≤ 15 V , 4.5 V ≤ V_{CC} ≤ 5.5 V (see Figure 8-1)		2.1			V
		Vcc=5.0V, R_L = 100 Ω (see Figure 8-2)		2	4		V
		Vcc=3.3V, R_L = 100 Ω (see Figure 8-2)		1.5	2.7		V
		Vcc=5.0V, R_L = 54 Ω (see Figure 8-2)		1.5	3.7		V
		Vcc=3.3V, R_L = 54 Ω (see Figure 8-2)		1.5	2.4		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	V_{CC}=3.3V/5.0V ,R_L = 54 Ω (see Figure 8-2)		-200		200	mV
V_{OC}	Common-mode output voltage			1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
I_{OS}	Short-circuit output current	V_{CC}=3.3V/5.0V ,DE = V_{CC}, -7 V ≤ V_O ≤ 12 V		-250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} = 0V/3.3V/5.0V	V_I = 12V		75	125	μA
			V_I = -7V	-100	-43		μA
		DE = 0 V, V_{CC} = 0V/3.3V/5.0V	V_I = 15V		91	125	μA
			V_I =-15V	-200	-97		μA
V_{TH+}	Receiver differential threshold voltage rising	V_{CC} = 3.3V/5.0V, Over common-mode range			-100	-20	mV
V_{TH-}	Receiver differential threshold voltage falling			-200	-130		mV
V_{HYS}	Receiver input hysteresis				30		mV
V_{OH}	Output high voltage	V_{CC} = 3.3V/5.0V, I_{OH} = -4 mA		V_{CC}-0.4	V_{CC}-0.2		V
V_{OL}	Output low voltage	V_{CC} = 3.3V/5.0V, I_{OL} = 4 mA			0.2	0.4	V
I_{OZR}	Output high-impedance current	V_{CC} = 3.3V/5.0V, V_O = 0 V or V_{CC}, REB= V_{CC}		-1		1	μA
Input Logic							
I_{IN}	Logic Input current	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}		-6.2		6.2	μA
Device							
I_{CC}	Supply current (quiescent)	V_{CC}=5.0V, Driver and receiver enabled REB=0V, DE = V_{CC}, No load		0.4	0.8	1.2	mA
		V_{CC}=3.3V, Driver and receiver enabled REB=0V, DE = V_{CC}, No load			0.7	1.1	mA
		V_{CC}=5.0V, Driver enabled, receiver Disabled REB=V_{CC}, DE = V_{CC}, No load			0.8	1.2	mA
		V_{CC}=3.3V, Driver enabled, receiver Disabled REB=V_{CC}, DE = V_{CC}, No load			0.7	1.1	mA
		V_{CC}=5.0V, Driver disabled, receiver enabled REB=0V, DE = 0V, No load			700	960	μA
		V_{CC}=3.3V, Driver disabled, receiver enabled REB=0V, DE = 0V, No load			700	960	μA
		V_{CC}=5.0V, Driver and receiver disabled REB=V_{CC}, DE = 0V, D=open, No load			2.9	5	μA
		V_{CC}=3.3V, Driver and receiver disabled REB=V_{CC}, DE = 0V, D=open, No load			1.6	3	μA

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T_{SD}	Thermal shutdown temperature		180	°C

Notes:

1. $|V_{OD}| \geq 1.4$ V with $T_A > 85°C$, $V_{test} < -7$ V and $V_{CC} < 3.135$ V.
2. Under any condition, ensure that V_{TH+} is at least V_{HYS} higher than V_{TH-}.

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7.6. Switching Characteristics

All typical specs are at V_{CC} = 5V, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter		Test Conditions	Minimum value	Typical value	Maximum value	Unit
Driver: CA-IF4805HS/ CA-IF4805HM/ CA-IF4805HD						
t_r, t_f	Driver differential output rise/fall time	V_{CC}=5.0 V R_L = 54 Ω, C_L = 50 pF, see Figure 8-3	250	360	680	ns
t_{PHL},t_{PLH}	Propagation delay			280	500	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				10	ns
t_r, t_f	Driver differential output rise/fall time	V_{CC}=3.3 V, R_L = 54 Ω, C_L = 50 pF, see Figure 8-3	240	350	670	ns
t_{PHL},t_{PLH}	Propagation delay			280	500	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				10	ns
t_{PHZ},t_{PLZ}	Disable time	see Figure 8-4, Figure 8-5		10	200	ns
t_{PZH},t_{PZL}	Enable time	REB = 0V, see Figure 8-4, Figure 8-5		100	600	ns
		REB = V_{CC}, see Figure 8-4, Figure 8-5		7.2	11	us
Receiver: CA-IF4805HS/ CA-IF4805HM/ CA-IF4805HD						
t_r, t_f	Output rise/fall time	V_{CC}=3.3 V/5.0 V, C_L = 15 pF, see Figure 8-6		3.8	10	ns
t_{PHL},t_{PLH}	Propagation delay			23	110	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time	see Figure 8-7, Figure 8-8		7	20	ns
$t_{PZH(1)}$,$t_{PZL(1)}$, $t_{PZH(2)}$,$t_{PZL(2)}$,	Enable time	DE = V_{CC}, see Figure 8-7, Figure 8-8		8	20	ns
		DE = 0 V, see Figure 8-7, Figure 8-8		7	14	µs
Driver: CA-IF4805FS/ CA-IF4805FM/ CA-IF4805FD						
t_r, t_f	Driver differential output rise/fall time	V_{CC}=5.0 V R_L = 54 Ω, C_L = 50 pF, see Figure 8-3	250	360	680	ns
t_{PHL},t_{PLH}	Propagation delay			280	500	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				10	ns
t_r, t_f	Driver differential output rise/fall time	V_{CC}=3.3 V R_L = 54 Ω, C_L = 50 pF, see Figure 8-3	240	350	670	ns
t_{PHL},t_{PLH}	Propagation delay			280	500	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				10	ns
Receiver: CA-IF4805FS/ CA-IF4805FM/ CA-IF4805FD						
t_r, t_f	Output rise/fall time	V_{CC}=3.3 V/5.0 V C_L = 15 pF, see Figure 8-6		3.8	10	ns
t_{PHL},t_{PLH}	Propagation delay			23	110	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				7	ns
Driver: CA-IF4820HS/CA-IF4820HM/CA-IF4820HD/ CA-IF4850HS/CA-IF4850HM/CA-IF4850HD						
t_r, t_f	Driver differential output rise/fall time	V_{CC}=3.3 V/5.0 V R_L = 54 Ω, C_L = 50 pF, see Figure 8-3	1	3	6	ns
t_{PHL},t_{PLH}	Propagation delay		3	10	20	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				3.5	ns
t_{PHZ},t_{PLZ}	Disable time	see Figure 8-4, Figure 8-5. V_{CC}=3.3 V/5.0 V		15	25	ns
t_{PZH},t_{PZL}	Enable time	REB = 0V, see Figure 8-4, Figure 8-5. V_{CC}=3.3 V/5.0 V		20	50	ns
		REB = V_{CC}, see Figure 8-4, Figure 8-5. V_{CC}=3.3 V/5.0 V		2.5	10	µs
Receiver: CA-IF4820HS/CA-IF4820HM/CA-IF4820HD/ CA-IF4850HS/CA-IF4850HM/CA-IF4850HD						
t_r, t_f	Output rise/fall time	V_{CC}=3.3 V/5.0 V, C_L = 15 pF, see Figure 8-6		3.8	10	ns
t_{PHL},t_{PLH}	Propagation delay			23	110	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time	see Figure 8-7, Figure 8-8. V_{CC}=3.3 V/5.0 V		7	20	ns

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$t_{PZH(1)}$,$t_{PZL(1)}$, $t_{PZH(2)}$,$t_{PZL(2)}$,	Enable time	DE = V_{CC}, see Figure 8-7, Figure 8-8. V_{CC}=3.3 V/5.0 V		8	20	ns
		DE = 0 V, see Figure 8-7, Figure 8-8. V_{CC}=3.3 V/5.0 V		7	14	µs
Driver: CA-IF4820FS/CA-IF4820FM/CA-IF4820FD/CA-IF4850FS/ CA-IF4850FM/CA-IF4850FD						
t_r, t_f	Driver differential output rise/fall time	V_{CC}=3.3 V/5.0 V ,R_L = 54 Ω, C_L = 50 pF, see Figure 8-3	1	3	6	ns
t_{PHL},t_{PLH}	Propagation delay		3	10	20	ns
$t_{SK(P)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				3.5	ns
Receiver: CA-IF4820FS/CA-IF4820FM/CA-IF4820FD/CA-IF4850FS/ CA-IF4850FM/CA-IF4850FD						
t_r, t_f	Output rise/fall time	V_{CC}=3.3 V/5.0 V ,C_L = 15 pF, see Figure 8-6		2	6	ns
t_{PHL},t_{PLH}	Propagation delay			25	40	ns
$t_{SK(P)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				3.5	ns

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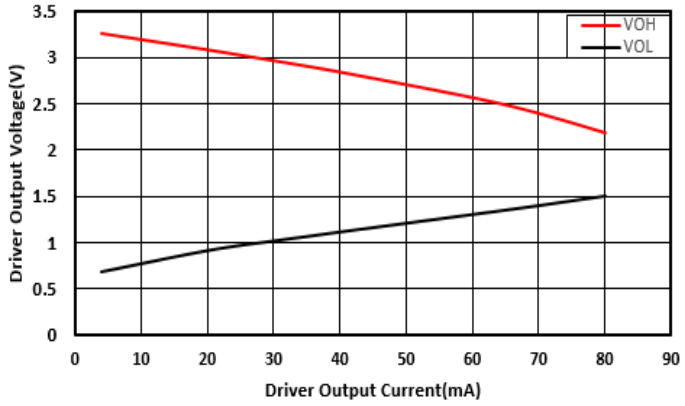
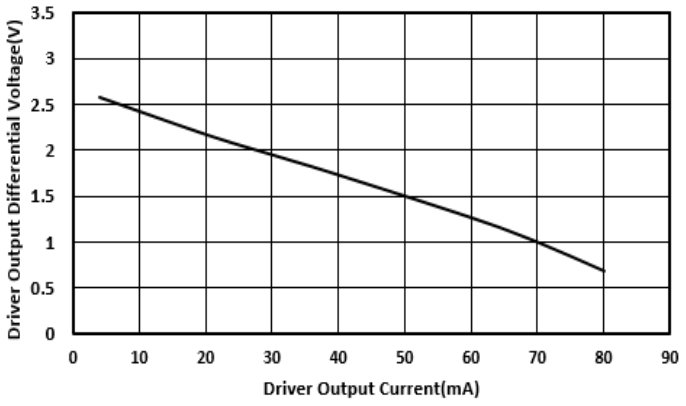
7.7. Typical Characteristics: all devices



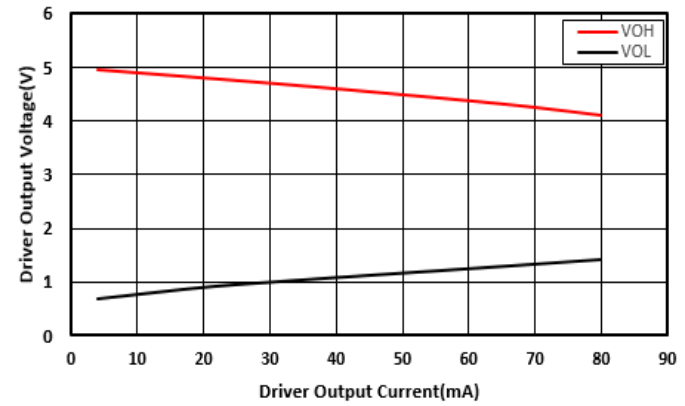
VCC=3.3V DE=VCC DI=0V

Figure 7-1 Driver Output Voltage vs Driver Output Current



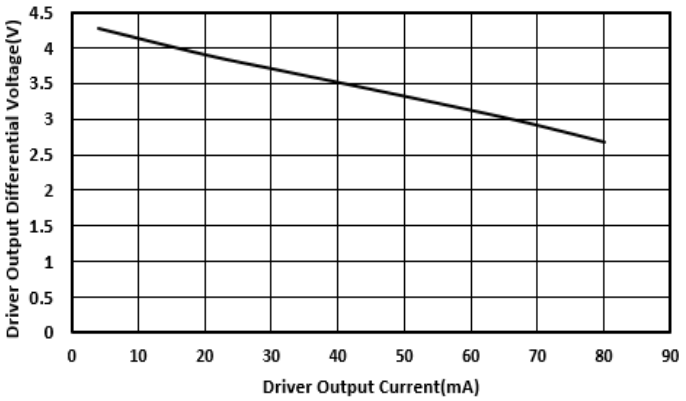
VCC=3.3V DE=VCC DI=0V

Figure 7-2 Driver Differential Output Voltage vs Driver Output Current



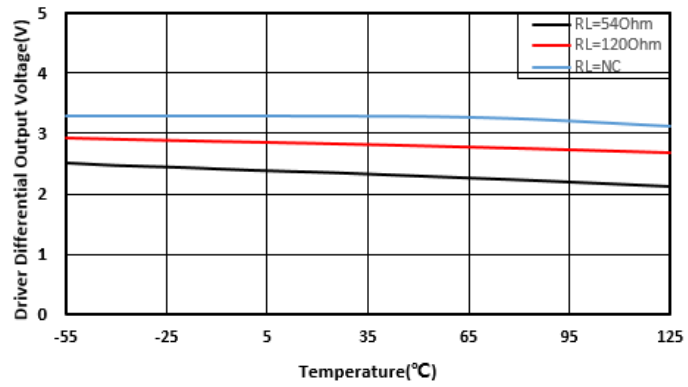
VCC=5V DE=VCC DI=0V

Figure 7-3 Driver Output Voltage vs. Driver Output Current



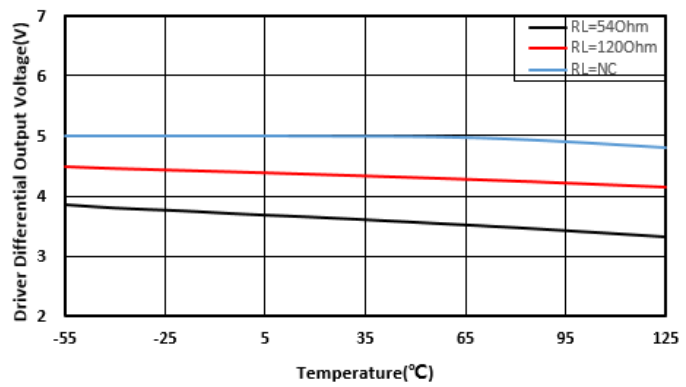
VCC=5V DE=VCC DI=0V

Figure 7-4 Driver Differential Output Voltage vs. Driver Output Current



V_{CC}=3.3V

Figure 7-5 Driver Differential Output Voltage vs. Temperature



V_{CC}=5V

Figure 7-6 Driver Differential Output Voltage vs. Temperature

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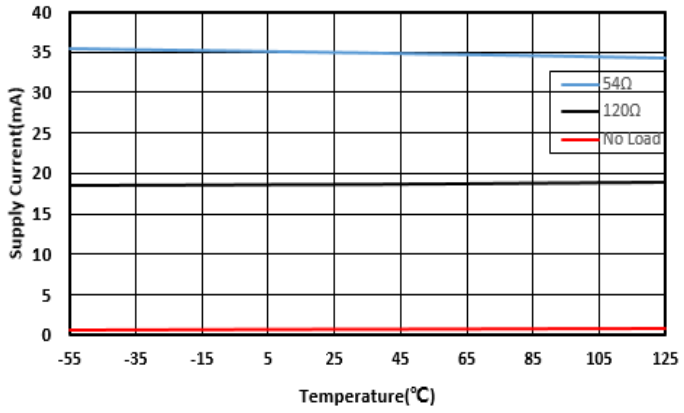
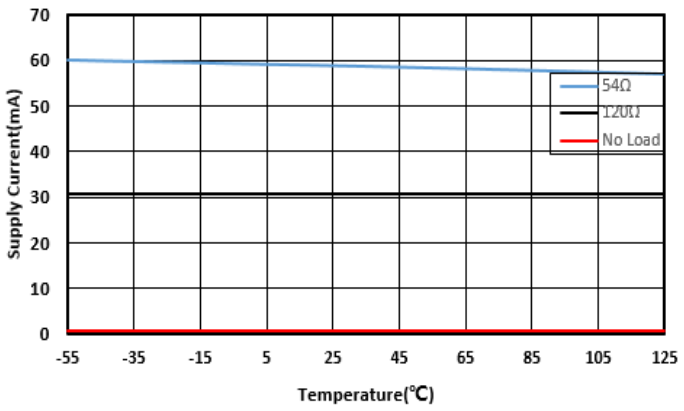
Typical Characteristics: all devices(continued)



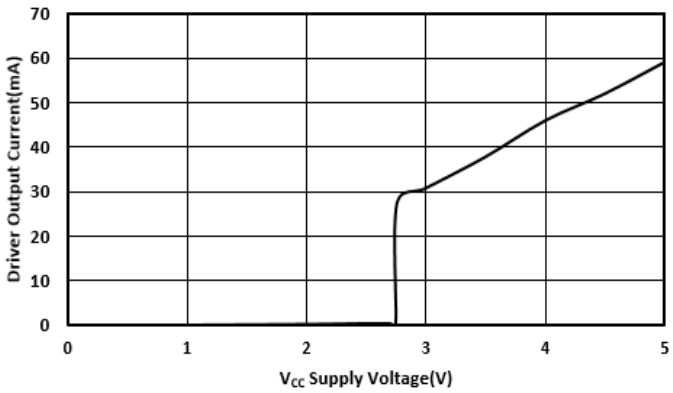
V_{CC}=3.3V DI=VCC

Figure 7-7 Quiescent Current vs. Temperature



V_{CC}=5V DI=VCC

Figure 7-8 Quiescent Current vs. Temperature



T_A=25℃ DE=VCC R_L=54Ω

Figure 7-9 Driver Output Current vs. Supply Voltage

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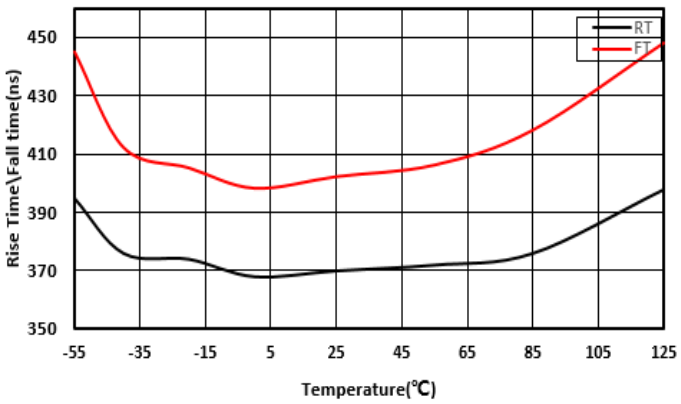
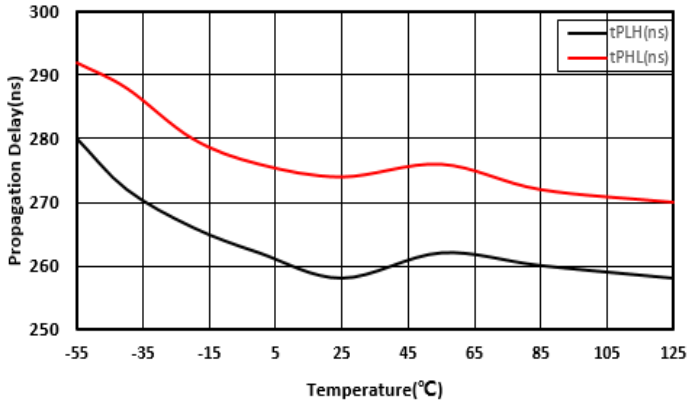
7.8. Typical Characteristics for the CA-IF4805



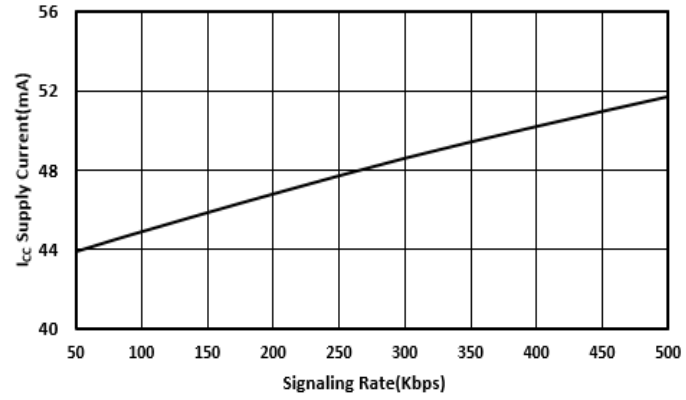
V_{CC}=3.3V

Figure 7-10 Driver Output Rise Time/Fall Time vs. Temperature



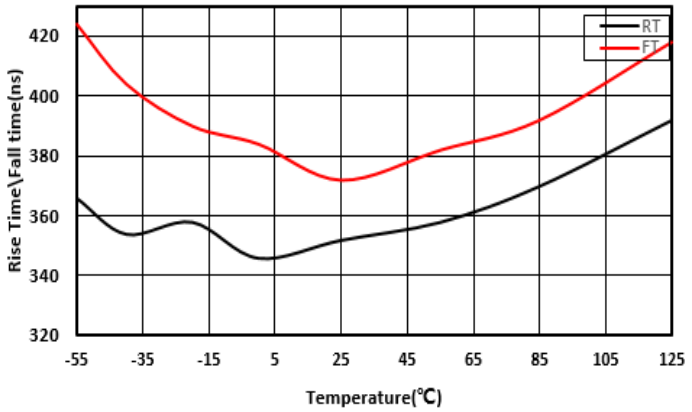
V_{CC}=3.3V

Figure 7-11 Driver Propagation Delay vs. Temperature



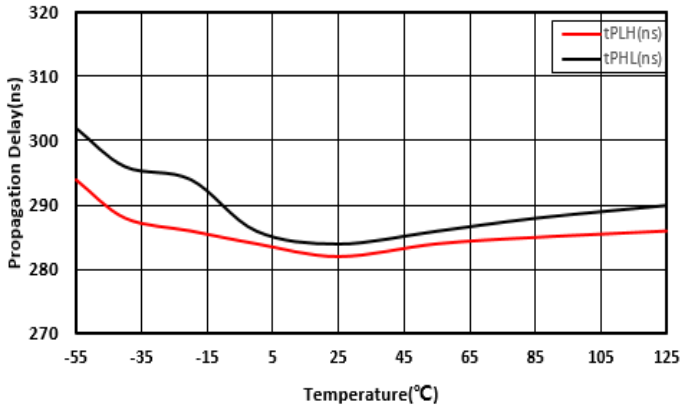
T_A=25℃ VCC =3.3V R_L=54Ω

Figure 7-12 Supply Current vs. Signal Rate



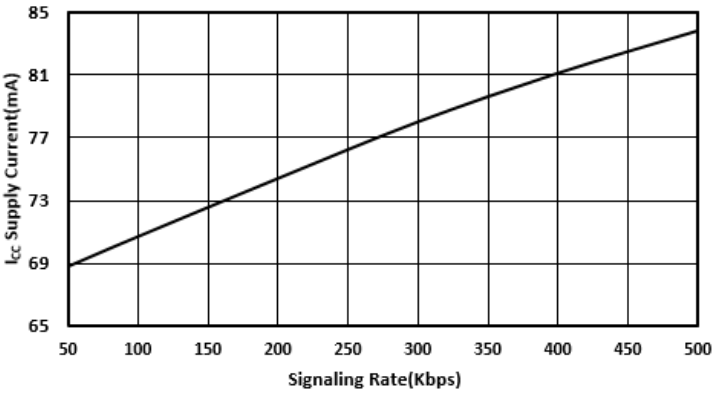
V_{CC}=5V

Figure 7-13 Driver Output Rise Time\Fall Time vs. Temperature



V_{CC}=5V

Figure 7-14 Driver Propagation Delay vs. Temperature



T_A=25℃ VCC =5V R_L=54Ω

Figure 7-15 Supply Current vs. Signal Rate

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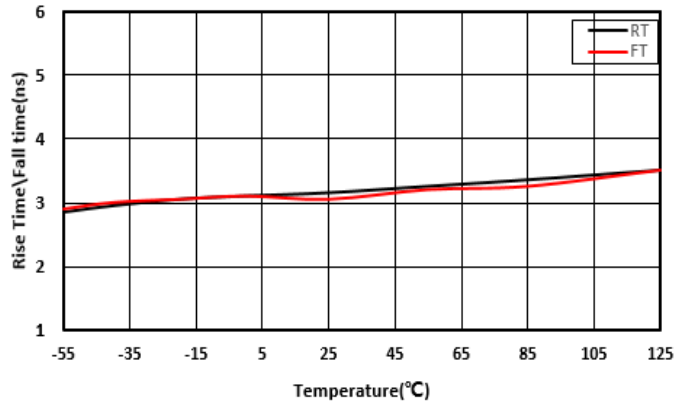
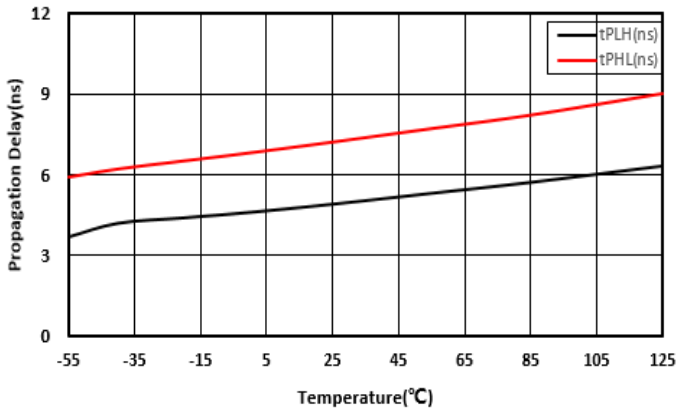
7.9. Typical Characteristics for the CA-IF4820 and CA-IF4850



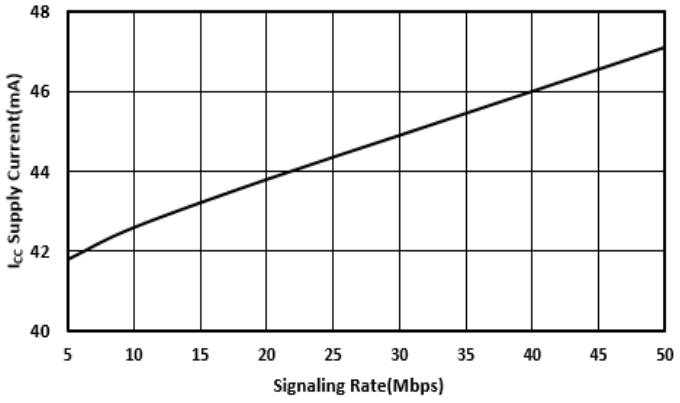
V_{CC}=3.3V

Figure 7-16 Driver Output Rise Time\Fall Time vs. Temperature



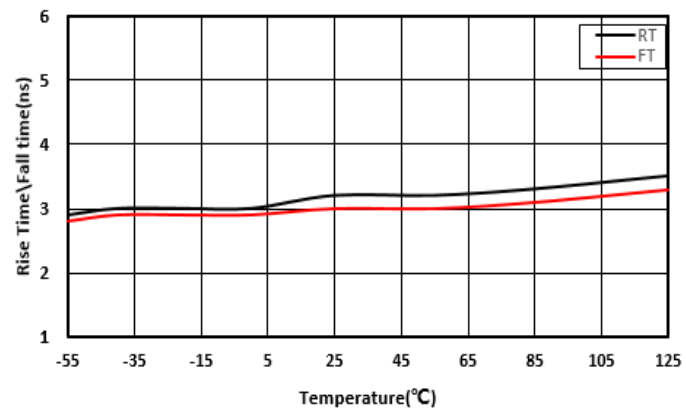
V_{CC}=3.3V

Figure 7-17 Driver Propagation Delay vs. Temperature



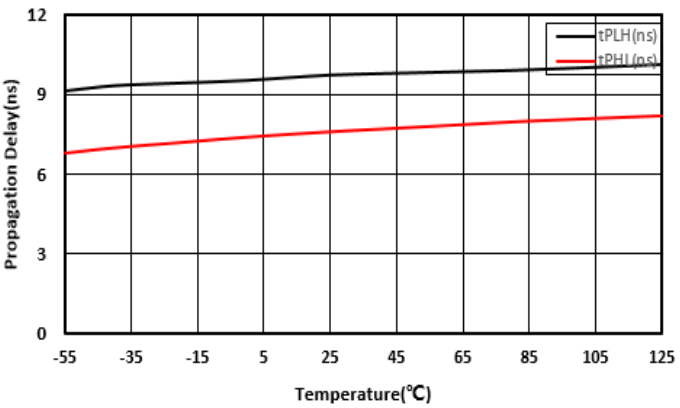
T_A=25℃ VCC =3.3V R_L=54Ω

Figure 7-18 Supply Current vs. Signal Rate



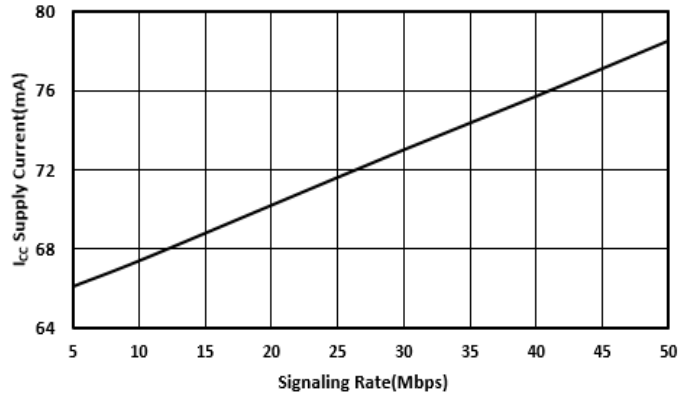
V_{CC}=5V

Figure 7-19 Driver Output Rise Time\Fall Time vs. Temperature



V_{CC}=5V

Figure 7-20 Driver Propagation Delay vs. Temperature



T_A=25℃ VCC =5V R_L=54Ω

Figure 7-21 Supply Current vs. Signal Rate

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8. Parameter Measurement Information

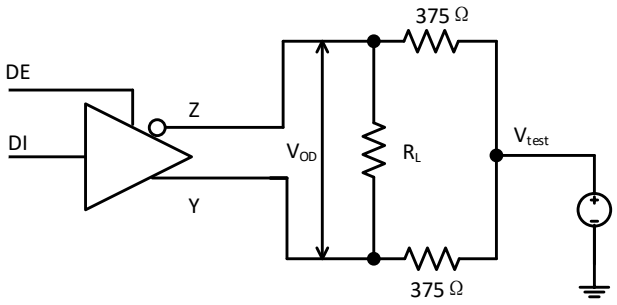

Figure 8-1. Driver Differential Output Voltage With Common-Mode Load

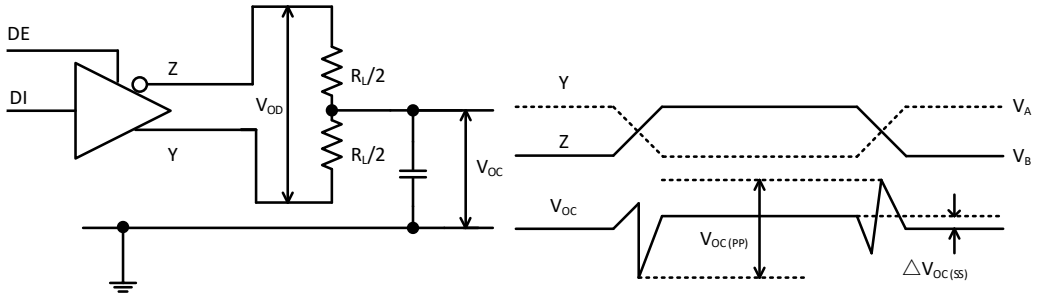

Figure 8-2. Driver Differential and Common-Mode Output With RS-485 Load

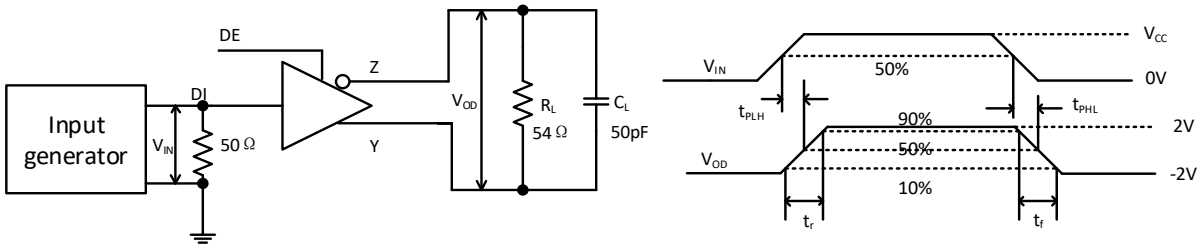

Figure 8-3. Driver Differential Output Rise and Fall Times and Propagation Delays

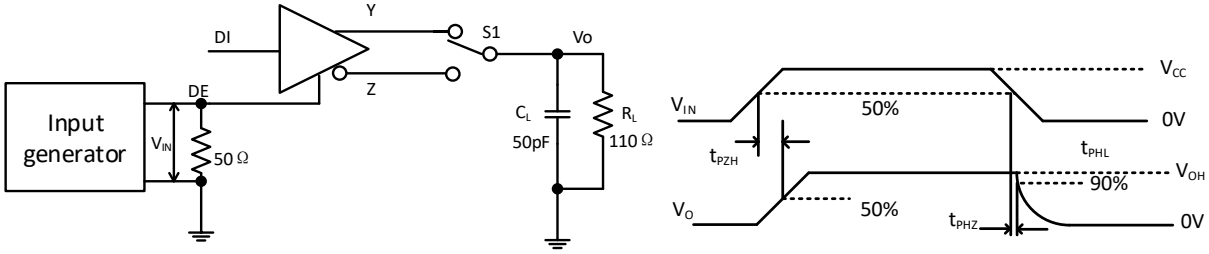

Figure 8-4. Driver Enable and Disable Times With Active High Output and Pull-Down Load

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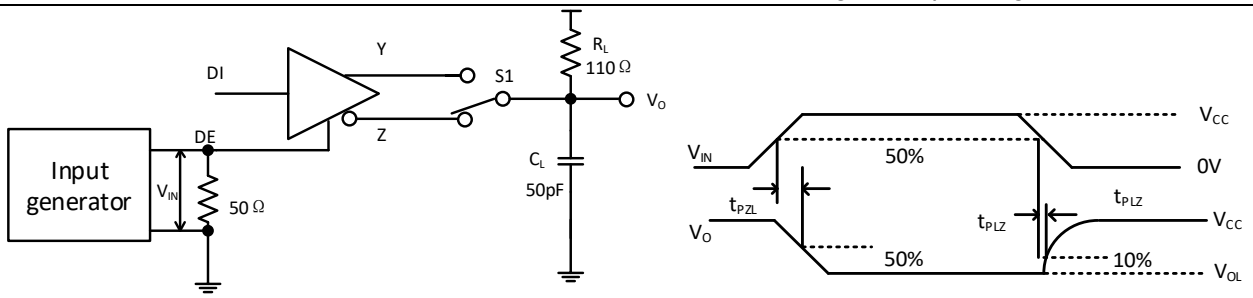

Figure 8-5. Driver Enable and Disable Times With Active Low Output and Pull-up Load

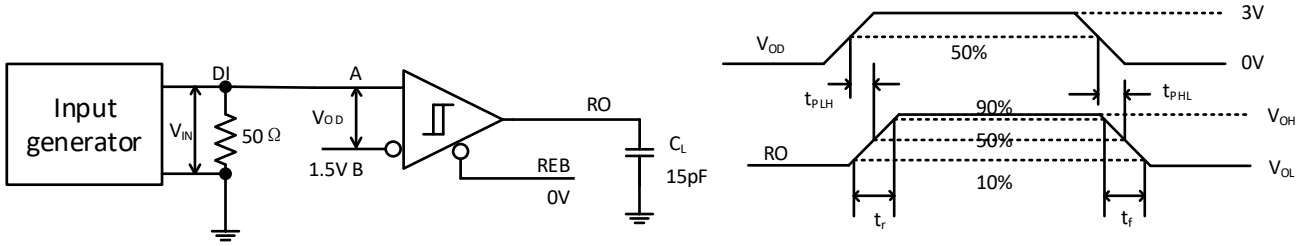

Figure 8-6. Receiver Output Rise and Fall Times and Propagation Delays

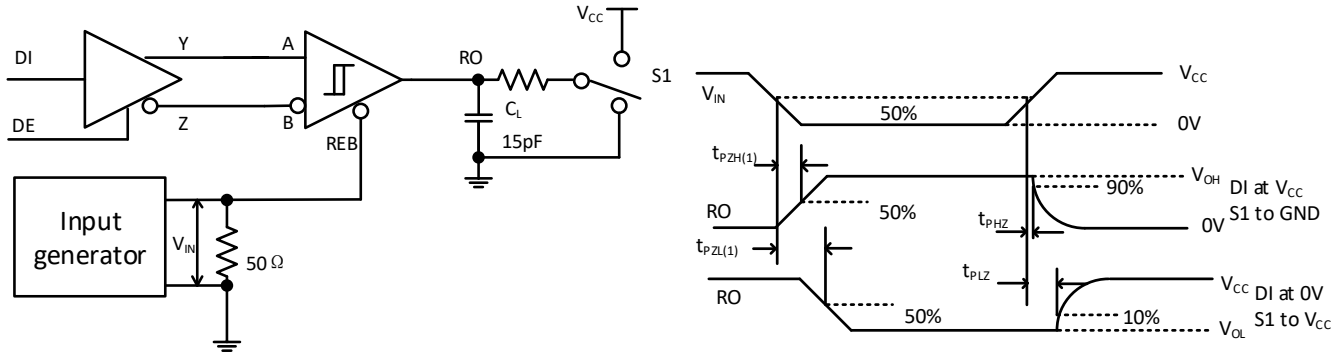

Figure 8-7. Receiver Enable/Disable Times With Driver Enabled

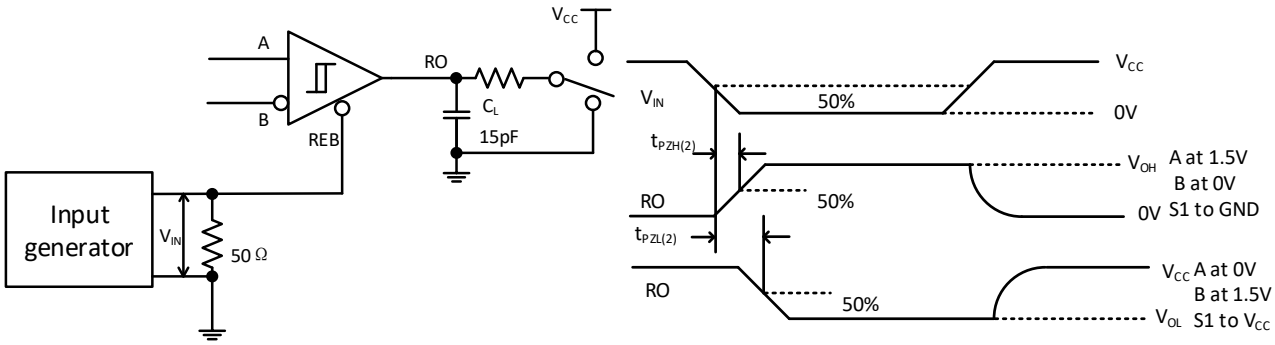

Figure 8-8. Receiver Enable Times With Driver Disabled

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9. Detailed Description

9.1. Overview

The CA-IF48xx family of devices are optimized for RS-485/RS-422 applications per the EIA/TIA-485 standard. These devices contain one differential driver and one differential receiver. The receiver features a 1/8-unit load input impedance, allowing up to 256 transceivers on a single bus. The CA-IF48xxHS/HM/HD serials devices are the half-duplex transceivers, and the CA-IF48xxFS/FM/FD serials devices are the full-duplex transceivers. Driver Enable (DE) and Receiver Enable (REB) pins are included on the half-duplex transceivers CA-IF48xxHS/HM/HD. When disabled, the driver and receiver outputs are high impedance. In addition, the CA-IF4805 features reduced slew-rate driver that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 500kbps. The driver slew-rates of the CA-IF4820 and CA-IF4850 are not limited, allowing them to transmit up to 20Mbps and up to 50Mbps data rate respectively.

To reduce system complexity and the need for external protection, the driver outputs/receiver inputs of the CA-IF4805/CA-IF4820/CA-IF4850 devices are designed to withstand voltage faults of up to ±30V with respect to ground without damage, and the common-mode range exceeds the standard with ±15V for both the driver and receiver. They also incorporate a high ESD protection circuit capable of protecting against up to ±30kV (half-duplex transceivers) or up to ±15kV (full-duplex transceivers) of ESD Human Body Model (HBM) for driver outputs and receiver inputs. In addition, two mechanisms against excessive power dissipation caused by faults or bus contention. The first, over-current protection on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state once the junction temperature of the devices exceed the thermal shutdown threshold T_{SD} (180°C, typ.). The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.2. Device Functional Modes

9.2.1. Device Function Modes for the CA-IF48xxHS/HM/HD

The CA-IF48xxHS/HM/HD driver accepts a single-ended, logic-level input (DI) and transfers it to a differential RS-485/RS-422 level output on the A and B driver outputs. Set the driver enable input (DE) low to disable the driver. A and B are high impedance when the driver is disabled. Also, the DE pin has internal pull-down to GND, when left open, the driver is disabled as well. The DI pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low. See Table 9-1 for more details.

Table 9-1. CA-IF48xxHS/HM/HD Driver Function Table

Input	Enable	Output		Function
DI	DE	A	B	
H	H	H	L	Drive bus high
L	H	L	H	Drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Drive bus high by default

Note:
L = Low level; H = High level; Z = high impedance; X = Don't care.

The receiver accepts a differential, RS-485/RS-422 level input on the A and B inputs and transfers it to a single-ended, logic-level output (RO). Drive the receiver enable input (REB) low to enable the receiver. Drive REB high to disable the receiver. RO is high impedance when REB is high. Also, the REB pin has an internal pull-up resistor to V_{CC}, thus, when left open, the receiver is disabled and RO output is high impedance.

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Table 9-2. CA-IF48xxHS/HM/HD Receiver Function Table

Differential Input	Enable	Output	Function
$V_{ID} = V_A - V_B$	REB	RO	
$V_{TH+} < V_{ID}$	L	H	High-level bus state
$V_{TH-} < V_{ID} < V_{TH+}$	L	Indeterminate	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Low-level bus state
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output
Note: L = Low level; H = High level; Z = high impedance.			

The CA-IF48xx devices include a true fail-safe feature that ensures the receiver output (RO) is high when the receiver inputs are shorted or open, or when they are connected to a differentially terminated transmission line with all drivers disabled. If the differential receiver input voltage (V_A - V_B) is greater than or equal to V_{TH+} (-20mV, maximum), RO is logic high. When the input voltage (V_A - V_B) is less than the negative input threshold V_{TH-} (-200mV, minimum), the receiver output RO turns low. See Table 9-2 for more details.

9.2.2. Device Function Modes for the CA-IF48xxFS/FM/FD

For these full-duplex devices, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input DI at all times. In order to avoid data conflict, only one CA-IF48xxFS/FM/FD driver can be attached to a twisted pair of RS485 cable. The DI pin has an internal pull-up resistor to V_{CC}, thus, when DI left open or a logic high at DI causes Y to turn high and Z to turn low. When DI is low, the output states reverse: Z turns high, Y becomes low. See Table 9-3 for details. Considering that the driver of this series full-duplex transceivers doesn't have enable control, these devices can only be used for point-to-point communication or single transmitter multi-receivers bus topology to avoid the data conflict on the bus.

Table 9-3. CA-IF48xxFS/FM/FD Driver Function Table

Input	Output		Function
DI	Y	Z	
H	H	L	Drive bus high
L	L	H	Drive bus low
OPEN	H	L	Drive bus high by default
Note: L = Low level; H = High level; Z = high impedance.			

When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output RO turns high. When V_{ID} is less than the negative input threshold V_{TH-}, the receiver output RO turns low. As mentioned above, all of the CA-IF48xx devices include a true fail-safe feature that ensures the receiver output (RO) is high when the receiver inputs are shorted or open, or idle status.

Table 9-4. CA-IF48xxFS/FM/FD Receiver Function Table

Differential Input	Enable	Output	Function
$V_{ID} = V_A - V_B$	REB	RO	
$V_{TH+} < V_{ID}$	L	H	High-level bus state
$V_{TH-} < V_{ID} < V_{TH+}$	L	Indeterminate	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Low-level bus state
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output
Note: L = Low level; H = High level; Z = high impedance.			

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10. Application Information

The CA-IF48xx family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following Figure 10-1 typical network application circuit, to minimize reflections, terminate the line at both ends with a termination resistor, R_T, whose value matches the characteristic impedance(Z_0) of the cable, and keep stub lengths off the main line as short as possible. This method, known as parallel termination, generally allows for higher data rates over longer cable length. For the CA-IF48xxFS/FM/FD full-duplex transceivers, since the driver has no enable control, these devices are usually used for point-to-point communication to avoid data conflict problems. See Figure 10-2 typical application circuit.

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with at least 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

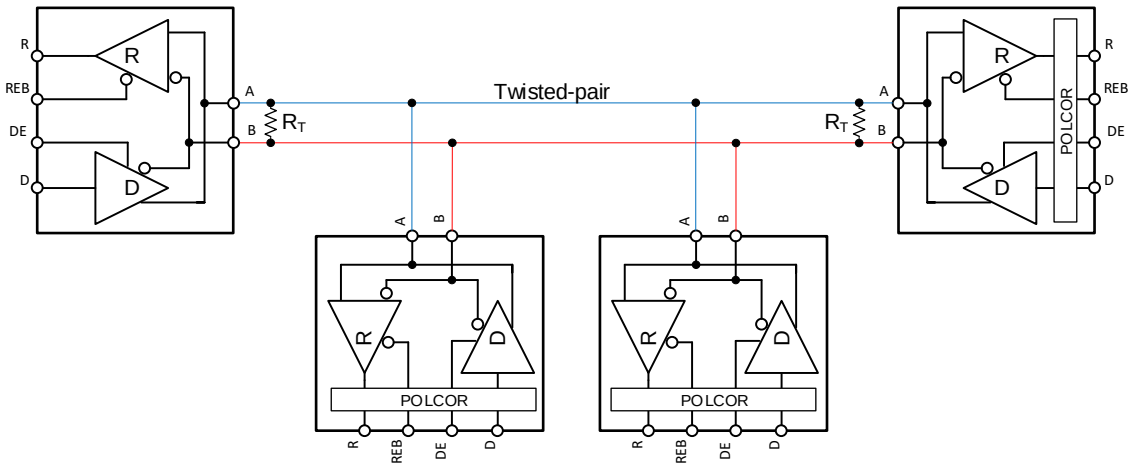

Figure 10-1. Typical RS-485 Network With CA-IF48xxHS/HM/HD Half-Duplex Transceivers

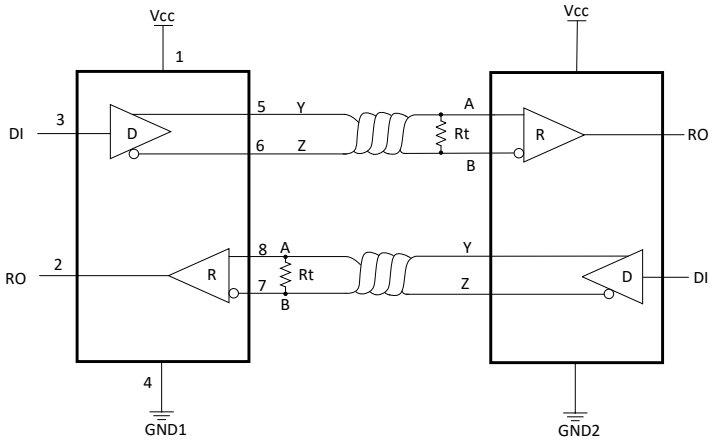

Figure 10-2. Typical RS-485 Network With CA-IF48xxFS/FM/FD Full-Duplex Transceivers

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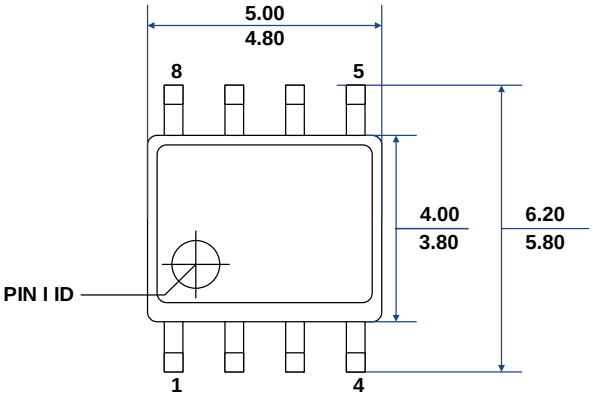
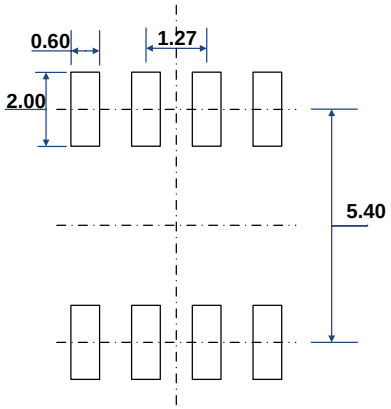
11. Package Information

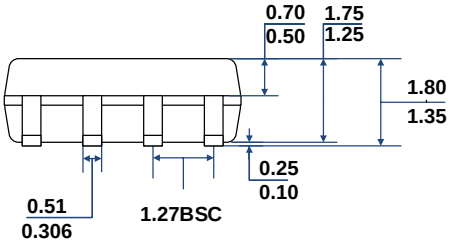
11.1. SOIC8 Package Outline



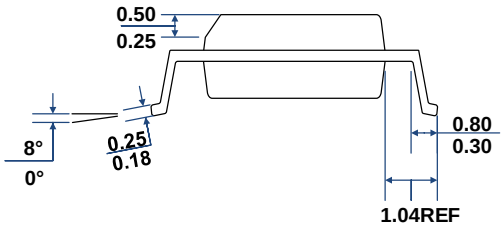
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

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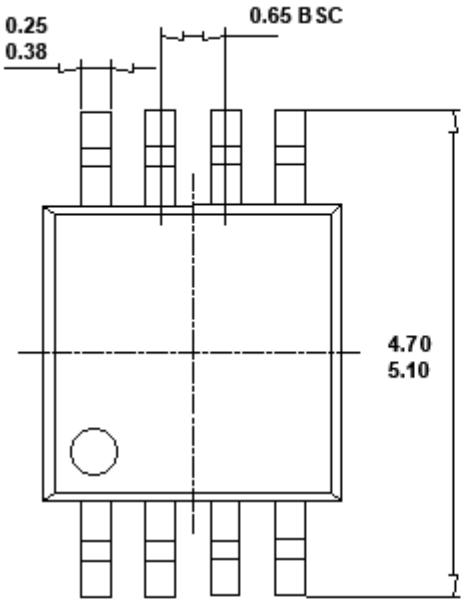
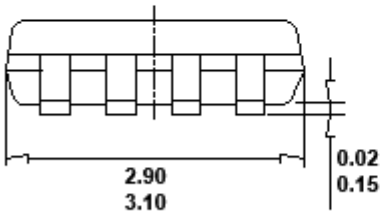
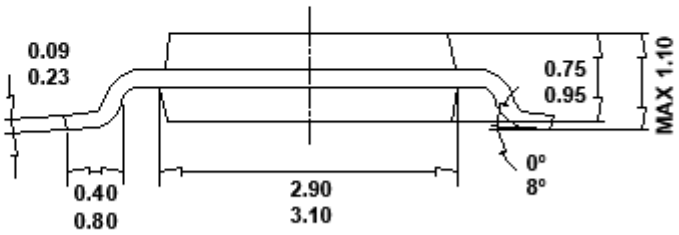
11.2. MSOP8 Package Outline



TOP VIEW



BOTTOM VIEW



LEFT SIDE VIEW

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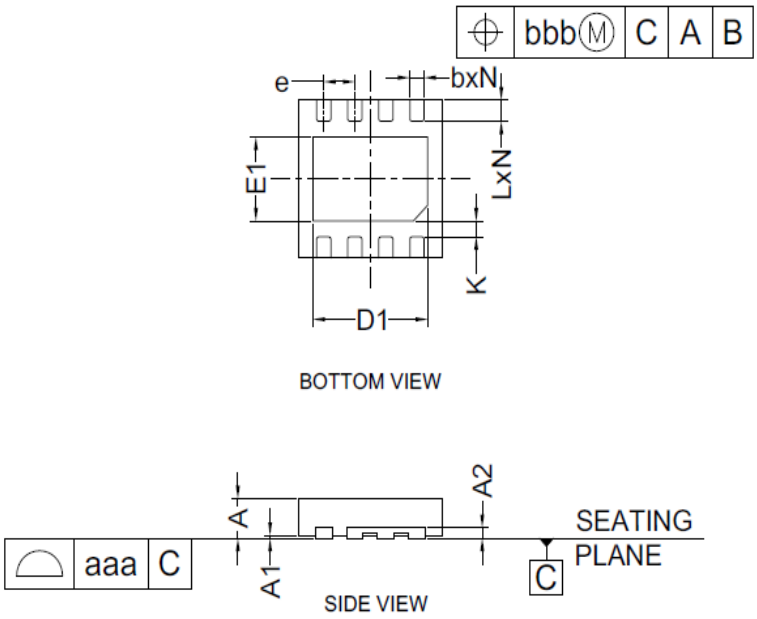
11.3. DFN8 Package Outline

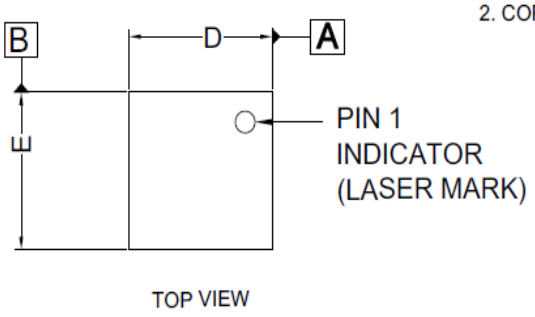


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.30	0.35	0.40
D	2.90	3.00	3.10
D1	2.51	2.56	2.61
E	2.90	3.00	3.10
E1	1.55	1.60	1.65
e		0.65BSC	
L	0.35	0.40	0.45
N		8	
aaa		0.08	
bbb		0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS(ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS THE TERMINALS.



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12. Soldering Temperature (reflow) Profile

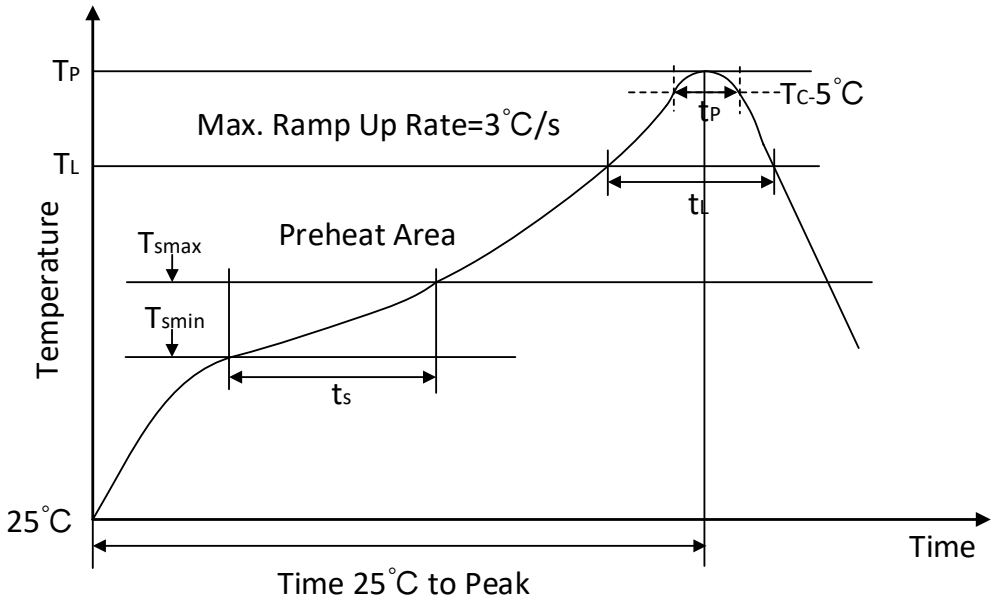

Figure 12- 1 Soldering Temperature (reflow) Profile

Table12- 1 Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃ of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

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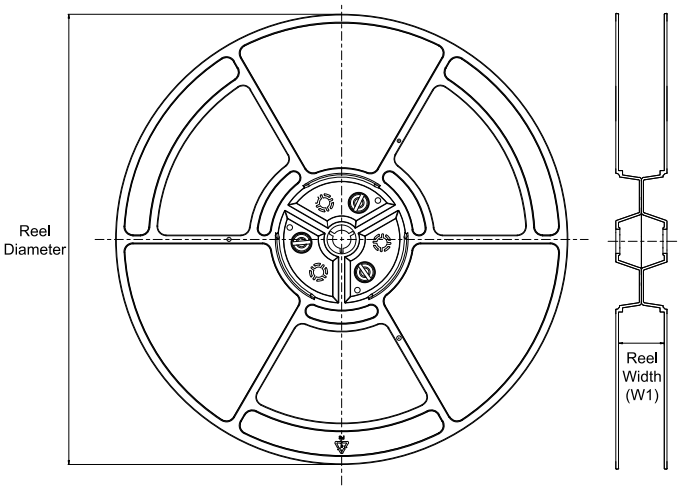
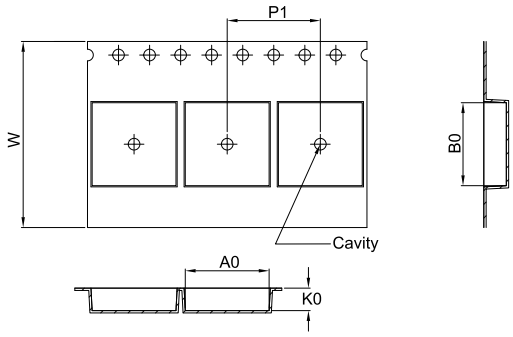
13. Tape and Reel Information

REEL DIMENSIONS

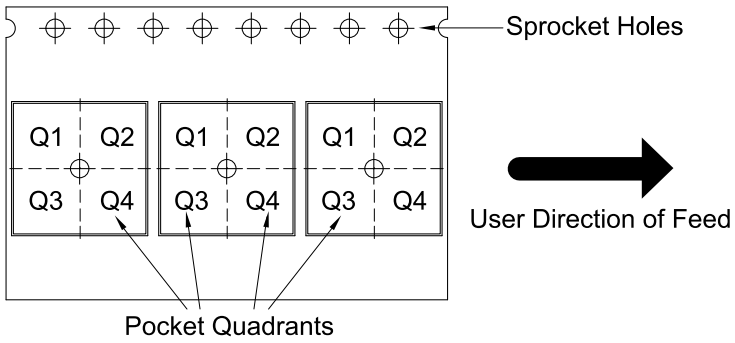


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF4805HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4805FS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4820HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4820FS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4850HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4850FS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4805HM	MSOP8	M	8	5000	330	12.4	5.2	3.3	1.50	8.00	12.00	Q1
CA-IF4805FM	MSOP8	M	8	5000	330	12.4	5.2	3.3	1.50	8.00	12.00	Q1
CA-IF4820HM	MSOP8	M	8	5000	330	12.4	5.2	3.3	1.50	8.00	12.00	Q1
CA-IF4820FM	MSOP8	M	8	5000	330	12.4	5.2	3.3	1.50	8.00	12.00	Q1
CA-IF4850HM	MSOP8	M	8	5000	330	12.4	5.2	3.3	1.50	8.00	12.00	Q1
CA-IF4850FM	MSOP8	M	8	5000	330	12.4	5.2	3.3	1.50	8.00	12.00	Q1
CA-IF4805HD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4805FD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4820HD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4820FD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4850HD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4850FD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1

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