6A Sink/5A Source, 5.7kV$_{RMS}$ Opto-Compatible Single-Channel Isolated Gate Driver

1. Features

- **6A Peak Sink Current and 5A Peak Source Current**
- **Up to 30V Output Drive Supply Range with 8V and 12V UVLO options**
- **Support Rail to Rail Output**
- **Up to 7V Reverse Voltage on Input-stage, Interlock**
- **Matching Propagation Delay**
  - 70ns Propagation delay (typical)
  - 25ns Part to part propagation delay matching (maximum)
  - 35ns Pulse width distortion(maximum)
- **-40°C to +150°C Operating Junction Temperature Range**
- **Robust Galvanic Isolation**
  - High lifetime: >40 years
  - Up to 5.7kV$_{RMS}$ isolation rating for the wide-body packages and 3.75 kV$_{RMS}$ isolation rating for DUB8 package
  - Common-mode transient immunity (CMTI) > ±150kV/µs
- **Package options**
  - 6-pin wide-body SOIC (J) Package
  - 8-pin wide-body SOIC8 (G) Package
  - 8-pin DUB8 (U) package
- **Safety regulatory approvals**
  - VDE Reinforced isolation and Basic isolation per DIN EN IEC 60747-17 (VDE 0884-17): 2021-10
  - UL certification per UL 1577 for 1 minute
  - TUV certification per EN61010-1:2010+A1
  - CQC certification per GB 4943.1-2022

2. Applications

- Isolated DC-DC and AC-DC Converters
- Motor Control
- Uninterruptible Power Supply (UPS)
- Isolated Gate Driver for Inverters

3. General Description

The CA-IS3211 devices are a family of single-channel, opto-compatible isolated gate driver capable of sinking 6A and sourcing 5A currents. These devices operate with dual supplies or a single supply of 10V to 30V (8V UVLO version) or 14V to 30V (12V UVLO version) wide voltage range of V_{CC} - V_{EE}, making them ideal to drive power MOSFET, IGBT or silicon-carbide(SiC) transistors in various inverter, motor control or isolated power supply systems. The CA-IS3211 can be configured as low-side and high-side drivers. The CA-IS3211Vx offers single terminal gate drive output: V_{OUT} and the CA-IS3211Sx offers dual separate output terminals: OUTH and OUTL. The driver output is pulled to low state to turn-off external power transistors when V_{CC} supply input is either not powered, open-circuit or in UVLO.

All devices have integrated digital galvanic isolation using Chipanalog's proprietary capacitive isolation technology and feature isolation with a withstand voltage rating of up to 5.7kV$_{RMS}$ for 60 seconds and minimum common-mode transient immunity (CMTI) of 150kV/µs. These devices can be used as drop-in replacement for the industry standard optocoupler-based gate drivers while providing high CMTI, low propagation delay, small pulse width distortion and small part-to-part skew. The input stage is an analog diode which means long term reliability and excellent aging characteristics.

The CA-IS3211 devices are available either in a 6-pin or 8-pin wide-body SOIC packages, and 8-pin DUB package. All devices are rated for operation at junction temperatures of -40°C to +150°C.

Device Information

Part Number	Package	Package Size(NOM)
CA-IS3211VBJ	SOIC6-WB	7.5 mm x 4.68 mm
CA-IS3211VCJ	SOIC6-WB	7.5 mm x 4.68 mm
CA-IS3211VBG	SOIC8-WB	7.5 mm x 5.85 mm
CA-IS3211VCG	SOIC8-WB	7.5 mm x 5.85 mm
CA-IS3211SBG	SOIC8-WB	7.5 mm x 5.85 mm
CA-IS3211SCG	SOIC8-WB	7.5 mm x 5.85 mm
CA-IS3211VBU	DUB8	6.35 mm x 9.2 mm
CA-IS3211VCU	DUB8	6.35 mm x 9.2 mm

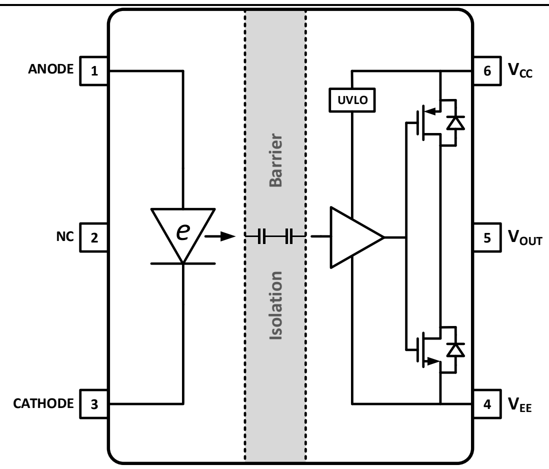

Figure 3-1. Simplified Schematic

4. Ordering Information

Table 4-1. Ordering Information

Part #	Output	UVLO (V)	Isolation Rating(V_{PK})	Package
CA-IS3211VBJ	Single output	8	8000	SOIC6-WB
CA-IS3211VCJ	Single output	12	8000	SOIC6-WB
CA-IS3211VBG	Single output	8	8000	SOIC8-WB
CA-IS3211VCG	Single output	12	8000	SOIC8-WB
CA-IS3211SBG	Split output, OUTH & OUTL	8	8000	SOIC8-WB
CA-IS3211SCG	Split output, OUTH & OUTL	12	8000	SOIC8-WB
CA-IS3211VBU	Single output	8	5300	DUB8
CA-IS3211VCU	Single output	12	5300	DUB8

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5. Revision History

Revision Number	Description	Revised Date	Page Changed
Version 1.00	NA		NA
Version 1.01	1. Update package size of DUB8 2. Update POD of DUB8 package		1 24
Version 1.02	1. Update POD of SOIC6-WB package, add PIN 1 marker		22
Version 1.03	1. Update UL certification information		8
Version 1.04	1. Update TUV certification information		8
Version 1.05	1. Update VDE certification information 2. Add new part number of CA-IS3221VBU 3. Update the POD of SOIC6-WB		8 2 22
Version 1.06	1. Update insulation specification	2023/11/02	7
Version 1.07	1. Update insulation specification 2. Update the POD 3. Update CQC certification information	2024/05/27	1,7,8,22,23,24
Version 1.08	1. Taping information SPQ updated from 700 to 800	2024/06/20	26

6. Pin Configuration and Description

6.1. CA-IS3211 VBJ/VCJ Pin Configuration and Description

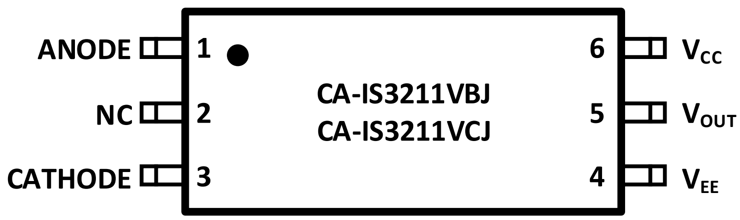


Figure 6-1. The CA-IS3211 VBJ/VCJ Pin Configuration

Table 6-1. The CA-IS3211VBJ/VCJ Pin Description

Pin Name	Pin Number	Type	Description
ANODE	1	Input	Driver input, the anode of input diode.
NC	2	---	No internal connection.
CATHODE	3	Input	Driver input, the cathode of input diode.
V_{EE}	4	Power Supply	Negative Power supply input for output-side, it's the negative output supply rail. For bipolar operation, bypass V_{EE} to output-side ground with 0.1µF||10µF capacitors as close as possible to the device. For single supply operation, connect V_{EE} to GND on the output-side.
V_{OUT}	5	Output	Gate driver output.
V_{CC}	6	Power Supply	Positive Power supply input for output-side, it's the positive output supply rail. Bypass V_{CC} to output-side ground with 0.1µF||10µF capacitors as close as possible to the device.

6.2. CA-IS3211VBG/VCG/VBU/VCU Pin Configuration and Description

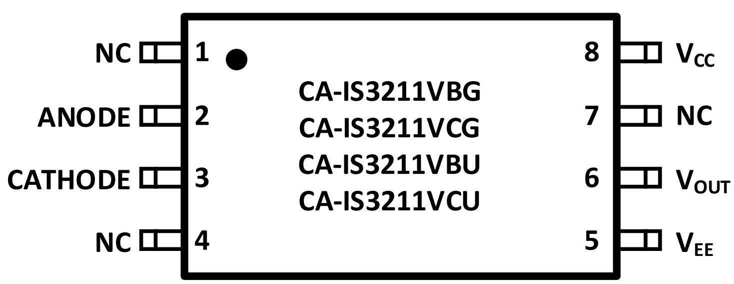


Figure 6-2. The CA-IS3211VBG/VCG/VCU Pin Configuration

Table 6-2. The CA-IS3211VBG/VCG/VCU Pin Description

Pin Name	Pin Number	Type	Description
ANODE	2	Input	Driver input, the anode of input diode.
CATHODE	3	Input	Driver input, the cathode of input diode.
NC	1, 4, 7	---	No internal connection.
V_{EE}	5	Power Supply	Negative Power supply input for output-side, it's the negative output supply rail. For bipolar operation, bypass V_{EE} to output-side ground with 0.1µF||10µF capacitors as close as possible to the device. For single supply operation, connect V_{EE} to GND on the output-side.
V_{OUT}	6	Output	Gate driver output.
V_{CC}	8	Power Supply	Positive Power supply input for output-side, it's the positive output supply rail. Bypass V_{CC} to output-side ground with 0.1µF||10µF capacitors as close as possible to the device.

6.3. CA-IS3211SBG/SCG Pin Configuration and Description

Figure 6-3. The CA-IS3211SBG/SCG Pin Configuration

Table 6-3. The CA-IS3211SBG/SCG Pin Description

Pin Name	Pin Number	Type	Description
ANODE	2	Input	Driver input, the anode of input diode.
CATHODE	3	Input	Driver input, the cathode of input diode
NC	1, 4	---	No internal connection.
V_{EE}	5	Power Supply	Negative Power supply input for output-side, it's the negative output supply rail. For bipolar operation, bypass V_{EE} to output-side ground with 0.1µF||10µF capacitors as close as possible to the device. For single supply operation, connect V_{EE} to GND on the output-side.
OUTL	6	Output	Gate driver pull-down output.
OUTH	7	Output	Gate driver pull-up output.
V_{CC}	8	Power Supply	Positive Power supply input for output-side, it's the positive output supply rail. Bypass V_{CC} to output-side ground with 0.1µF||10µF capacitors as close as possible to the device.

7. Specifications

7.1. Absolute Maximum Ratings[1]

over operating free-air temperature range unless otherwise specified. [1]

Parameters		Minimum	Maximum	Unit
$I_{F(AVG)}$	Average input current	-	25	mA
$I_{F(TRAN)}$ < 1us pulse, 300ps	Peak transient input current		1	A
$V_{R(MAX)}$	Reverse input voltage		7.0	V
V_{CC} - V_{EE}	Output-side supply voltage range	-0.3	32	V
V_{OUT}	Driver output voltage	V_{EE} - 0.3	V_{CC} + 0.3	V
T_J [2]	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. To maintain the recommended operating junction temperature conditions, see Thermal Information.

7.2. ESD Ratings

			Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001.	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101.	±2000	

7.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

Parameters			Minimum	Typical	Maximum	Unit
V_{CC}	Driver output voltage(V_{CC} - V_{EE})	12V UVLO version	14		30	V
		8V UVLO version	10		30	
$I_{F(ON)}$	Input diode turn-on: diode forward current		7		16	mA
$V_{F(OFF)}$	Input diode turn-off: anode voltage - cathode voltage		-5.5		0.9	V
T_J	Junction temperature		-40		150	°C
T_A	Ambient temperature		-40		125	°C

7.4. Thermal Information

Thermal Metric		SOIC8-WB (G)	SOIC6-WB (J)	DUB8 (U)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	126	73.3	°C/W
$R_{\theta JC(top)}$	Junction to Case (top)	51.7	66.1	63.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	62.8	43.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.0	29.6	27.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.5	60.8	42.7	°C/W

7.5. Power Ratings

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
P_D	Maximum input and output power dissipation (derate 6mW/°C above +25°C)	V_{CC}= 20V, I_F = 10mA, 10kHz square wave with 50% duty cycle, C_L = 180nF, T_A = 25°C			750	mW
P_{D1}	Maximum input power dissipation[1]				10	mW
P_{D2}	Maximum output power dissipation				740	mW

Note:

1. The maximum P_{D1} = 40mW and the absolute maximum rating of P_{D1} is 55mW.

7.6. Insulation Specifications

Parameters		Test Conditions	Specifications		Unit
			G/J	U	
CLR	External clearance	Shortest terminal-to-terminal distance through air	>8.5	>6.1	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	>8.5	>6.8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>28	>28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)；IEC 60112	>600	>600	V
	Material group	According to IEC 60664-1	I		
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I-III	
DIN V VDE V 0884-17:2021-10[1]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	1414	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1500	1000	V_{RMS}
		DC voltage	2121	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% production test)	8000	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (certified) (Reinforced) $V_{TEST} = 1.3 \times V_{IOSM}$ (certified) (Basic)	8000	6250	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5		pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5		
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s; (Reinforced) $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s; (Basic)	≤5		
C_{IO}	Barrier capacitance, input to output[4]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	0.5		pF
R_{IO}	Isolation resistance , input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$		
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$		
	Pollution degree		2		
	Climatic category		40/125/21		
UL 1577					
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5700	3750	V_{RMS}

Notes:
1. This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7. Safety-Related Certifications

VDE	UL	TUV	CQC
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to EN61010-1:2010+A1	Certified according to GB 4943.1-2022
Reinforced isolation(SOIC6-WB/ SOIC8-WB): Maximum transient isolation voltage: $8000V_{pk}$ Maximum repetitive-peak isolation voltage: 2121 V_{pk} Maximum surge isolation voltage: $8000V_{pk}$ **Basic isolation (DUB8):(pending)** Maximum transient isolation voltage: $5300V_{pk}$ Maximum repetitive-peak isolation voltage: 1414 V_{pk} Maximum surge isolation voltage: $6250V_{pk}$	Protection voltage: - $5.7kV_{RMS}$ for SOIC6-WB and SOIC8-WB packages - $3.75kV_{RMS}$ for DUB8 package	Reinforced insulation 5.7 kV_{RMS} for SOIC6-WB and SOIC8-WB packages Basic insulation 3.75 kV_{RMS} for DUB8 packages	Reinforced insulation: SOIC8-WB package
Certificate number: 40052786 (Reinforced)	Certificate number: E511334 CA-IS3211VBU： Pending	Certificate number: AK 505918190001 CA-IS3211VBU： Pending	Certificate number: CQC24001434134

7.8. Safety Limits

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Safety output supply current	R_{qJA} = 126°C/W, V_I = 15V, T_J = 150°C, T_A = 25°C			50	mA
		R_{qJA} = 126°C/W, V_I = 30V, T_J = 150°C, T_A = 25°C			25	
P_S	Safety power dissipation	R_{qJA} = 126°C/W, T_J = 150°C, T_A = 25°C			750	mW
T_S	Maximum safety temperature[1]				150	°C

Note：
1. $T_{J(max)} = T_S = T_A + R_{\theta JA} * P_S$, where $T_{J(max)}$) is the maximum allowed junction temperature. $P_S = I_S * V_{IN}$, where V_{IN} is the maximum supply voltage.

7.9. Electrical Characteristics

All minimum/maximum specs are at T_A = -40°C to +125°C, V_{CC} = 15V to 30V, V_{EE} = GND, $I_{F(on)}$ = 7mA to 16mA, $V_{F(off)}$ = -5V to 0.8V, unless otherwise noted. Typical values are at T_A = +25°C, $V_{CC} – V_{EE}$ = 15V, V_{EE} = GND, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
Input						
I_{FLH}	Input diode forward threshold: low to high	V_{out} > 5 V, Cg = 1 nF	1.5	2.8	4	mA
V_F	Input diode forward voltage	I_F = 10 mA	1.8	2.1	2.4	V
V_{F_HL}	Input voltage threshold: high to low	V < 5 V, Cg = 1 nF	0.9			V
$\Delta V_F/\Delta T$	Temp coefficient of V_F	I_F = 10 mA		1.5	1.8	mV/°C
V_R	Input reverse breakdown voltage	I_R = 10 µA	7			V
C_{IN}	Input Capacitance	F = 0.5 MHz		15		pF
Output						
I_{OH}	High level Output Peak current, Figure 8-2	I_F = 10 mA, V_{CC} = 15 V, C_{LOAD} = 0.18µF, C_{VDD} = 10µF, Pulse width <10µs	3	5.0		A
I_{OL}	Low level Output Peak current, Figure 8-2	V_F = 0 V, V_{CC} = 15 V, C_{LOAD} = 0.18µF, C_{VDD} = 10uF, Pulse width <10µs	3.5	6.0		A
V_{OH}	Output high voltage	I_F = 10 mA, I_O = -20mA (respect to V_{CC})	0.07	0.11	0.36	V
		I_F = 10 mA, I_O = 0mA		V_{CC}		V
V_{OL}	Output low voltage	V_F = 0 V, I_O = 20mA		10	25	mV
I_{CC_H}	Output supply current (e-diode turn on)	I_F = 10 mA, I_O = 0mA		1.13	2.2	mA
I_{CC_L}	Output supply current (e-diode turn off)	V_F = 0 V, I_O = 0mA		1.05	2	mA
Undervoltage-Lockout Threshold (12V UVLO)						
$UVLO_R$	UVLO threshold (V_{CC} rising)	I_F = 10mA	10.9	12.1	13.3	V
$UVLO_F$	UVLO threshold (V_{CC} falling)	I_F = 10mA	9.9	11.1	12.3	V
$UVLO_{HYS}$	Undervoltage-lockout threshold hysteresis			1.0		V
Undervoltage-Lockout Threshold (8V UVLO)						
$UVLO_R$	UVLO threshold (V_{CC} rising)	I_F = 10mA	7.3	8.1	8.9	V
$UVLO_F$	UVLO threshold (V_{CC} falling)	I_F = 10mA	6.7	7.4	8.2	V
$UVLO_{HYS}$	Undervoltage-lockout threshold hysteresis			0.7		V

7.10. Switching Characteristics

All minimum/maximum specs are at T_A = -40°C to +125°C, V_{CC} = 15V to 30V, V_{EE} = GND, $I_{F(on)}$ = 7mA to 16mA, $V_{F(off)}$ = -5V to 0.8V, unless otherwise noted. Typical values are at T_A = +25°C, $V_{CC} – V_{EE}$ = 30V, V_{EE} = GND, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
t_r	Output rise time, Figure 8-1	Cg = 1nF, F_{SW} = 20 kHz with 50% duty-cycle; V_{CC} = 15 V		6	28	ns
t_f	Output fall time, Figure 8-1			4	25	ns
t_{PLH}	Propagation delay, low to high, Figure 8-1		40	70	105	ns
t_{PHL}	Propagation delay, high to low, Figure 8-1		40	60	105	ns
t_{PWD}	Pulse width distortion $\lvert t_{PHL}-t_{PLH}\rvert$			10	35	ns
$t_{sk(pp)}$	Part to part propagation delay matching	Cg = 1nF, F_{SW} = 20 kHz with 50% duty-cycle; V_{CC} = 15 V, I_F = 10 mA			25	ns
t_{UVLO_rec}	UVLO recovery time, Figure 9-3	V_{CC} rising from 0V to 15V		70	100	µs
$CMTI_H$	CMTI (output high), Figure 8-3	I_F = 10 mA, V_{CM} = 1500 V, V_{CC} = 30V, T_A = 25°C	150			KV/µs
$CMTI_L$	CMTI (output low), Figure 8-3	V_F = 0 V, V_{CM} = 1500 V, V_{CC} = 30 V, T_A = 25°C	150			KV/µs

7.11. Typical Operating Characteristics

All values are at V_{CC} = 15V, C_{LOAD} = 1nF for timing specs and C_{LOAD} = 180nF for IOH, IOL specs; T_A = -40°C to +125°C, V_{EE} = GND, bypass V_{CC} to V_{EE} with 1µF capacitor, unless otherwise noted.

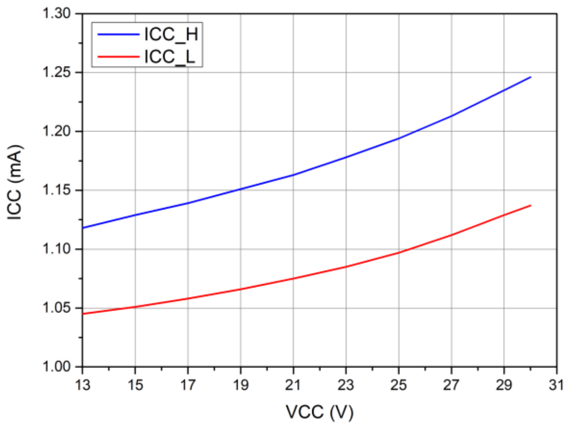


Figure 7-1. V_{CC} supply current vs. V_{CC} supply voltage

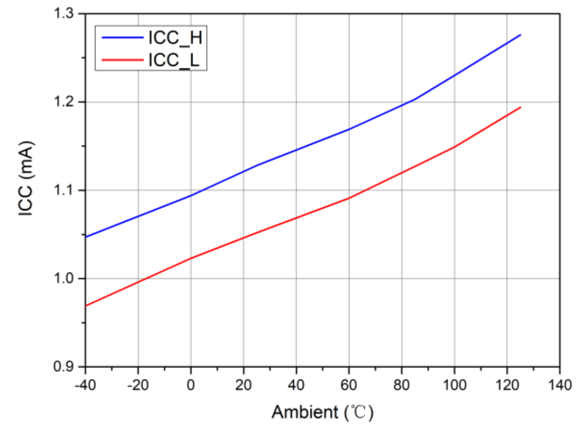


Figure 7-2. V_{CC} supply current vs. Temperature

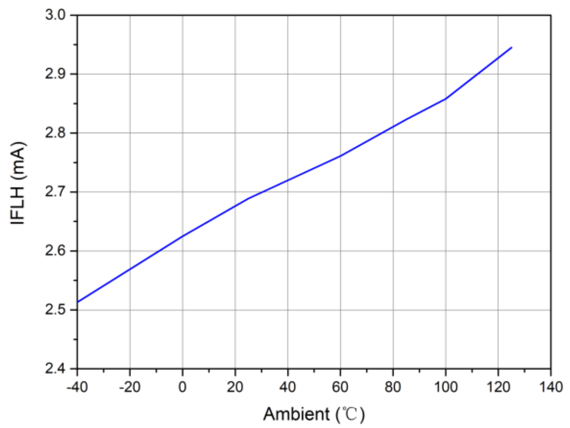


Figure 7-3. Input diode forward threshold vs. Temperature

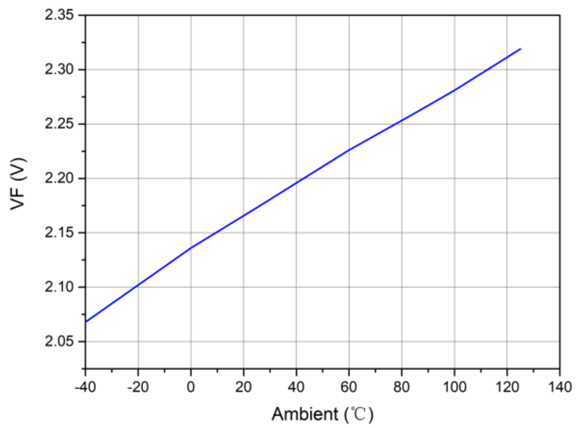
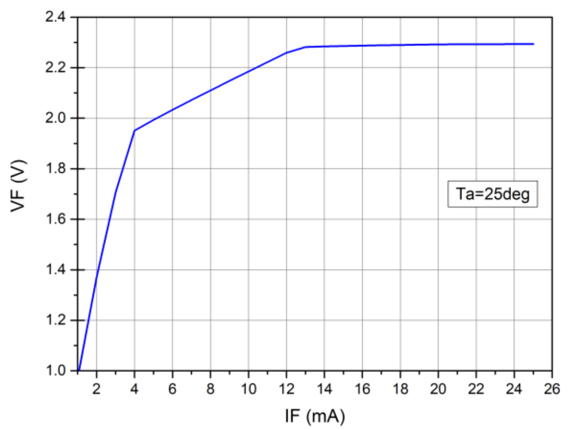


Figure 7-4. Input diode forward voltage vs. Temperature (I_F=10mA)



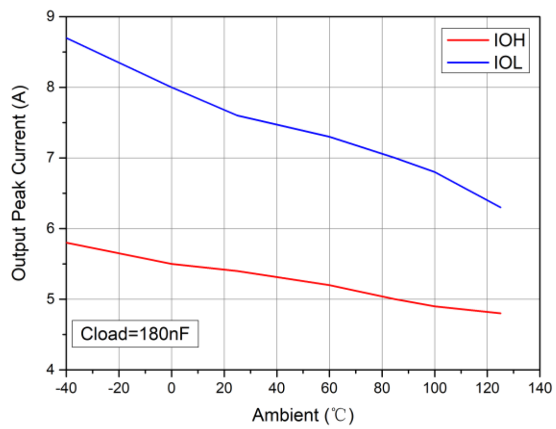
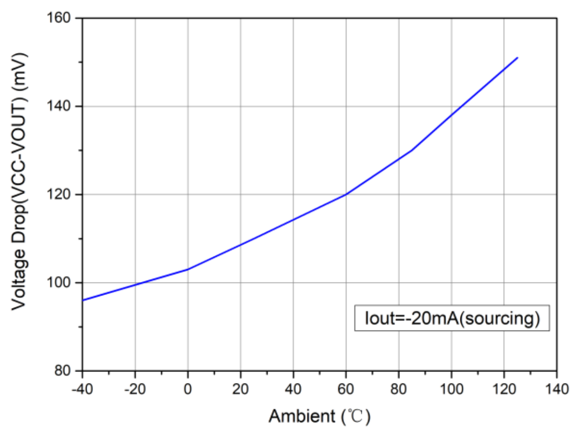


Figure 7-5. Input diode forward voltage vs. Forward current

Figure 7-6. Output peak current vs. Temperature



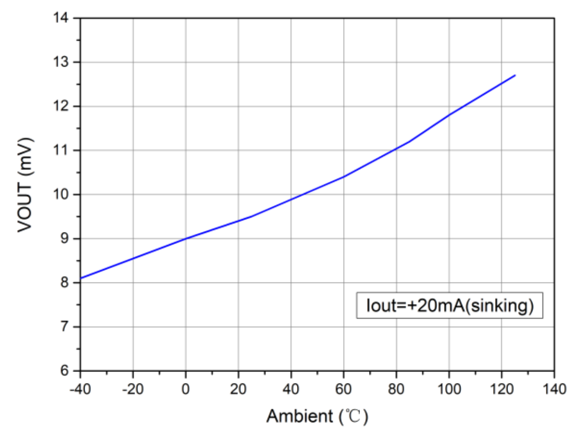
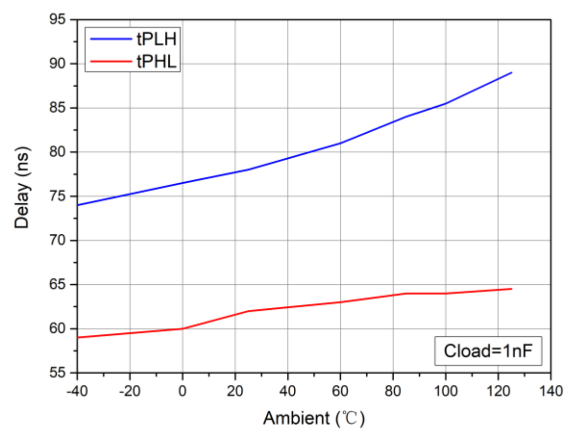


Figure 7-7. V_{OH} vs. Temperature (20mA load current)

Figure 7-8. V_{OL} vs. Temperature (20mA load current)



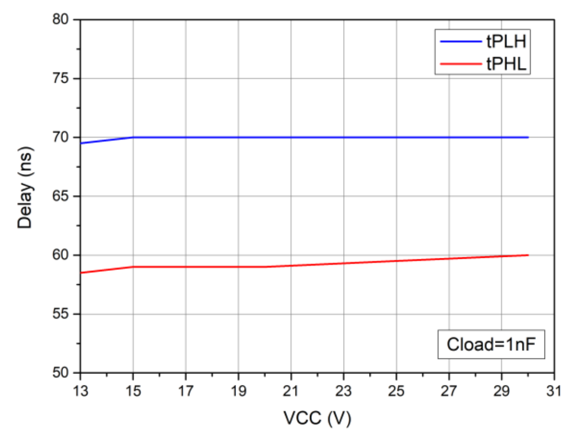
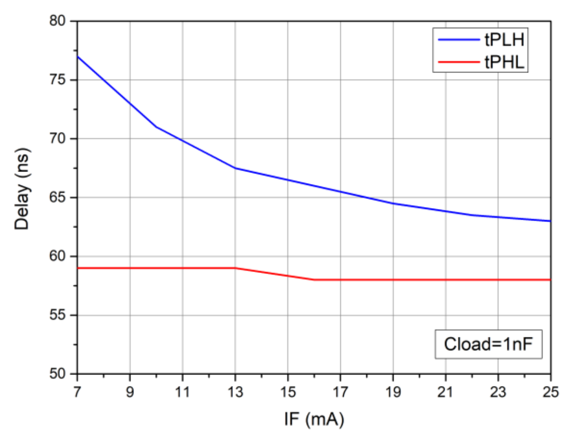


Figure 7-9. Propagation delay vs. Temperature

Figure 7-10. Propagation delay vs. V_{CC} supply voltage



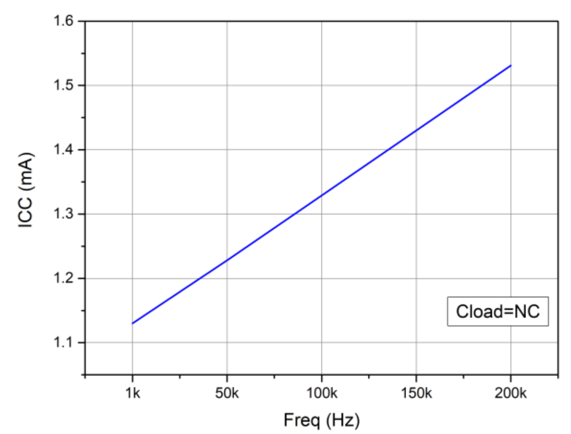


Figure 7-11. Propagation delay vs. Input diode forward current

Figure 7-12. V_{CC} operating current vs. Frequency

8. Parameter Measurement Information

8.1. Propagation Delay and Rising time/Falling time

Figure 8-1 shows the definition and measurement for the propagation delay t_{PLH}, t_{PHL}, and rising time (t_r), falling time (t_f).

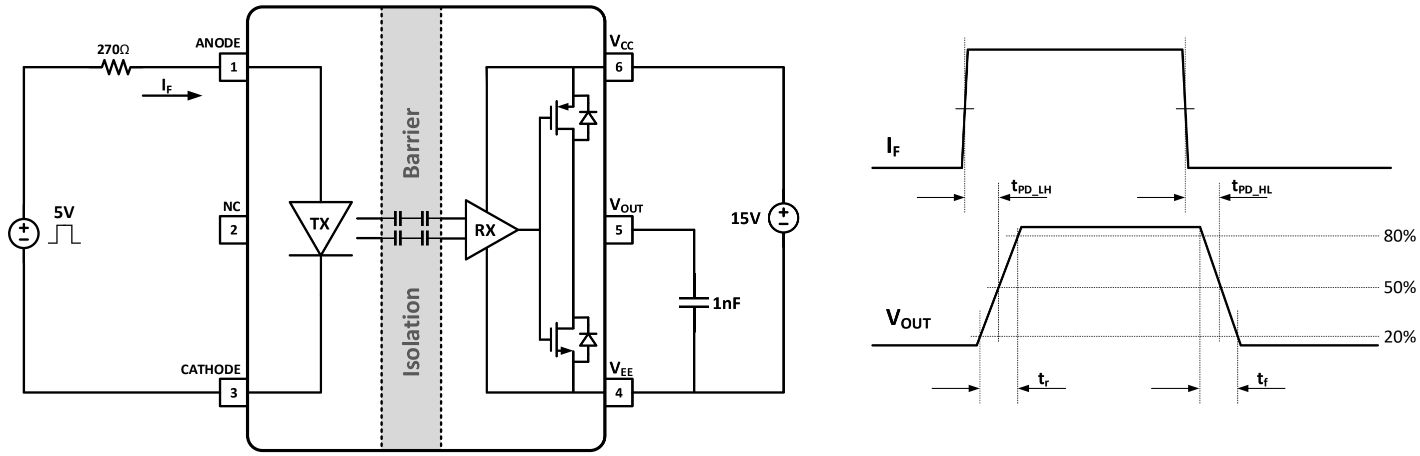


Figure 8-1. Propagation delay and rise time/fall time measurement

8.2. I_{OH} and I_{OL}

Figure 8-2 shows the measurement of output driving current I_{OH} and I_{OL}. In Figure 8-2, C_{OUT} = 180nF. The peak dV/dt of capacitor voltage is measured to determine gate driver's peak sourcing and sinking current.

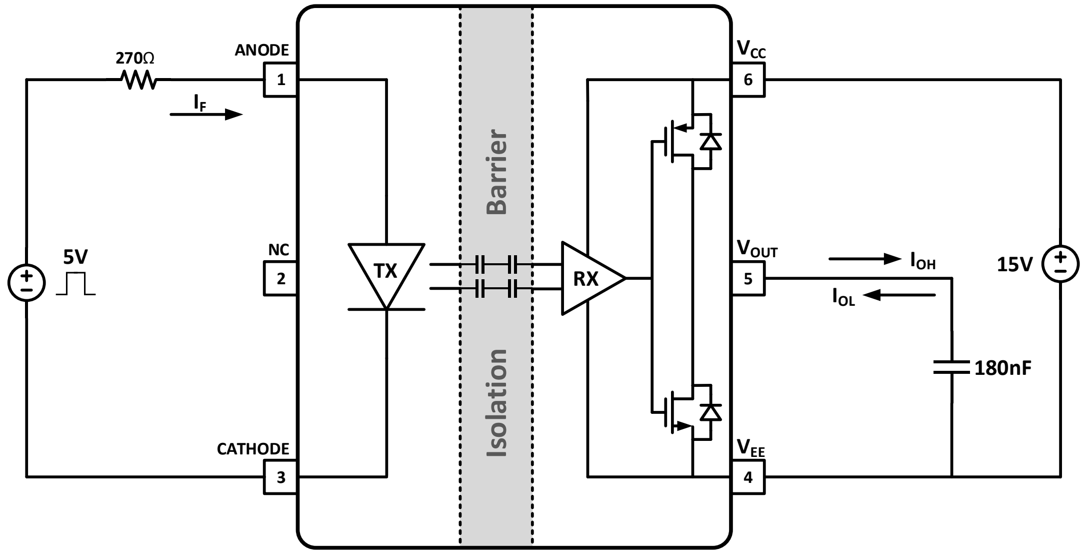


Figure 8-2. I_{OH} and I_{OL} test circuit

8.3. CMTI Test Circuit

Figure 8-3 is the CMTI test configuration for the CA-IS3211.

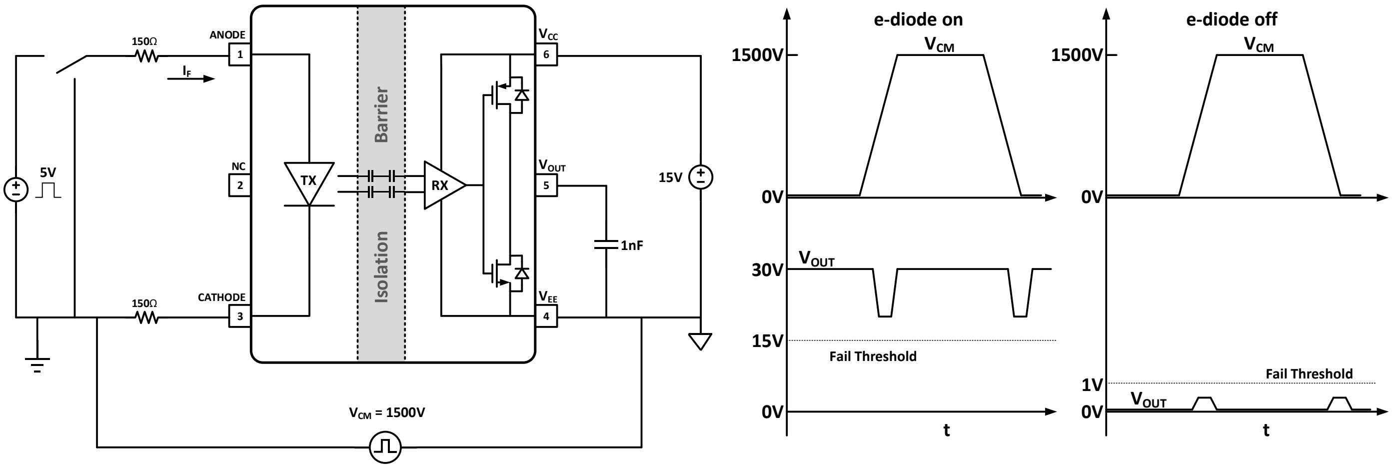


Figure 8-3. Common-mode transient immunity test circuit and waveform

9. Detailed Description

9.1. Overview

The CA-IS3211 is a family of single-channel, opto-compatible isolated gate driver capable of sinking 6A and sourcing 5A currents, that can be used to replace industry standard optocoupler-based gate drivers with pin-to-pin compatibility while providing high CMTI, low propagation delay, small pulse width distortion and small part-to-part skew to achieve the fast switching frequency, and better jitter and propagation delay performance. As the input stage uses an emulated diode (analog diode), these gate drivers offer long term reliability and excellent aging characteristics. The CA-IS3211 devices operate with dual supplies or a single supply of 10V to 30V (8V UVLO parts) or 14V to 30V (12V UVLO parts) wide voltage range of V_{CC} – V_{EE}, support unbalanced dual supplies operation, making them ideal to drive power MOSFET, IGBT or silicon-carbide(SiC) transistors in various inverter, power supply or motor drive applications. The CA-IS3211Vx offers single terminal gate drive output V_{OUT} and the CA-IS3211Sx offers dual separate output: OUTH and OUTL. All devices can be configured as low-side and high-side drivers. The driver output is pulled to low state to turn-off external power transistors when V_{CC} supply input is either not powered or is in UVLO. Undervoltage lockout (UVLO) with hysteresis is integrated on V_{CC} supply which ensure robust system performance under noisy conditions.

The CA-IS3211 devices are available either in a 6-pin or 8-pin wide-body SOIC packages with 8.5mm of creepage and clearance, also offer DUB8 small size package with 6.8mm creepage and 6.1mm clearance. All devices are rated for operation at -40°C to +150°C junction temperature. Higher operation temperature range extends gate driver designs in industrial and automotive applications with the high temperature environment that can not supported by optocoupler-based isolator. Figure 9-1 provides a conceptual block diagram of the CA-IS3211 isolated gate driver. It shows the main elements of CA-IS3211, including input stage, output stage, V_{CC} UVLO, digital isolator functional groups. Their operations are described separately in the following sections.

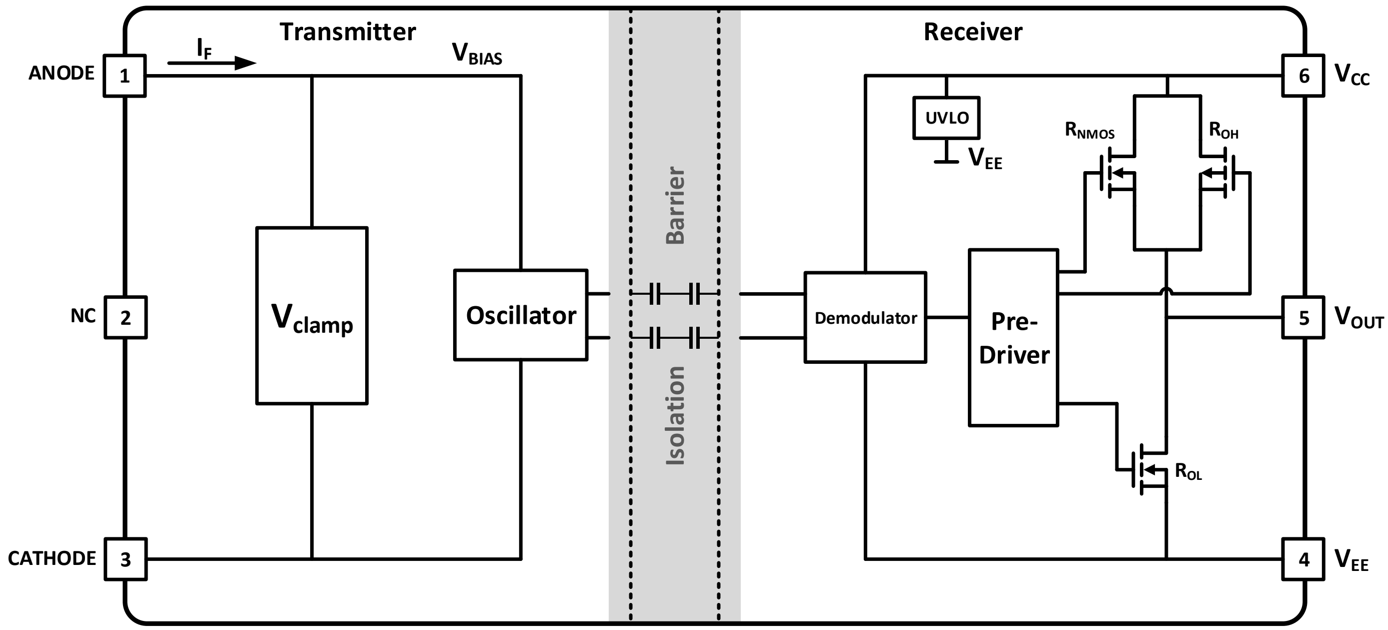


Figure 9-1. Functional block diagram

The CA-IS3211 devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO_2 based isolation barrier between circuits with different power domains. The isolation transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The isolation receiver demodulates the signal and recovery input signal at output-side through a buffer stage. With Chipanalog's full differential OOK capacitive isolation technology, the CA-IS3211 builds a robust data transmission path between different power domains and the wide-body package parts support up to 5.7kV$_{RMS}$ galvanic isolation between input-side and output-side, also features up to 150kV/µs common mode transient immunity, 1500V$_{RMS}$ working voltage, up to 8kV$_{PK}$ surge rating. This enables efficient signal transmission in noisy environments. The advanced full differential techniques can maximize CMTI performance and minimize the radiated emissions due the high frequency carrier and driver switching.

9.2. Input Stage

The input stage of CA-IS3211 integrated an analog diode with anode and cathode pins, see Figure 3-1 the CA-IS3211 input circuit in 6-pin SOIC package. There is no power supply and ground pins on the input-side. Applying a positive voltage between the anode and cathode, the analog diode is forward biased and a forward current I_F flows into the diode. The analog diode features 2.1V typical forward voltage. Like optocoupler-based gate drivers, an external resistor (R_{EXT} in the typical application circuits) is needed to limit the forward current. For the CA-IS3211 devices, the operating forward current range is 7mA to 16mA. If $I_F > I_{FLH}$(2.8mA, typ.), the isolation transmitter sends a high frequency carrier across the SiO_2 barrier and the isolation receiver demodulates this high-frequency signal and drive output V_{OUT} high; If the anode voltage drops below V_{F_HL} (0.9V, min.), or reverse biased, the gate driver output is put to low state. The reverse breakdown voltage of the CA-IS3211 input diode is >7V. Refer to Table 9-1 for the inputs vs. output truth table of the CA-IS3211.

Table 9-1. The CA-IS3211 Inputs vs. Output Truth Table

Input diode	V_{CC}	V_{OUT}
Turn off ($I_F < I_{FLH}$)	$UVLO_R$ to 30V	Low
Turn on ($I_F > I_{FLH}$)	$UVLO_R$ to 30V	High
X	0V to $UVLO_R$, $UVLO_F$ to 0V	Low

As an opto-compatible isolated gate driver, the CA-IS3211 family of products can be used as drop-in replacement for the industry standard optocoupler-based gate drivers. The key features and characteristics of the CA-IS3211 also bring significant performance and reliability improvement over opto-based gate drivers as flowing list:

1. High reliability and stability, since the analog diode does not use light emission for its operation, the operating point of input stage is very stable and predictable over operating temperature range. The dynamic impedance of the CA-IS3211 input diode is very small (<1.0Ω) and the temperature coefficient of the forward voltage drop is less than 1.35mV/°C. These advanced features lead to excellent stability of the forward current I_F across all operating conditions, provide better reliability and stability over full temperature range and life-time, also offer better part to part matching.
2. Smaller propagation delay and skew, due to Chipanalog's proprietary process technology, the CA-IS3211 drivers feature smaller pulse width distortion and less part to part propagation skew. The part-to-part propagation delay is matched within 25ns over the junction temperature range of -40°C to +150°C.
3. More robust, the CA-IS3211 silicon-based gate drivers can operate at higher ambient temperature range(up to 125°C), while most of opto-isolated gate drivers only operate up to 105°C. They also feature higher common mode transient immunity than opto isolated gate drivers.

9.3. Driver Output Stage

The output driver stage of the CA-IS3211 integrates a pull-up structure and a pull-down structure. They have distinct current sourcing/sinking capabilities to control the external transistors. Figure 9-2 shows the output stage circuit, in the output stage, a p-channel MOSFET and an additional n-channel MOSFET in parallel combined into the pull-up structure. The n-channel MOSFET only turns on for a short period of time during the output low-to-high transition and provides a boost current to enable the fast turn-on of the device. The on-resistance of this n-channel MOSFET (R_{NMOS}) is about 0.8Ω when activated. In Figure 9-2, R_{OH} (5.5Ω, typ.) is the on-resistance of the P-channel MOSFET only. This is because the n-channel MOSFET is placed in off state in DC condition and is turned on only for a very short time when the output is changing from low to high. Thus, the effective on-resistance(R_{NMOS} //R_{OH}) of the output pull-up stage during NMOS turn-on phase is much lower than R_{OH}.

The pull-down circuit of CA-IS3211 is simply composed of an n-channel MOSFET. R_{OL} in Figure 9-2 is the on-resistance of the pull-down n-channel MOSFET, the typical value of R_{OL} is 0.5Ω. Because of the very low turn-on impedance of the output stage MOSFETs, the CA-IS3211 isolated gate drivers provide rail-to-rail outputs (output voltage swings between V_{CC} and V_{EE}). Also, the CA-IS3211 family offers different output option, the CA-IS3211Vx offers single terminal gate drive output and the CA-IS3211Sx offers split output terminals: OUTH and OUTL.

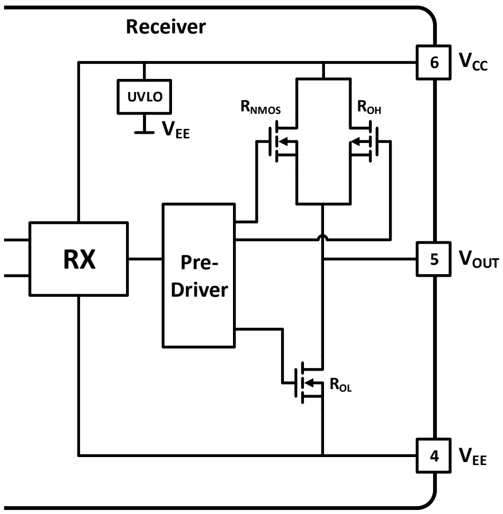


Figure 9-2. Driver output stage

When the V_{CC} supply is in power-off or UVLO condition, the high-side p-channel MOSFET and n-channel MOSFET are held off while the low-side n-channel MOSFET gate is connected to the driver output through a clamp resistor (about 500kΩ). This active clamp circuit holds driver outputs to the threshold voltage of the lower n-channel MOSFET(less than 2.0V) or low state, to turn off the external power transistors when no power is connected to the V_{CC} supply. This prevents the external power transistors from falsely turning on during V_{CC} power off or UVLO.

The output stage of the CA-IS3211 also features short-circuit clamping function that clamp the driver output voltage and pull the V_{OUT} slightly higher than V_{CC} supply during short-circuit conditions. This protects the external transistors from overvoltage breakdown. The internal conduction diode can support up to 500mA @10µs pulse current and 20mA continuous current. An external diode can be used to provide larger current conduction capability.

9.4. Undervoltage Lockout (UVLO)

The CA-IS3211 supply (V_{CC}-V_{EE}) is internally monitored for undervoltage conditions. The supply terminal V_{CC} undervoltage detection places the driver output in low state(default state) during an undervoltage event: V_{CC} < $UVLO_R$ during power on, or V_{CC} < $UVLO_F$ during power-down or during normal operation due to a sagging supply voltage. Low state output turn off the external power transistor regardless of the state of the input to avoid under-driven condition on IGBTs and MOSFETs, see Figure 9-3 for more details. The V_{CC} UVLO has hysteresis to avoid chattering when there is ground noise from the power supply, also allows the device to accept small drops in supply voltage and ensures stable operation. Table 9-1 illustrate the output behavior during V_{CC} undervoltage conditions.

Note that before the device enters normal operation and get ready to provide driver output correctly, there is a power-up delay from UVLO rising edge to driver output. This delay time is defined as t_{UVLO_rec} as shown in Figure 9-3. Designers need to leave proper margin before sending PWM signal to gate driver after the V_{CC} supply is ready.

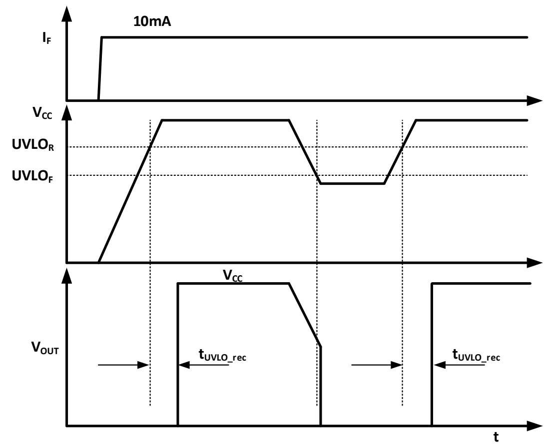


Figure 9-3. UVLO timing diagram

10. Application and Implementation

10.1. Typical Application Circuit

The CA-IS3211 isolated gate drivers are designed to drive power MOSFET, IGBT or silicon-carbide(SiC) transistors in various power supply systems to optimize system cost and efficiency. This family of devices can be configured as low-side and high-side drivers. The default-low output keeps the output in low state when V_{CC} supply is in UVLO or power off. The high CMTI rating of 150kV/µs (min) @ at 1500V common mode voltages, UVLO detection and the propagation delay matching of 25ns (max) part to part make the CA-IS3211 devices ideal to drive high-power transistors in motor drives, industrial inverters, isolated power supply etc. high reliability applications. Figure 10-1 and Figure 10-2 provide the CA-IS3211 typical application circuits for IGBT driving.

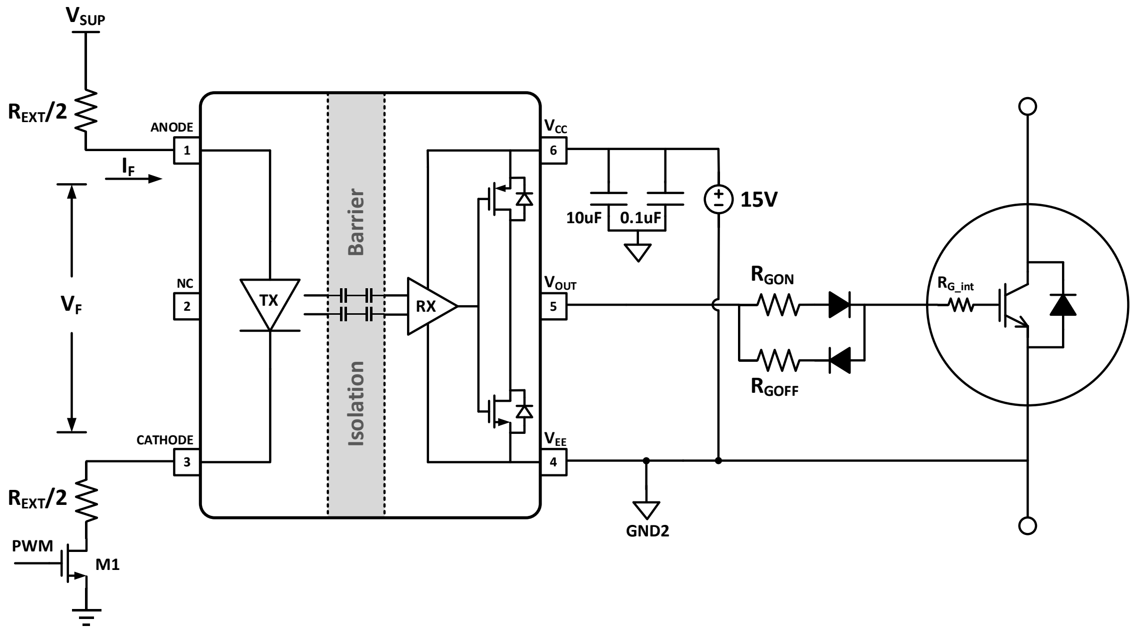


Figure 10-1. Typical application circuit with NMOS & current limit resistor at input side

The gate driver is typically placed between micro-controller (that is MCU or FPGA) and power transistors. As the CA-IS3211 input stage requires 7mA to 16mA forward current to drive the anode to turn-on input diode, most MCUs are not capable of providing enough forward current for this design, an external buffer is needed between the MCU output and CA-IS3211 input in the typical applications, see Figure 10-2. Usually, the buffer power supply is 3.3V or 5.0V, while the forward voltage drop of input diode is typically 2.1V (1.8V to 2.4V) with 1.35mV/°C tempco, need to add a resistor R_{EXT} before the CA-IS3211 input to limit the forward current. For the input resistor selection, see the Input Current Limit section for more details.

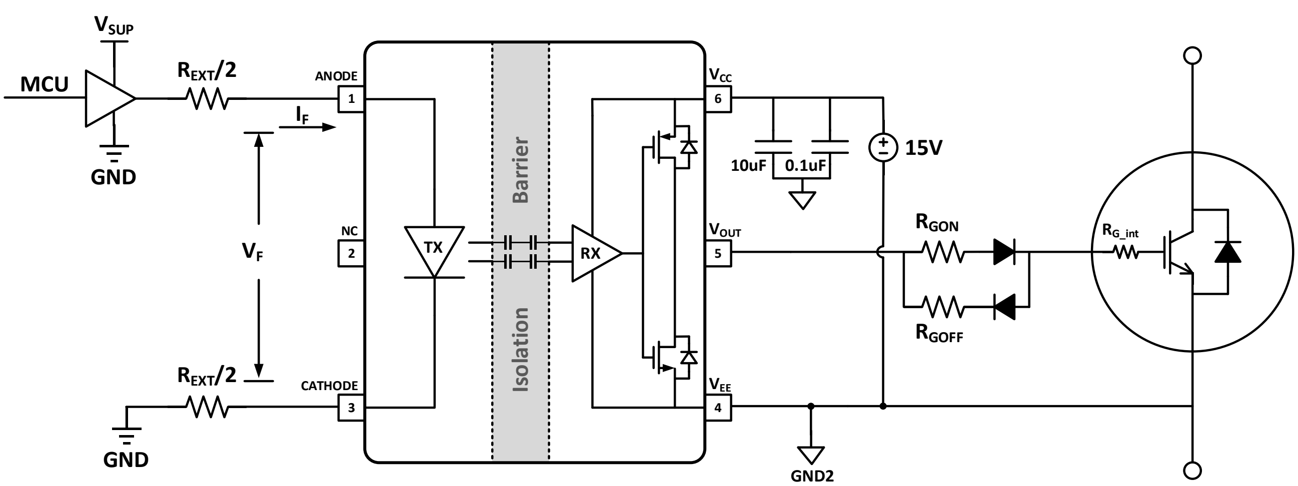


Figure 10-2. Typical application circuit with input buffer and current limit resistor

On the output-side, the power supply V_{CC} can be as high as 30V (32V abs max). The V_{CC} supply can be a single isolated supply up to 30V or isolated bipolar supply such that V_{CC}-V_{EE} does not exceed 30V, or it can be bootstrapped with external diode and capacitors if the system uses a single power supply respected to the power ground. For most operation with single supply, the V_{CC} pin is connected to 15V with respect to ground for IGBT driver, and 20V for SiC MOSFET driver; connect the V_{EE} pin to GND.

For most operation with dual-supplies, the power transistors are turned off with a negative voltage on the gate with respect to the emitter or source. This configuration can prevent the power transistors from unintentionally turning on because of current induced from the Miller effect. The typical supply voltage of the V_{CC} and V_{EE} for bipolar operation are 15V and -8V with respect to GND for IGBT driver, and 20V and -5V for SiC MOSFET driver. Bypass V_{CC} and V_{EE} (for bipolar operation) with at least 10μF/50V low-ESR and low-ESL capacitors to GND. An additional 0.1μF /50V capacitor in parallel with the device biasing capacitor for high frequency filtering. To ensure the best performance, place the decoupling capacitors as close to the power-supply pin as possible.

10.2. Interlock configuration

In the typical applications, the gate drivers are used to drive high-side and low-side power transistors. The MCU generates complementary PWM pulses during normal operation. However, MCU failures or software faults can cause both the high-side and low-side PWM signals from the MCU to latch high. Interlock configuration can be used to prevent the output from being high at same time even both high-side and low-side inputs are pulled high. As shown in Figure 10-3, the anode of the high-side driver's input diode is connected to the cathode of the low-side driver's input diode. The cathode of the high-side driver's input diode is connected to the anode of the low-side driver's input diode. This architecture prevents both the input diodes from being "ON" at the same time, preventing shoot through in the external power transistors.

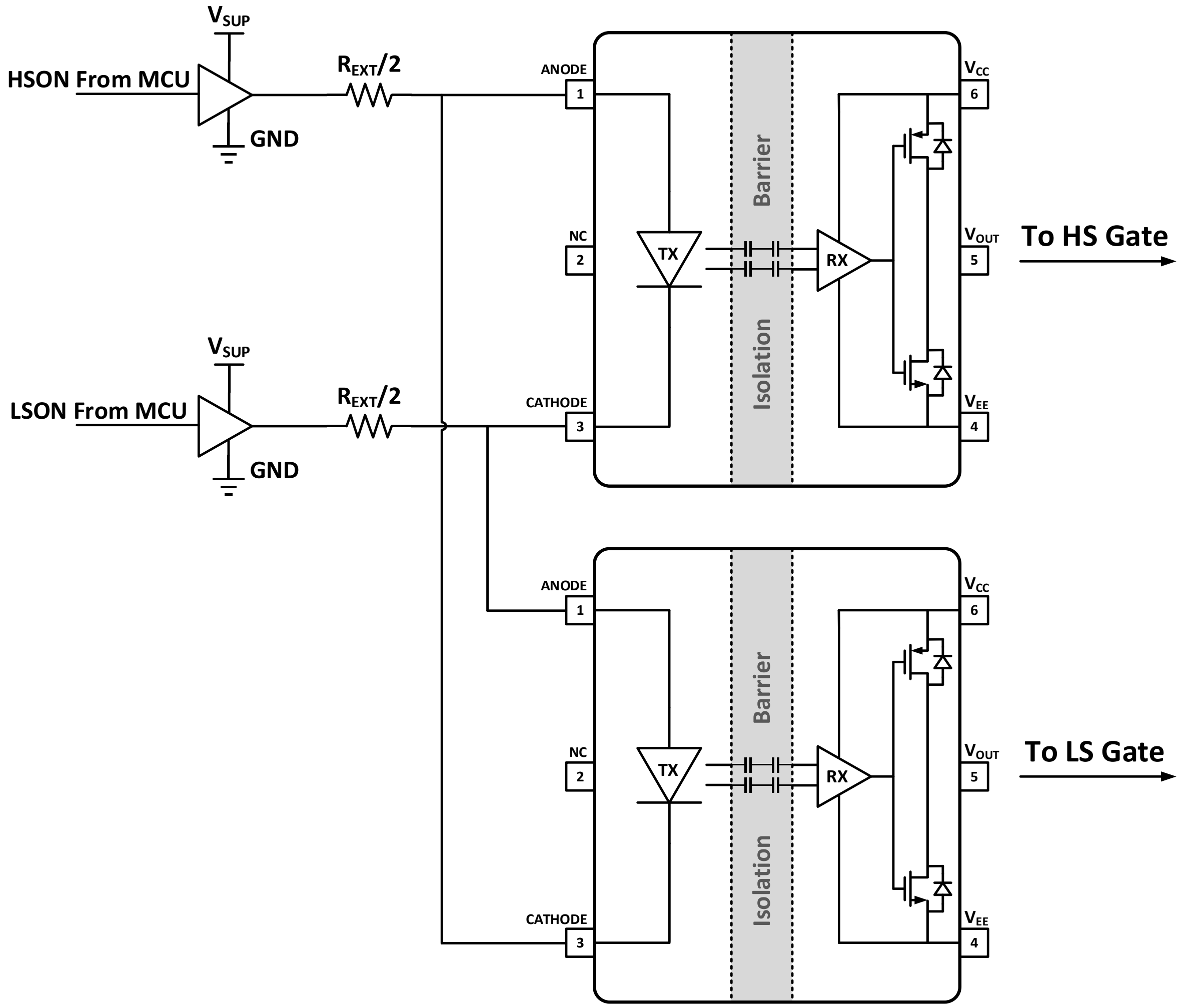


Figure 10-3. Interlock configuration

10.3. Input Current Limit

It is important to select a suitable resistor R_{EXT} to keep the diode forward current within 7mA to 16mA, and must be less than 16mA over the temperature range. The typical value of input diode forward threshold (I_{FLH}) is 2.8mA. In Figure 10-2 application circuit, the R_{EXT} is determined as follows:

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{OH\_buf}$$

Where,

- I_F is input forward current, the typical value is 10mA, with 7mA minimum value and 16mA maximum value;
- V_{SUP} is the supply voltage of the buffer, typical value is 5V ±5%;
- V_F is the forward voltage drop of input diode, typical value is 2.1V (1.8V minimum value and 2.4V maximum value);
- R_{OH_buf} is the buffer's output resistances, typical value is 18Ω (13Ω minimum value and 22Ω maximum value).

Calculate the external resistor R_{EXT} using the above equation,

R_{EXT} =262Ω (typ), or 196Ω to 300Ω

To turn the input diode off, the voltage between anode and cathode should be less than 0.8V, or $I_F < I_{FLH}$. The input diode can also be reverse biased up to 7V to turn it off and put the gate driver output low.

10.4. Driver Output Resisters Selection

In the typical application circuits Figure 10-1 and Figure 10-2, there are two external gate driver resistors: R_{GOFF} and R_{GON}, R_{GOFF} is the external turn-off resistance; R_{GON} is the external turn-on resistance. These two resistors are chosen to limit the ringing caused by fast switching and parasitic inductances and capacitances, reduce EMI, also can be used to fine-tune gate drive strength and optimize the switching loss. Use the following equations to estimate R_{GOFF} and R_{GON} resistor values,

I_{OH} peak current calculation:

$$I_{OH} = \min\left[5A, \quad \frac{V_{CC} - V_{EE}}{\left(R_{NMOS} || R_{OH} + R_{GON} + R_{GFET_{int}}\right)}\right]$$

Where $R_{GFETint}$ is the gate resistance of the external power transistor, this number is available from power transistor data sheet. R_{NMOS} is 0.8ohm. R_{OH} is 5.5ohm.

I_{OL} peak current calculation:

$$I_{OL} = \min\left[6A, \quad \frac{V_{CC} - V_{EE}}{\left(R_{OL} + R_{GOFF} + R_{GFET_{int}}\right)}\right]$$

Where $R_{GFETint}$ is the gate resistance of the external power transistor, this number is available from power transistor data sheet. R_{OL} is 0.5ohm.

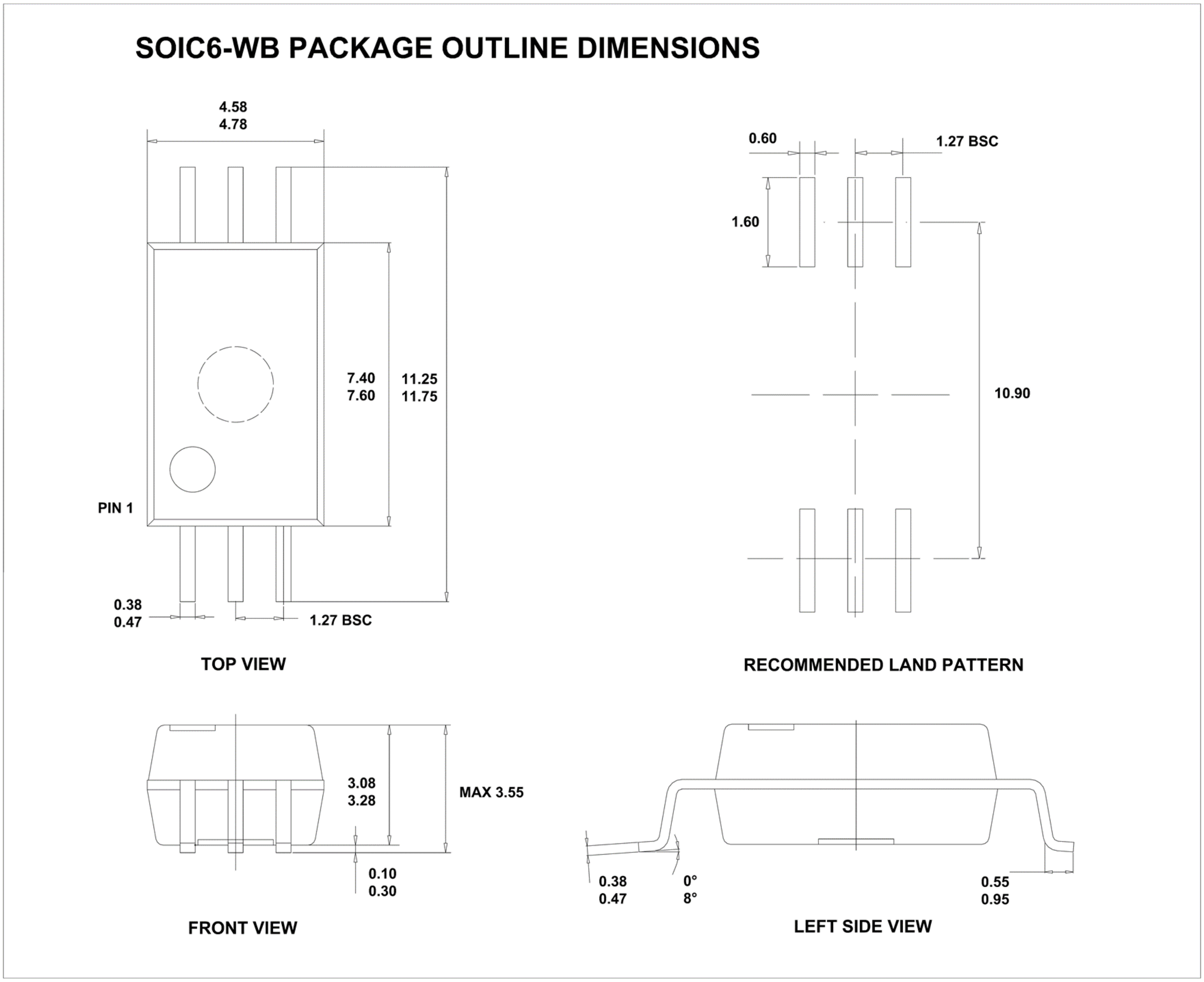
10.5. PCB Layout

Due to high current levels and fast switching(high dv/dt and di/dt) that radiate noise, proper PC board layout is essential. Follow these guidelines for good PCB layout:

- To ensure the best performance and keep lower supply ripple, place the decoupling capacitors as close to the power-supply pin as possible. We recommend to use low ESR, low ESL MLCC capacitors.
- VOUT connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency-switching operation. This implies that the VOUT loop areas should be minimized. Additionally, small current loop areas reduce radiated EMI. Place the external transistor as close to the gate driver as possible.
- Connect the supply pins (V_{CC}, V_{EE}) to as large a copper pour or plane area as possible for best heat-sinking.
- To ensure isolation performance between the primary side and secondary side, on the top layer and bottom layer keep the space under the CA-IS3211 device free from traces, vias, and pads to maintain maximum creepage distance.
- For the multiple layers design, it is recommended to connect the V_{CC} and V_{EE} pins to internal ground or power planes through multiple vias. These vias should be located close to the IC pins to maximize thermal conductivity, also keep lower parasitic value.

11. Package Information

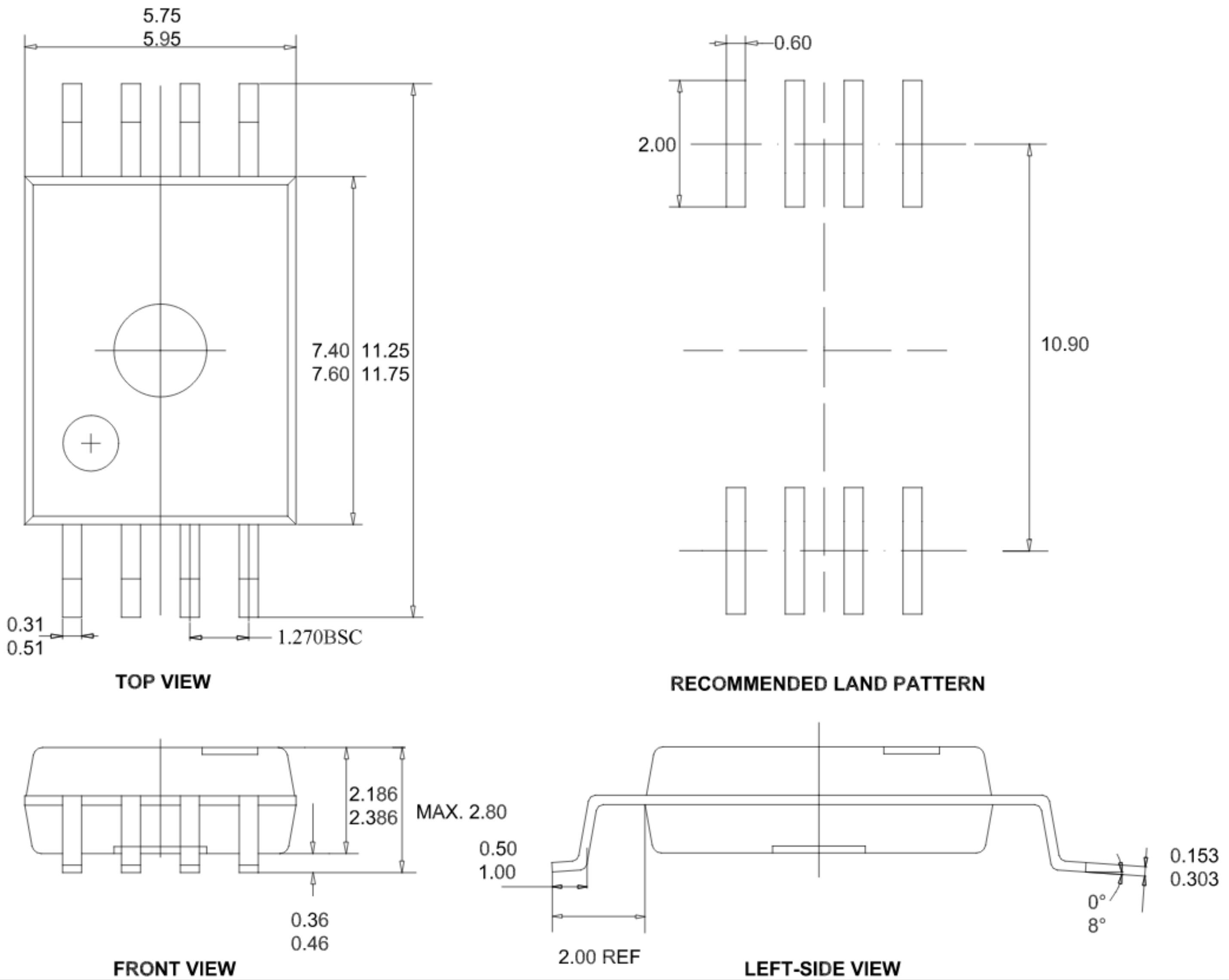
11.1. 6-Pin Wide Body SOIC Package Outline



Note:

1. All dimensions are in millimeters, angles are in degrees.

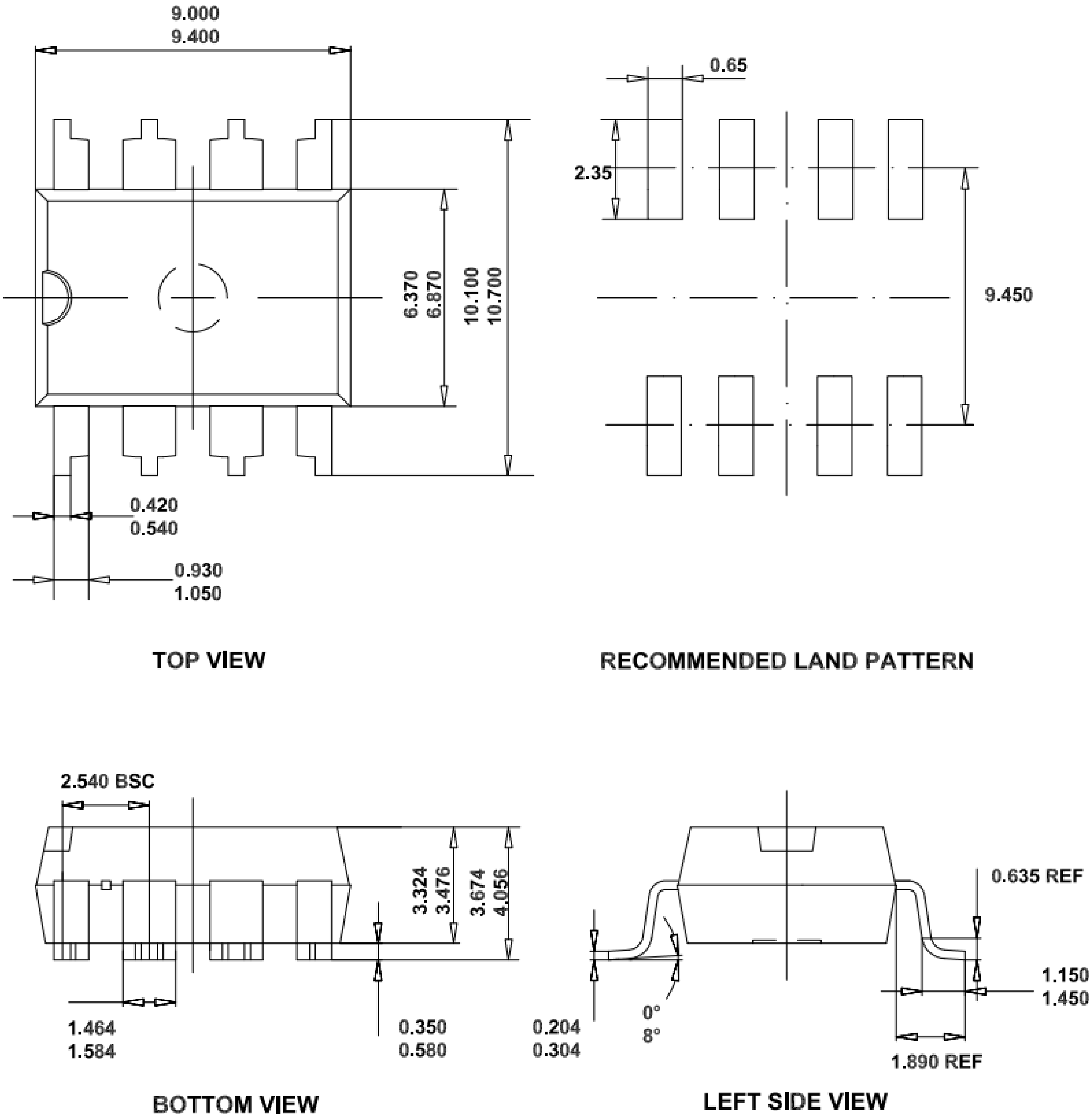
11.2. 8-Pin Wide Body SOIC Package Outline



Note:

1. All dimensions are in millimeters, angles are in degrees.

11.3. 8-Pin DUB8 Package Outline



Note:
1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

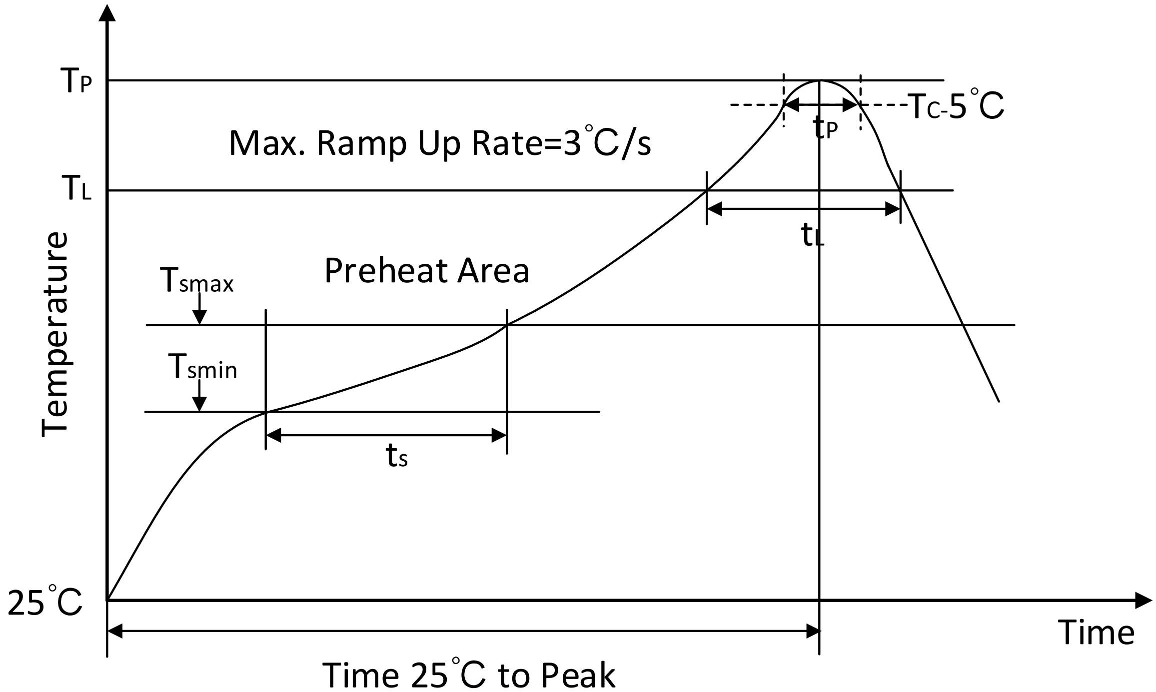


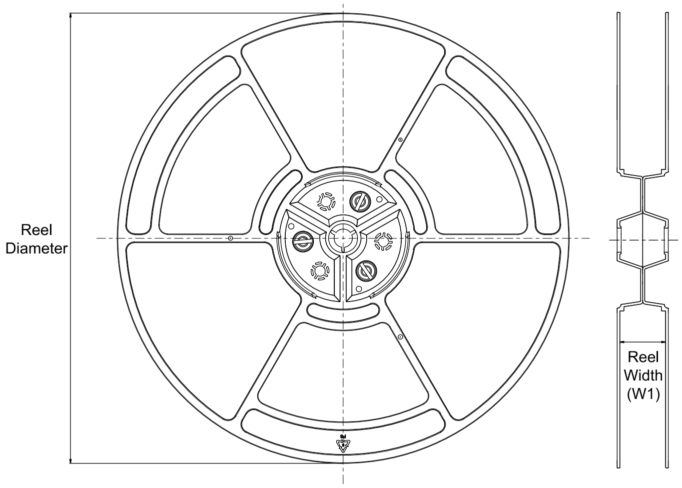
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

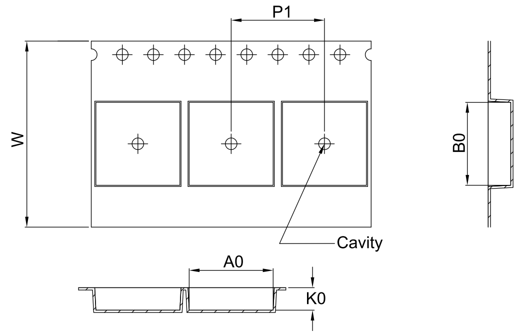
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3 ℃ /second max
Time of Preheat temp(from 150 ℃ to 200 ℃)	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃ of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25 ℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

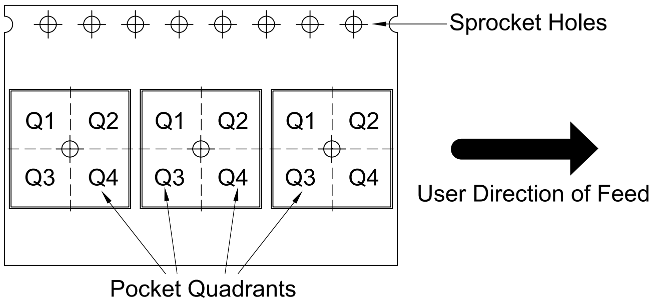


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3211VBJ	SOIC	J	6	1000	330	16.40	11.95	4.98	3.95	16.00	16.00	Q1
CA-IS3211VCJ	SOIC	J	6	1000	330	16.40	11.95	4.98	3.95	16.00	16.00	Q1
CA-IS3211VBG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211VCG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211SBG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211SCG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211VBU	DUB	U	8	800	330	24.40	10.90	9.60	4.30	16.00	24.00	Q1
CA-IS3211VCU	DUB	U	8	800	330	24.40	10.90	9.60	4.30	16.00	24.00	Q1

14. Important statement

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