CA-IS3720VLS High-Speed Dual-Channel Digital Isolators

1. Features

- **Data rate: DC to 150Mbps**
- **Robust isolation barrier**
  - High lifetime: >40 years
  - Up to 3750 V_{RMS} isolation rating
  - ±150 kV/µs typical CMTI
- **Wide supply range: 1.8V to 5.5V**
- **Wide operating temperature range: -40°C to 125°C**
- **No start-up initialization required**
- **Schmitt trigger inputs**
- **Default low-level output**
- **High electromagnetic immunity**
- **Low power consumption**
  - 1.5mA per channel at 1Mbps with V_{DD} = 5.0V
  - 6.6mA per channel at 100Mbps with V_{DD} = 5.0V
- **Best in class propagation delay and skew**
  - 12ns typical propagation delay
  - 2ns propagation delay skew (chip -to-chip)
  - 1ns pulse width distortion
  - 5ns minimum pulse width
- **Narrow-body SOIC8(S) package**
- **Safety regulatory approvals**
  - VDE 0884-11 isolation certification
  - UL according to UL1577
  - IEC 62368-1, IEC 61010-1, GB 4943.1-2011 and GB 8898-2011 certifications

2. Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated Interfaces.

3. General Description

The CA-IS3720VLS is high-performance dual - channel digital isolator with up to 3.75kV_{RMS} isolation rating. This device can operate as low as 1.8V supply voltage with up to 100Mbps data rate. The CA-IS3720VLS provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS digital I/O. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier, and each channel input integrated Schmitt trigger to provide excellent noise immunity.

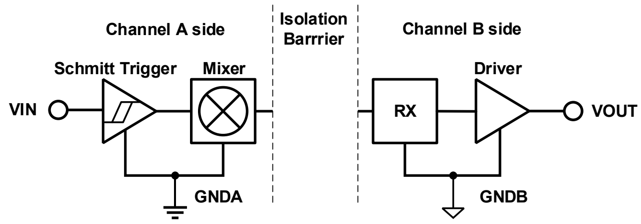
The CA-IS3720VLS features two channels transferring digital signals in one direction for applications such as isolated digital I/O. Also, this device offers default outputs. When the input is either not powered or is open-circuit, the default output of CA-IS3720VLS is low.

The CA-IS3720VLS is specified over the -40°C to +125°C operating temperature range and is available in 8-pin SOIC narrow body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3720VLS	SOIC8 (S)	4.90 mm × 3.90 mm

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV_{RMS})	Output Enable	Package
CA-IS3720VLS	2	0	Low	3.75	N/A	SOIC8

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5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	Updated UL certification informaiton	7
Version 1.02	Updated VDE certification informaiton	7

6. Pin Configuration and Functions

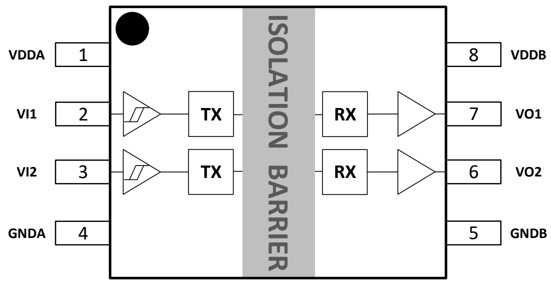


Figure 6-1. CA-IS3720VLS 8-Pin SOIC Narrow body Package Top View

Table 6-1. Pin description for the CA-IS3720VLS 8-Pin SOIC Narrow body package

SOIC8 Pin# CA-IS3720	Name	Type	Description
1	VDDA	Supply	Power supply for side A.
2	VI1	Digital I/O	Digital input 1 on side A/B, corresponds to logic output 1 on side B/A.
3	VI2	Digital I/O	Digital input 2 on side A/B, corresponds to logic output 2 on side B/A.
4	GNDA	Ground	Ground reference for side A.
5	GNDB	Ground	Ground reference for side B.
7	VO1	Digital I/O	Digital output 1 on side B/A, VO1 is the logic output for the VI1 input on side A/B.
6	VO2	Digital I/O	Digital output 2 on side B/A, VO2 is the logic output for the VI2 input on side A/B.
8	VDDB	Supply	Power supply for Side B.

7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage[2]	-0.5	7.0	V
V_{IN}	Voltage at VIx, VOx, ENx	-0.5	$V_{DD\_}$ + 0.5[3]	V
I_O	Output current	-20	20	mA
T_J	Operating Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:
1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 7 V.

7.2. ESD Ratings

		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±6000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	

7.3. Recommended Operating Conditions

Parameters			Minimum value	Typical value	Maximum value	Unit
V_{DDA}, V_{DDB}	Supply Voltage		1.7	1.8/2.5/3.3/5.0	5.5	V
$V_{DD(UVLO+)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Rising		1.5	1.57	1.64	V
$V_{DD(UVLO-)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Falling		1.4	1.49	1.5	V
$V_{HYS(UVLO)}$	V_{DD} Undervoltage-Lockout Threshold Hysteresis		50	80	100	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
		V_{DDO} = 1.8V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			1	
		V_{DDO} = 1.8V			1	
V_{IH}	High-level Input Voltage		1.5			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
TA	Ambient Temperature		-40	27	125	°C

Note:
1. V_{DDO} = Output-side supply V_{DD}.

7.4. Thermal Information

Thermal Metric		CA-IS3720VLS SOIC8-NB(S)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.0	°C/W

7.5. Power Ratings

Parameters		Test Conditions	Minimum value	Typical value	Maximum value	Unit
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave			120	mW
P_{DA}	Maximum Power Dissipation on Side-A				20	mW
P_{DB}	Maximum Power Dissipation on Side-B				100	mW

7.6. Insulation Specifications

Parameters		Test Conditions	Value S	Unit
CLR	External clearance	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	19	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	N/A	
DIN V VDE V 0884-17:2021-10[1]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage [2]	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	4070	V_{PK}
q_{pd}	Apparent charge [3]	Method a, After Input-Output safety test subgroup 2/3, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.2 × VIORM, t_m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, Vini = V_{IOTM}, tini = 60 s; Vpd(m) = 1.6 × V_{IORM}, t_m = 10 s	≤5	
		Method b, At routine test (100% production) and preconditioning (type test) Vini = 1.2 × V_{IOTM}, tini = 1 s; Vpd(m) = 1.875 × V_{IORM}, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output [4]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance [4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	3750	V_{RMS}

Notes:

1. This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7. Safety-Related Certifications

VDE	UL	TUV
Certified according to DIN VDE V 0884-17:2021-10.	Certified according to UL 1577 Component Recognition Program	Certified according to EN 61010-1:2010+A1
Maximum transient isolation voltage：5300V_{pk}(SOIC8-NB) Maximum repetitive peak isolation voltage：566V_{pk}(SOIC8-NB) Maximum surge isolation voltage：4070V_{pk}(SOIC8-NB)	3750 VRMS(SOIC8-NB)	3750 VRMS(SOIC8-NB)
Certification Number：40052786	Certification Number：E511334	Certification Number：CN23RC4J001

7.8. Electrical Characteristics

$V_{DDA} = V_{DDB}$ = 5 V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See Figure 8-1	V_{DDO}[1]-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See Figure 8-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		2.0			V
$V_{IT-(IN)}$	Falling input switching threshold				0.8	V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at INx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	$V_I = V_{DDI}$[1]or 0 V, V_{CM} = 1200 V; See Figure 8-3	100	150		kV/µs
C_I	Input Capacitance[3]	$V_I = V_{DD}/2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, V_{DD} = 5V		2		pF

Notes:
1. V_{DDI} = Input-side VDD supply voltage, V_{DDO} = Output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

$V_{DDA} = V_{DDB}$ = 3.3 V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -2mA; See Figure 8-1	V_{DDO}[1]-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA; See Figure 8-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		2.0			V
$V_{IT-(IN)}$	Falling input switching threshold				0.8	V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at Ax or Bx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	VI = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See Figure 8-3	100	150		kV/µs
C_I	Input Capacitance[3]	$V_I = V_{DD}/2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, V_{DD} = 3.3 V		2		pF

Notes:
1. V_{DDI} = Input-side VDD supply voltage, V_{DDO} = Output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

$V_{DDA} = V_{DDB}$ = 2.5 V ± 5%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -1mA; See Figure 8-1	V_{DDO}[1]-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 1mA; See Figure 8-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		2.0			V
$V_{IT-(IN)}$	Falling input switching threshold				0.8	V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at Ax or Bx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	VI = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See Figure 8-3	100	150		kV/µs
C_I	Input Capacitance[3]	$V_I = V_{DD}/2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, V_{DD} = 3.3 V		2		pF

Notes:
1. V_{DDI} = Input-side VDD supply voltage, V_{DDO} = Output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

$V_{DDA} = V_{DDB}$ = 1.8 V ± 5%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See Figure 8-1	V_{DDO}[1]-0.4	1.6		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See Figure 8-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.5			V
$V_{IT-(IN)}$	Falling input switching threshold				0.8	V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at Ax or Bx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	VI = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See Figure 8-3	100	150		kV/µs
C_I	Input Capacitance[3]	$V_I = V_{DD}/2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, V_{DD} = 3.3 V		2		pF

Notes:
1. V_{DDI} = Input-side VDD supply voltage, V_{DDO} = Output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

7.9. Supply Current Characteristics

$V_{DDA} = V_{DDB}$ = 5 V ± 10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3720							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3720VLS)		I_{DDA}		0.9	1.3	mA
			I_{DDB}		1.4	2.2	
	$V_{IN} = V_{DDI}$ [1] (CA-IS3720VLS)		I_{DDA}		2.5	4.1	
			I_{DDB}		1.5	2.3	
Supply Current – AC Signal	All Channels Switching with 5V, 50% Duty Cycle Square Wave Clock Input; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		1.7	2.7	
			I_{DDB}		2.2	3.2	
		10Mbps (5MHz)	I_{DDA}		1.8	2.9	
			I_{DDB}		8.8	11.8	
		100Mbps (50MHz)	I_{DDA}		2.5	3.9	
			I_{DDB}		22	30.0	

Note:
1. V_{DDI} = Input-side supply voltage V_{DD}.

$V_{DDA} = V_{DDB}$ = 3.3 V ± 10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3720							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3720VLS)		I_{DDA}		0.8	1.3	mA
			I_{DDB}		1.3	2.0	
	$V_{IN} = V_{DDI}$ [1] (CA-IS3720VLS)		I_{DDA}		2.4	4.0	
			I_{DDB}		1.4	2.2	
Supply Current – AC Signal	All Channels Switching with 3.3V, 50% Duty Cycle Square Wave Clock Input; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		1.6	2.7	
			I_{DDB}		1.9	2.7	
		10Mbps (5MHz)	I_{DDA}		1.7	2.7	
			I_{DDB}		6.2	8.4	
		100Mbps (50MHz)	I_{DDA}		2.2	3.5	
			I_{DDB}		14.4	19.7	

Note:
1. V_{DDI} = Input-side supply V_{DD} .

$V_{DDA} = V_{DDB}$ = 2.5 V ± 5%, T_A = -40 to 125°C

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3720							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3720VLS)		I_{DDA}		0.8	1.2	mA
			I_{DDB}		1.4	2.0	
	$V_{IN} = V_{DDI}$ [1] (CA-IS3720VLS)		I_{DDA}		2.4	4.0	
			I_{DDB}		1.4	2.1	
Supply Current – AC Signal	All Channels Switching with 2.5V, 50% Duty Cycle Square Wave Clock Input; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		1.6	2.6	
			I_{DDB}		1.7	2.5	
		10Mbps (5MHz)	I_{DDA}		1.7	2.7	
			I_{DDB}		5.0	6.8	
		100Mbps (50MHz)	I_{DDA}		2.1	3.4	
			I_{DDB}		10.8	14.7	

Note:
1. V_{DDI} = Input-side supply V_{DD}.

$V_{DDA} = V_{DDB}$ = 1.8 V ± 5%, T_A = -40 to 125°C

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3720							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3720VLS)		I_{DDA}		0.8	1.2	mA
			I_{DDB}		1.3	1.8	
	$V_{IN} = V_{DDI}$ [1] (CA-IS3720VLS)		I_{DDA}		3.2	4.7	
			I_{DDB}		1.3	1.9	
Supply Current – AC Signal	All Channels Switching with 2.5V, 50% Duty Cycle Square Wave Clock Input; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		1.9	2.8	
			I_{DDB}		1.7	2.5	
		10Mbps (5MHz)	I_{DDA}		1.9	2.7	
			I_{DDB}		5.3	7.1	
		100Mbps (50MHz)	I_{DDA}		2.4	3.5	
			I_{DDB}		11.2	15.0	

Note:
1. V_{DDI} = Input-side supply V_{DD}.

7.10. Timing Characteristics

$V_{DDA} = V_{DDB}$ = 5 V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Chip -to-chip Output Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2		0.1	0.3	μs
t_{SU}	Start-up Time			15	40	μs

Notes:
1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

V_{DDA} = V_{DDB} = 3.3V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Chip -to-chip Output Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2		0.1	0.3	µs
t_{SU}	Start-up Time			15	40	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

V_{DDA} = V_{DDB} = 2.5V ± 5%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$			0.2	5.0	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Chip -to-chip Output Skew Time[2]			2.0	5.0	ns
t_r	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2		0.1	0.3	µs
t_{SU}	Start-up Time			15	40	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

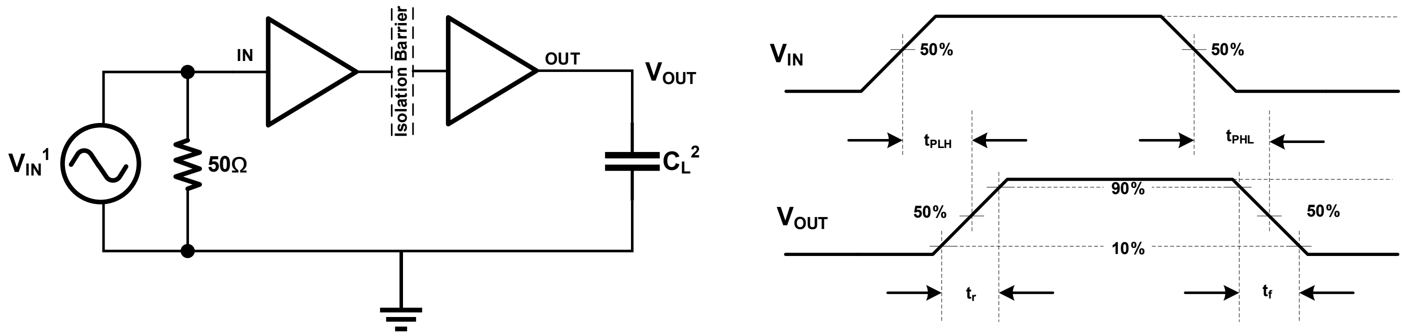
V_{DDA} = V_{DDB} = 1.8V ± 5%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		100	Mbps
PW_{min}	Minimum Pulse Width				10	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	See Figure 8-1	5.0	16	22	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$			0.2	5.0	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Chip -to-chip Output Skew Time[2]			1.0	5.0	ns
t_r	Output Signal Rise Time	See Figure 8-1		2.5	4.0	ns
t_f	Output Signal Fall Time	See Figure 8-1		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2		0.1	0.3	µs
t_{SU}	Start-up Time			15	40	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

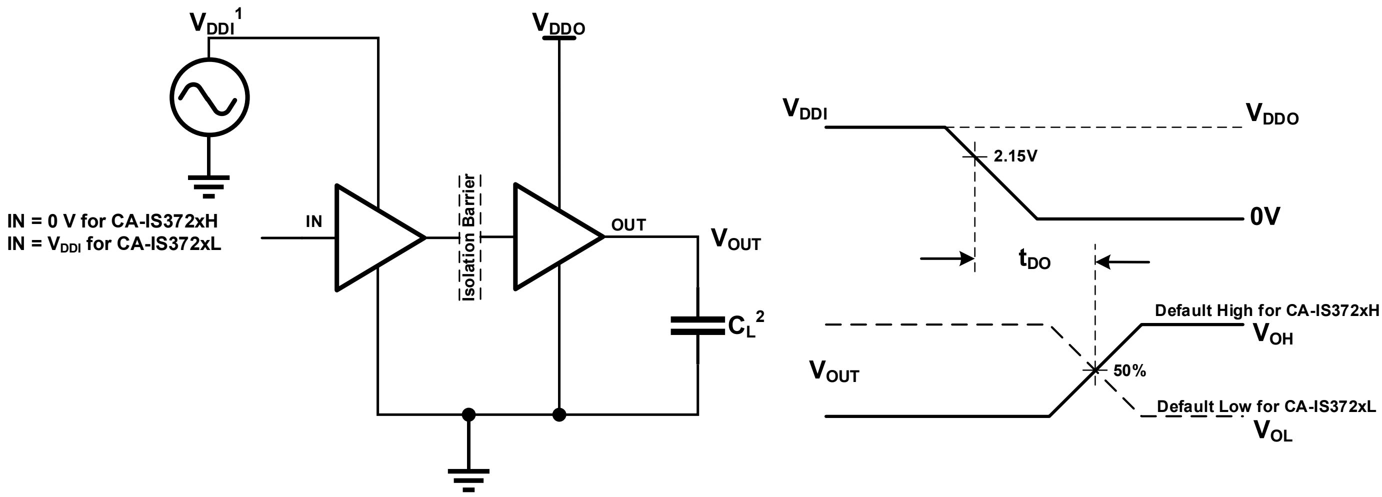
8. Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with characteristics: frequency ≤100kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns, Z_{out} = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

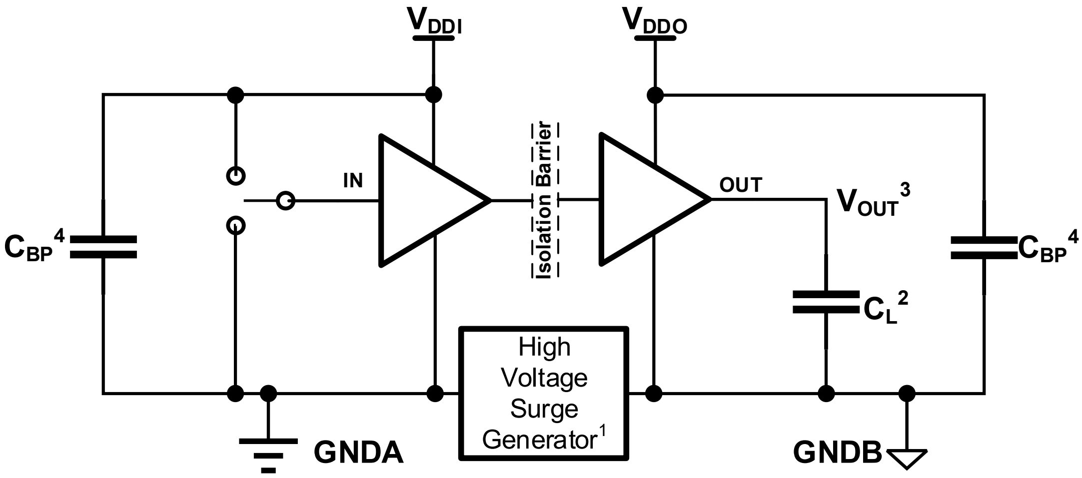
Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



Notes:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should be over 2.15V and less than 5.5V.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2. Default Output Delay Time Test Circuit and Voltage Waveforms



Notes:

1. The High Voltage Surge Generator generates repetitive surges with > 1kV, <10ns rise time and fall time to reach common-mode transient noise with > 100kV/µs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges occurs.
4. C_{BP} is bypass capacitor, 0.1uF ~ 1uF.

Figure 8-3. Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Overview

The CA-IS3720VLS is 2-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. This device has an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO_2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, the CA-IS3720VLS builds a robust data transmission path between different power domains, without any special start-up initialization requirements.

This device also incorporates advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 9-1, shows a functional block diagram of a typical channel; Figure 9-2 shows the operating waveform of a typical channel.

9.2. Functional Block Diagram

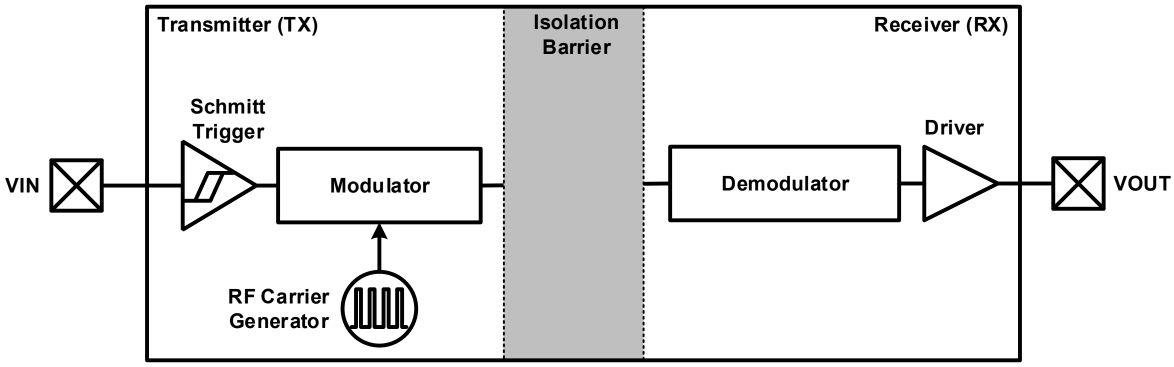


Figure 9-1. Functional Block Diagram of a Single Channel

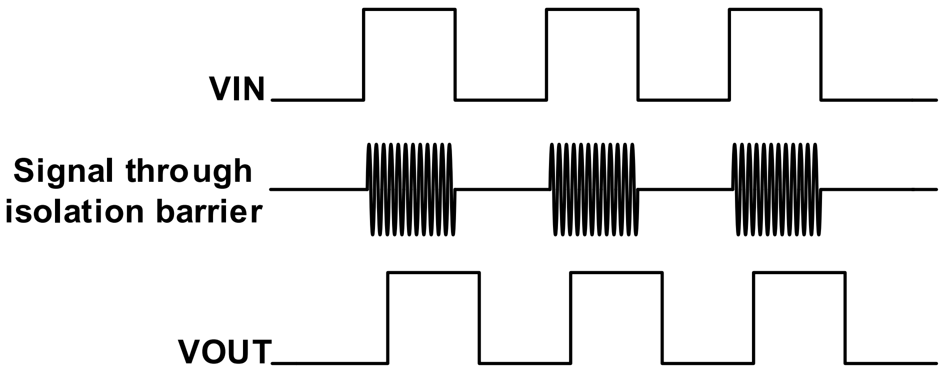


Figure 9-2. Conceptual Operation Waveform of a Single Channel

9.3. Device Operation Modes

Table 9-1 lists the operation modes for the CA-IS3720VLS device.

Table 9-1. Operation Mode Table

V_{DDI}[1]	V_{DDO}	INPUT(Ax/Bx) [2]	OUTPUT (Ax/Bx)	OPERATION
PU	PU	H	H	Normal operation mode: A channel output follows the logic state of the input.
		L	L	
		Open	Default	Default output, fail-safe mode: If a channel input is open, the corresponding channel output goes to the default logic state (Low for CA-IS3720VLS)
PD	PU	X	Default	Default output, fail-safe mode: When V_{DDI} is unpowered, the corresponding channel output goes to the default logic state (Low for CA-IS3720VLS)
X	PD	X	Undetermined	When V_{DDO} is unpowered, the output states are undetermined.[3]

Notes:
1. V_{DDI} = Input-side supply V_{DD}; V_{DDO} = Output-side supply V_{DD}; PU = Powered up ($V_{DD\_} \geq V_{DD(UVLO+)}$); PD = Powered down ($V_{DD\_} \leq V_{DD(UVLO\_)}$); X = Irrelevant; H = High level; L = Low level.
2. A strongly driven input signal can weakly power the floating VDD through an internal protection diode and cause undetermined output.
3. The outputs are in undetermined state when $V_{DD(UVLO+)} < V_{DDI}$, $V_{DDO} < V_{DD(UVLO-)}$.

10. Application and Implementation

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, Chipanalog's digital isolators, like the CA-IS3720VLS, only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1µF to 1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10-1 and Figure 10-2 show typical operating circuit of the CA-IS3720VLS and the CA-IS37xx family of digital isolators.

The CA-IS3720VLS does not require special power supply sequencing. The output logic high level is set independently by V_{DDB} supply voltage. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard. The PCB designer should follow some critical recommendations in order to get best performance. For high-speed signal circuit boards, we recommend to use the standard FR4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Layer order from top-to-bottom is: high-speed signal layer, ground plane, power plane, and low-frequency signal layer. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals. Keep the area underneath the digital isolator ICs free from ground and signal planes.

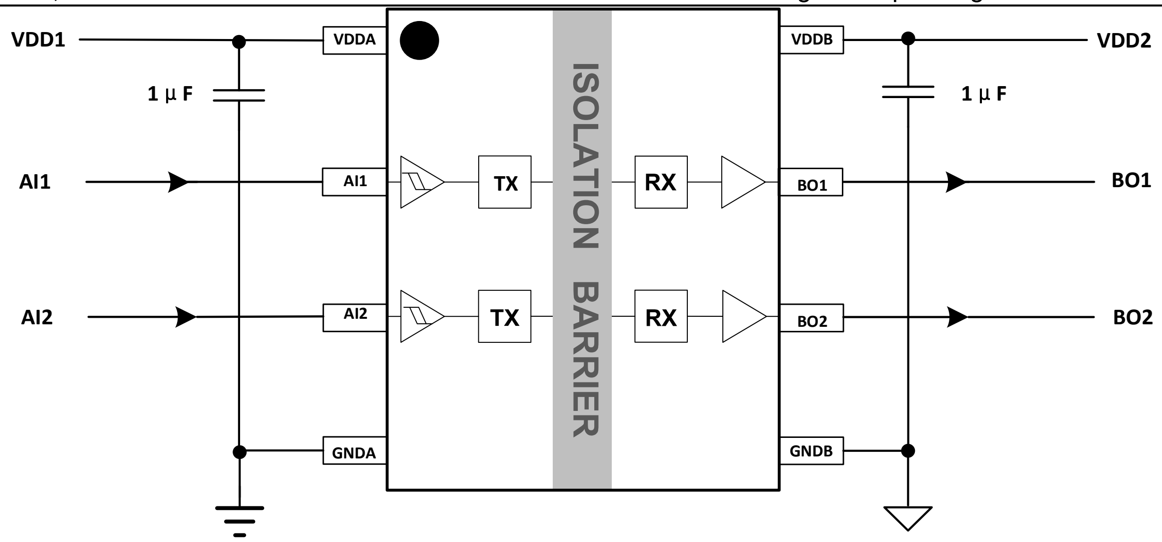


Figure 10-1. CA-IS3720 Typical Application Schematic

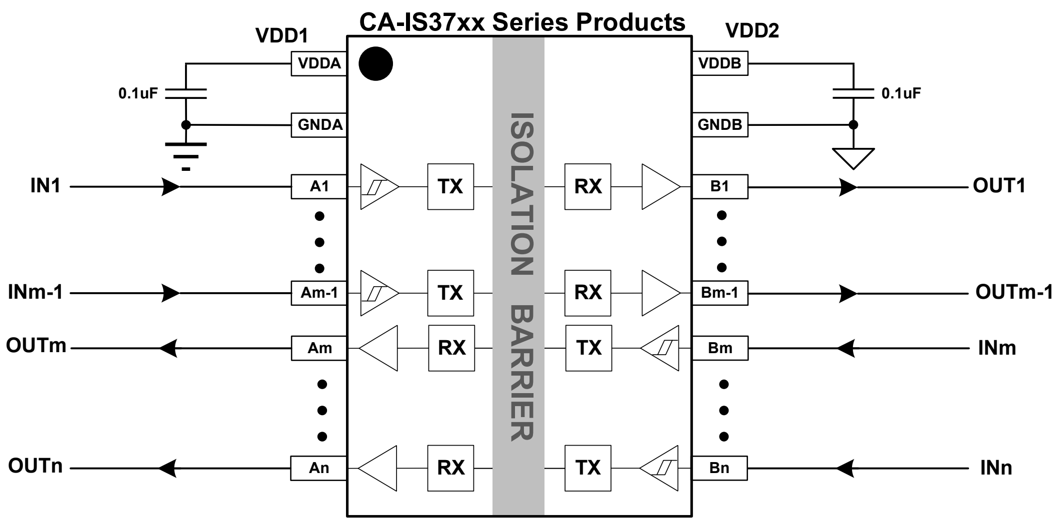
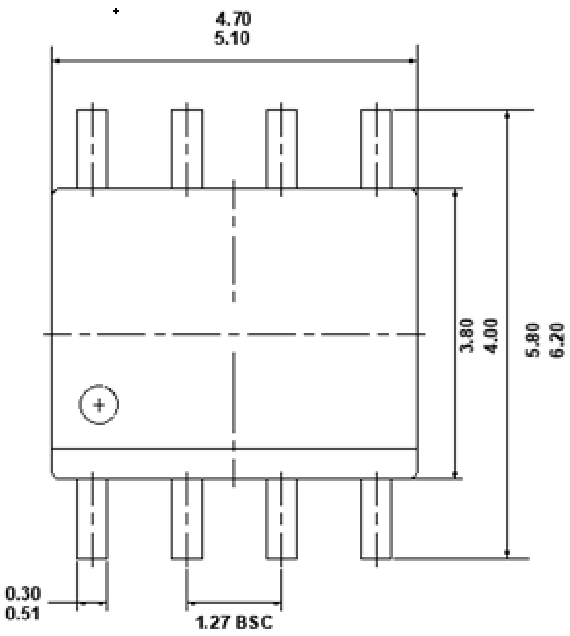


Figure 10-2. Typical Applications for the CA-IS37xx Series Digital Isolators

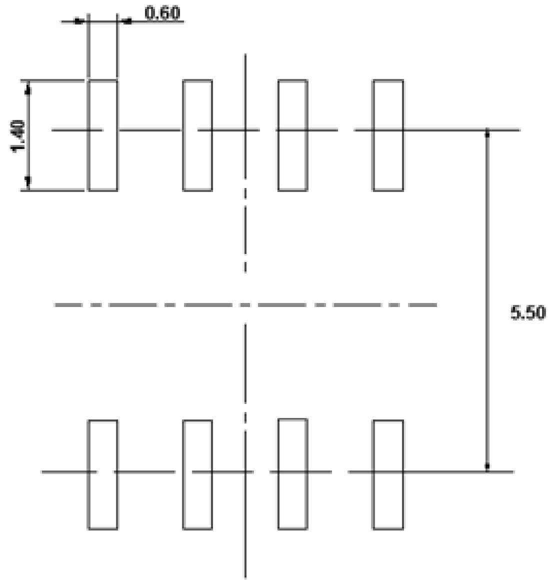
11. Package Information

8-Pin SOIC Package Outline

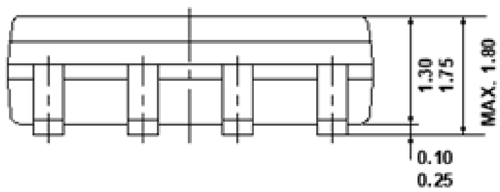
These figures show the package details and the recommended land pattern details for the CA-IS3720VLS digital isolator in 8-pin narrow-body SOIC package. The values for the dimensions are shown in millimeters.



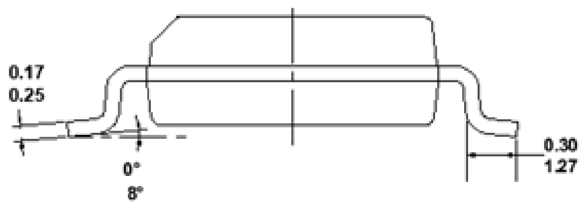
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

12. Soldering Temperature (reflow) Profile

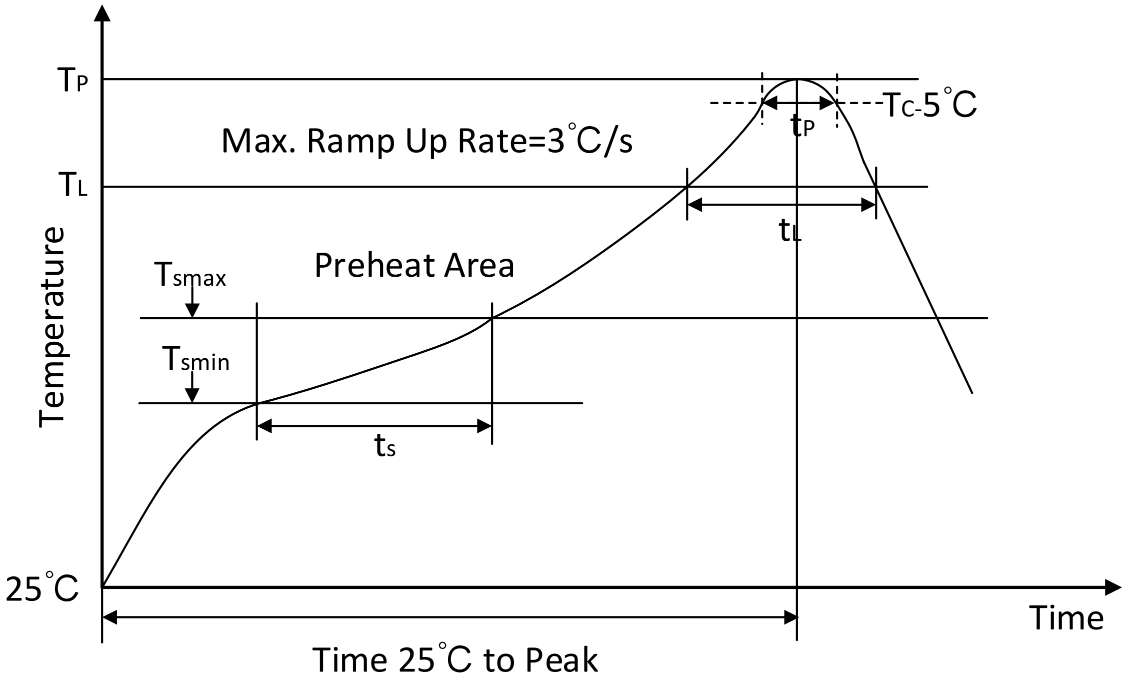


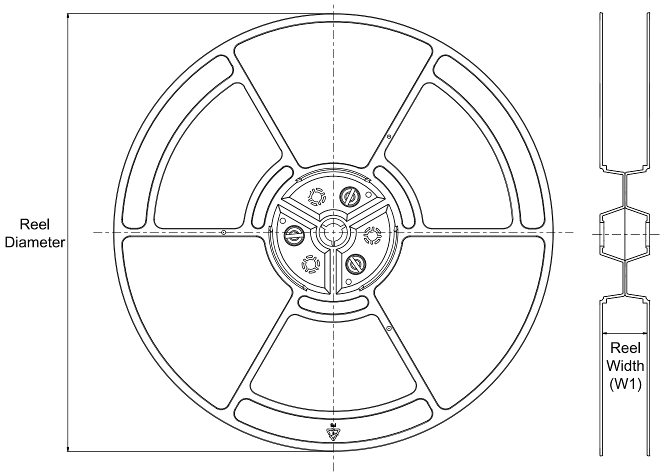
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

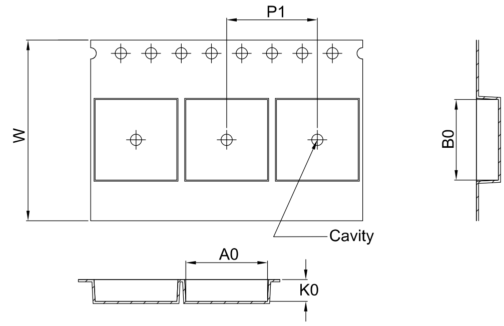
Profile Feature	Pb-Free Assembly
Average ramp rate (217 ℃ to Peak)	3℃/second max
Time of Preheat temp (from 150 ℃ to 200 ℃)	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃ of actual peak temp	30 second
Ramp down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

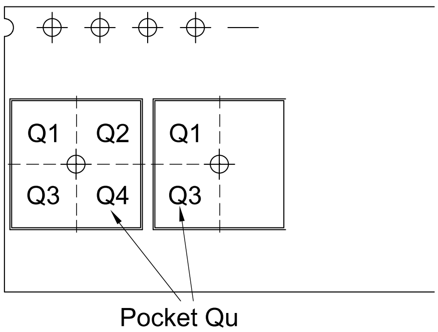


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3720VLS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1

14. Important statement

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