

NOT RECOMMENDED
FOR NEW DESIGNS
SEE CA741

May 1990

Operational Amplifiers

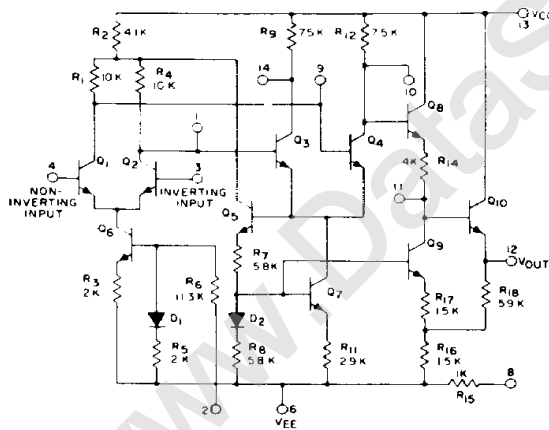
Features:

- These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance
- All types are electrically identical within their voltage groups
- For use in telemetry, data-processing, instrumentation, and communication equipment
- Built-in temperature stability from -55°C to $+125^{\circ}\text{C}$ for TO-5 style, and ceramic dual-in-line packages; 0°C to $+70^{\circ}\text{C}$ for plastic dual-in-line packages

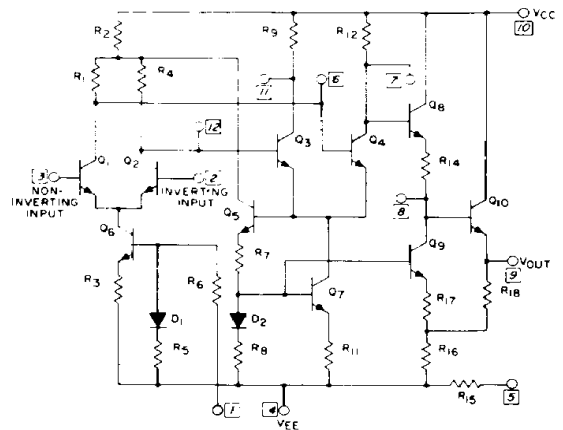
Applications:

- Narrow-band and band-pass amplifier
- Operational functions
- Feedback amplifier
- DC and video amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo driver
- Scaling adder
- Balanced modulator-driver

6-VOLT TYPES	12-VOLT TYPES	PACKAGE
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual-In-Line (TO-116)



CA3029A, CA3030A



CA3010A, CA3015A

Figure 1 - Schematic diagrams.

CA3010A, CA3015A, CA3029A, CA3030A

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3029A	Nega- tive	Posi- tive	Terminal	Voltage	
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3029A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10	6 13	-6 +6
				200 Ω Between Terminals 6 & 12 CA3029A, 4 & 9 (CA3010A)		
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE	Internally connected to Terminal No.4, CA3010A (Substrate) DO NOT GROUND					

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3030A	Nega- tive	Posi- tive	Terminal	Voltage	
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3030A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10	6 13	-12 +12
				400 Ω Between Terminals 6 & 12 CA3030A, 4 & 9 (CA3015A)		
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE	Internally connected to Terminal No.4, CA3015A (Substrate) DO NOT GROUND					

3

OPERATIONAL
AMPLIFIERS

	CA3010A CA3015A	CA3029A CA3030A		CA3015A	CA3010A
OPERATING TEMPERATURE RANGE . . .	-55°C to +125°C	-40°C to +80°C	MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-65°C to +150°C	MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

CA3010A, CA3015A, CA3029A, CA3030A

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 CA3029A, CA3030A, Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit	CA3010A CA3029A				CA3015A CA3030A			Units	Typical Charac- teristic Curves	
				Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.			Fig.
STATIC CHARACTERISTICS:													
Input Offset Voltage	V _{IO}	V _{CC} = +6V, V _{EE} = -6V = +12V = -12V	4	-	0.9	2	-	-	1	2	mV	2	
Input Offset Current	I _{IO}	= +6V = -6V = +12V = -12V	5	-	0.3	1.5	-	-	0.5	1.6	μA	2	
Input Bias Current	I _{IB}	= +6V = -6V = +12V = -12V	5	-	2.5	4	-	-	4.7	6	μA	3	
Input Offset Voltage Sensitivity:	Positive	ΔV _{IO} /ΔV _{CC}	4	-	0.10	1	-	-	0.096	0.5	mV/V	none	
	Negative	ΔV _{IO} /ΔV _{EE}		-	0.26	1	-	-	0.156	0.5			
Device Dissipation	P _D	= +6 V = -6 V = +12V = -12V	4	-	40	-	-	-	-	-	mW	none	
		[5] shorted to [9] 8 shorted to 12		V _{CC} = +6V V _{EE} = -6V V _{CC} = +12V, V _{EE} = -12V	-	102	-	-	-	500			-
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}													
Open-Loop Differential Voltage Gain	A _{OL}	V _{CC} = +6V, V _{EE} = -6V = +12V = -12V	8	57	60	-	-	-	66	70	-	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW _{OL}	= +6V = -6V = +12V = -12V	8	200	300	-	-	-	200	320	-	kHz	6 & 7
Slew Rate	SR	V _{CC} = +6V V _{EE} = -6V = +12V = -12V	none	-	3	-	-	-	-	7	-	V/μs	none
Common-Mode Rejection Ratio	CMR	V _{CC} = +6V, V _{EE} = -6V = +12V = -12V	11	70	94	-	-	-	80	103	-	dB	12
Maximum Output-Voltage Swing	V _O (P-P)	= +6V = -6V = +12V = -12V	8	4	6.75	-	-	-	12	14	-	V _{P-P}	9 & 10
Input Impedance	Z _{IN}	= +6V = -6V = +12V = -12V	14	15	20	-	-	-	7.5	10	-	kΩ	13
Output Impedance	Z _{OUT}	= +6V = -6V = +12V = -12V	15	-	160	-	-	-	-	85	-	Ω	16
Common-Mode Input-Voltage Range	V _{ICR}	= +6V = -6V = +12V = -12V	11	+0.5 to -4	-	-	-	-	+0.65 to -8	-	-	V	none
Noise Figure	NF	V _{CC} = +3V, V _{EE} = -3V	18	-	6.3	9	-	-	6.3	9	-	dB	17
		= +6V = -6V		-	8.3	12	-	-	8.3	12			
		= +9V = -9V		-	-	-	-	-	10	14			
		= +12V = -12V		-	-	-	-	-	11	16			

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max.

ALL TYPES
+265°C

CA3010A, CA3015A, CA3029A, CA3030A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A

Italic Numbers in Square Boxes are for CA3010A, CA3015A.

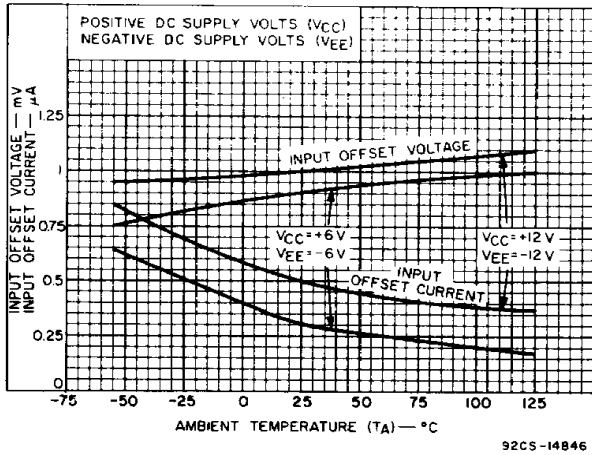


Fig. 2 — Input offset voltage and current

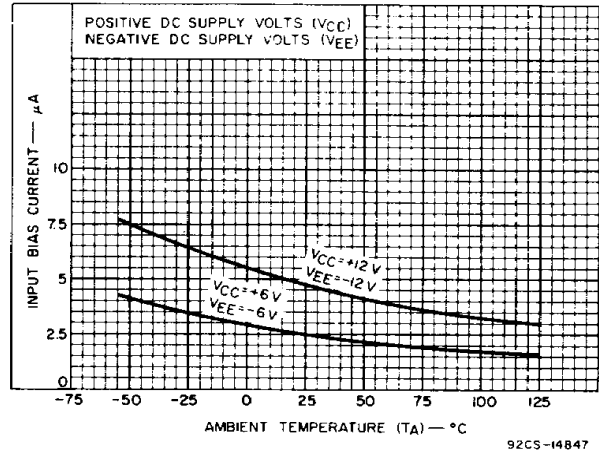


Fig. 3 — Input bias current

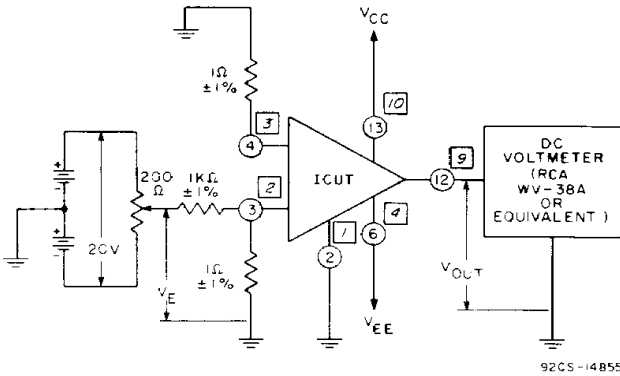


Fig. 4 — Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit.

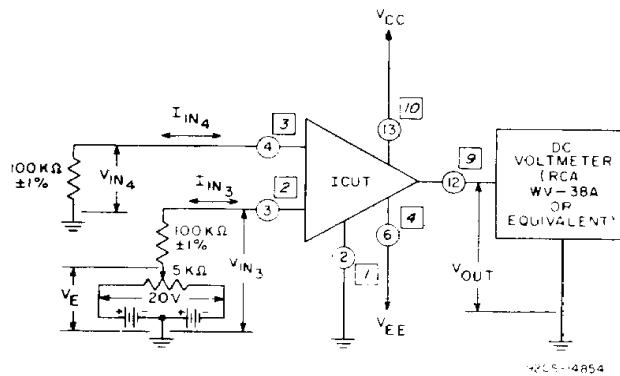


Fig. 5 — Input offset current and input bias current test circuit.

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the difference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}(\text{Step 2}) - V_{OUT}(\text{Step 3})}{2 \text{ volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO, V_{CC}} = \frac{V_{OUT} V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).

7. Device Dissipation

$$P_T = V_{CC} I_C + V_{EE} I_E$$

I_C = Direct Current into Terminal 13 or $\boxed{10}$

I_E = Direct Current out of Terminal 6 or $\boxed{4}$

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN4} .
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN4}}{100 \text{ k}\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E / 100 \text{ k}\Omega$$

CA3010A, CA3015A, CA3029A, CA3030A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A,
 Italic Numbers in Square Boxes are for CA3010A, CA3015A.

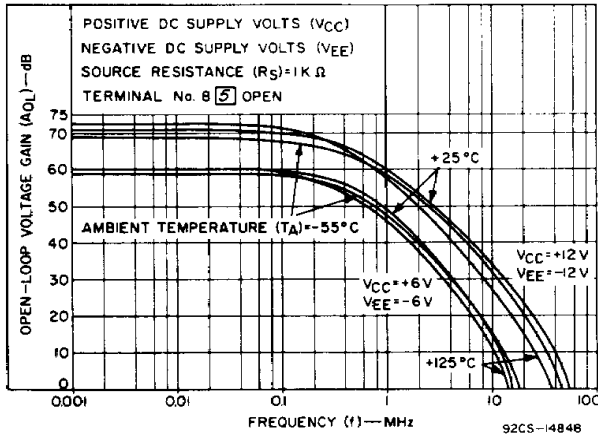


Fig. 6 — Open loop voltage gain vs. frequency for CA3015A, CA3016A

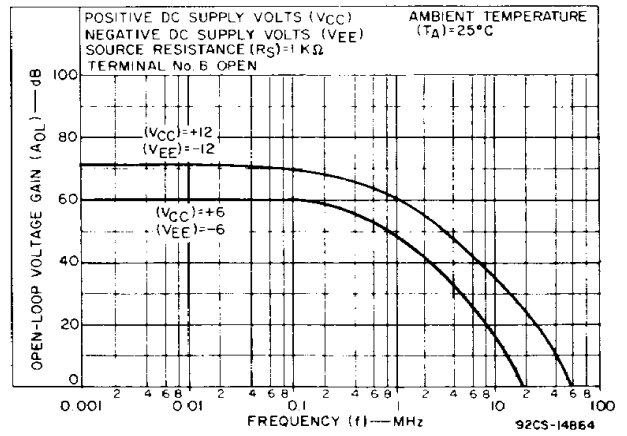


Fig. 7 — Open loop voltage gain vs. frequency for CA3029A and CA3030A.

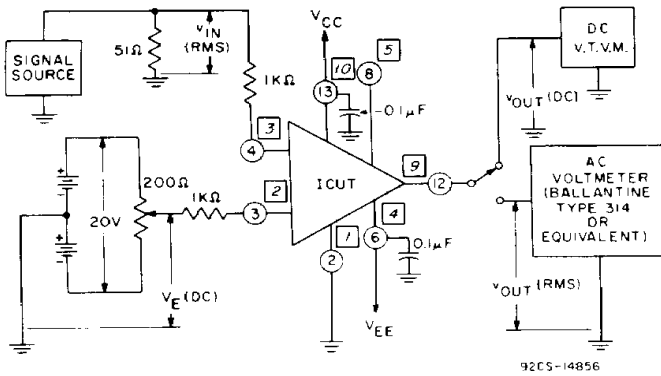


Fig. 8 — Open-loop differential voltage gain, maximum peak-to-peak output voltage, and open-loop bandwidth at -3 point test circuit.

Procedure:

1. Adjust V_E for $V_{OUT} = \pm 0.1$ V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at $f = 1$ kHz

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at $f = 1$ kHz
4. Measure Open-Loop Bandwidth at -3 dB Point
 Reference Level = A_{OL} at 1 kHz

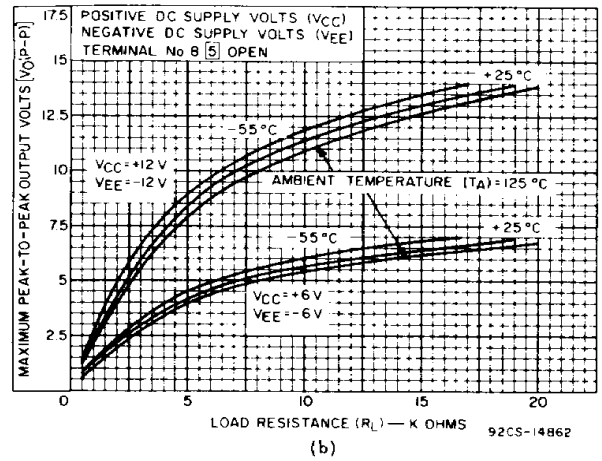
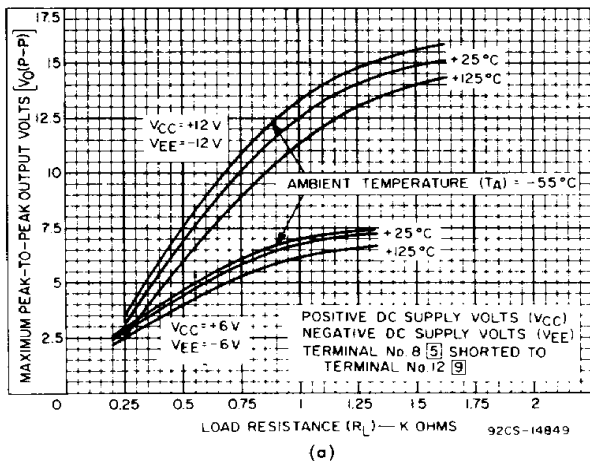


Fig. 9 — Maximum peak-to-peak output voltage vs. load resistance for CA3010A, CA3015A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A,
 Italic Numbers in Square Boxes are for CA3010A, CA3015A.

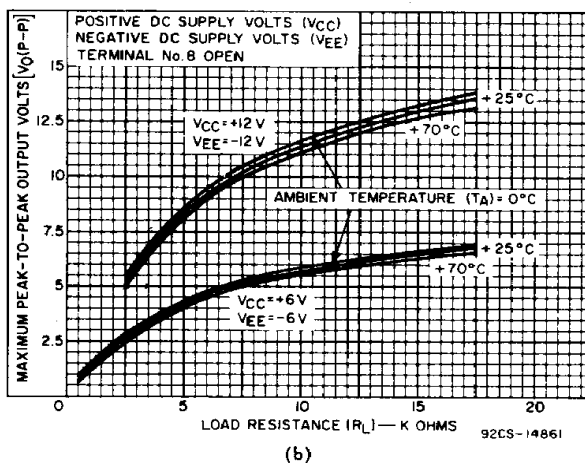
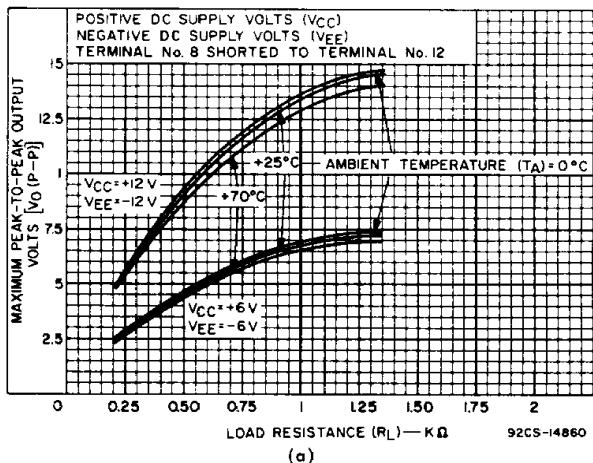
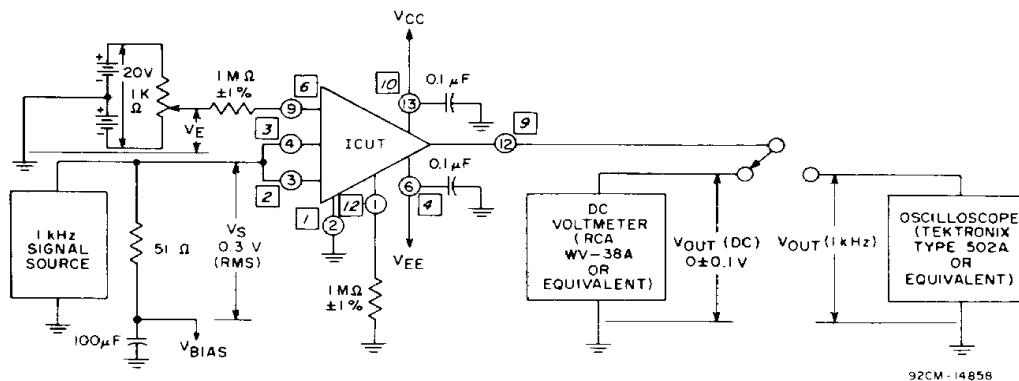


Fig. 10 — Maximum peak-to-peak output voltage vs. load resistance for CA3029A and CA3030A.



Procedures:

Common-Mode Rejection Ratio:

1. Set $V_{BIAS} = 0$. Adjust V_E for $V_{OUT(DC)} = 0 \pm 0.1$ V.
2. Apply 1-kHz sinusoidal input signal and adjust for $V_S = 0.3$ V (RMS).
3. Measure and record the RMS value of V_{OUT} . An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT} / V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S / V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB.}$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig. 11 — Common-mode rejection ratio and common-mode input-voltage-range test circuit.

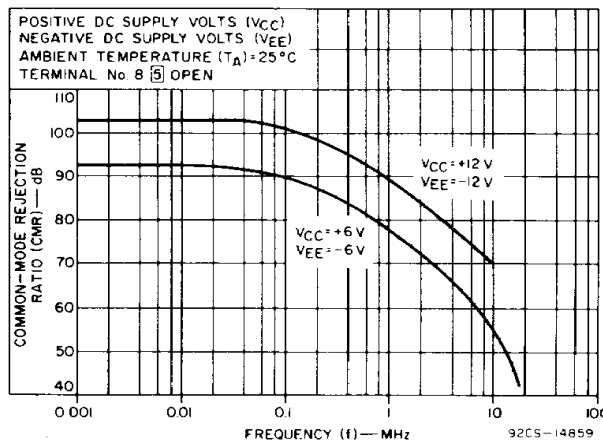


Fig. 12 — Common-mode rejection ratio vs. frequency.

CA3010A, CA3015A, CA3029A, CA3030A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A
 Italic Numbers in Square Boxes are for CA3010A, CA3015A.

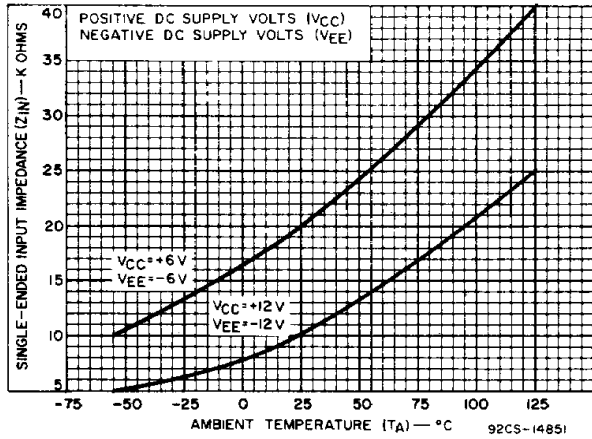


Fig. 13 — Single-ended input impedance vs. temperature.

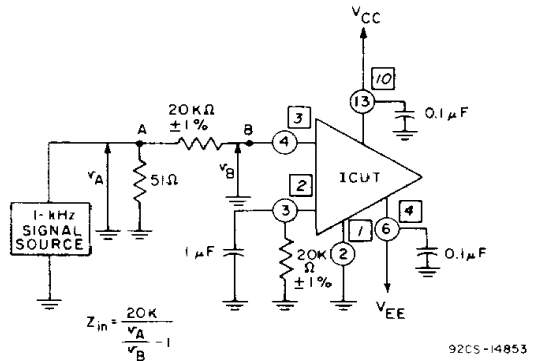
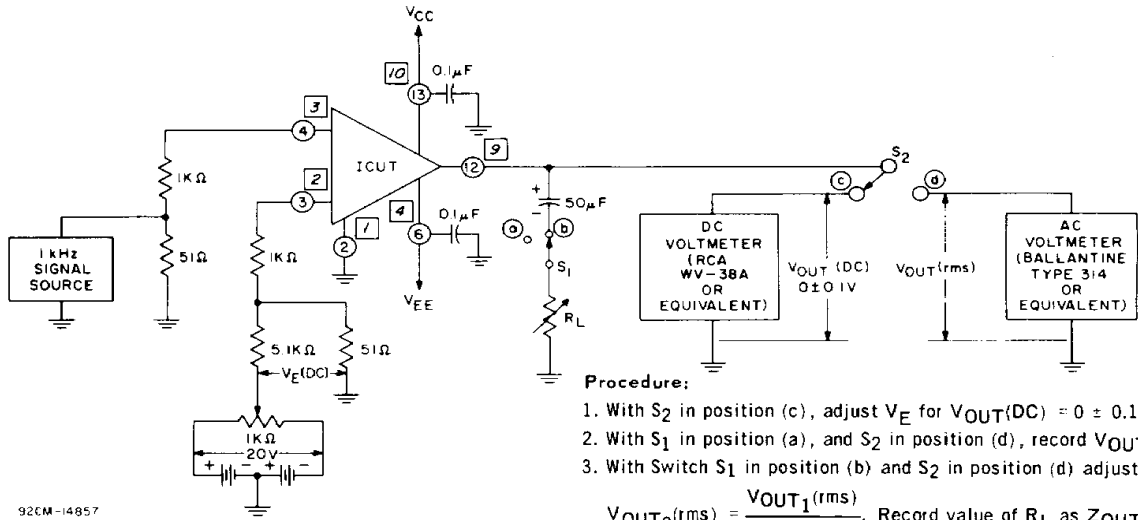


Fig. 14 — Single-ended input impedance test circuit.



Procedure:

1. With S₂ in position (c), adjust V_E for V_{OUT}(DC) = 0 ± 0.1 volt.
2. With S₁ in position (a), and S₂ in position (d), record V_{OUT1}(rms).
3. With Switch S₁ in position (b) and S₂ in position (d) adjust R_L until

$$V_{OUT2}(rms) = \frac{V_{OUT1}(rms)}{2}. \text{ Record value of } R_L \text{ as } Z_{OUT}.$$

Fig. 15 — Output impedance test circuit.

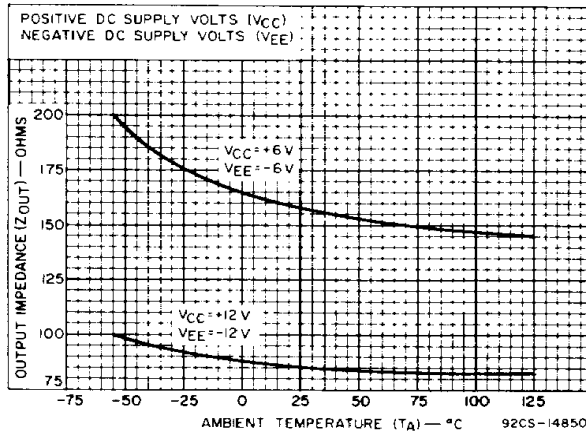


Fig. 16 — Output impedance vs. temperature.