CA3070, CA3071, CA3072

Television Chroma System

Features:

CA3070

- Voltage Controlled Oscillator
- Keyed APC & ACC Detectors
- DC Hue Control
- Shunt Regulator

CA3071

- ACC Controlled Chroma Amplifier
- DC Chroma Gain Control
- Color Killer
- Amplifier Short-Circuit Protection

CA3072

- Synchronous Detector with Color Difference Matrix
- Emitter-Follower Output Amplifiers with Short-Circuit Protection

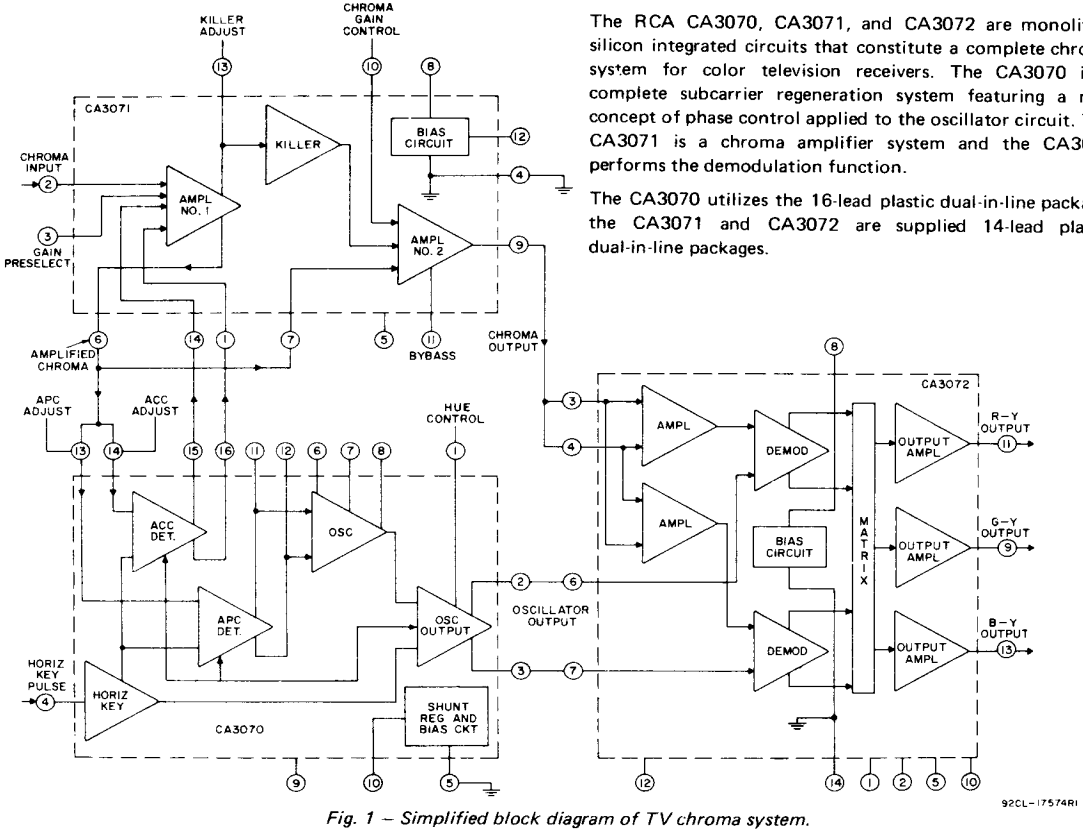


Fig. 1 – Simplified block diagram of TV chroma system.

The RCA CA3070, CA3071, and CA3072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The CA3071 is a chroma amplifier system and the CA3072 performs the demodulation function.

The CA3070 utilizes the 16-lead plastic dual-in-line package; the CA3071 and CA3072 are supplied 14-lead plastic dual-in-line packages.

File Number **468**

CA3070 Chroma Signal Processor

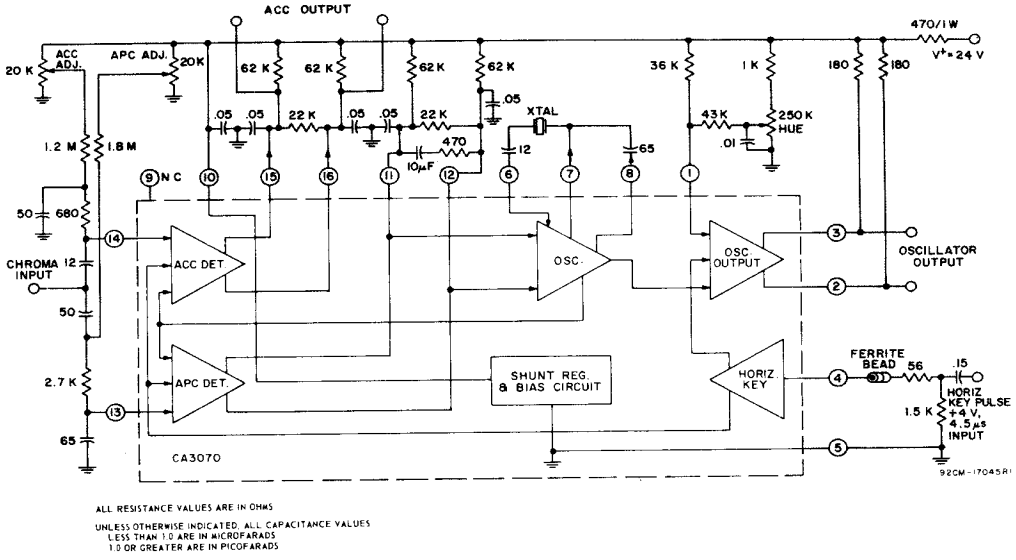


Fig. 2 – Functional diagram of RCA-CA3070.

The CA3070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 14 of the CA3071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3070 includes a shunt regulator to establish a 12-volt dc supply.

CA3070, CA3071, CA3072

MAXIMUM RATINGS, *Absolute Maximum-Values at $T_A = 25°C$*

DC Supply Voltage and Current . . . . . See Charts Below
Device Dissipation:
Up to $T_A = +70°C$ . . . . . 530 mW
Above $T_A = +70°C$ . . . Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:
Operating . . . . . −40 to +85 °C
Storage . . . . . −65 to +150 °C
Lead Temperature (During Soldering):
At distance 1/32 in. (3.17 mm) from seating plane for 10 s max. . . . . +265 °C

▲ With respect to terminal No.5 and with terminal No. 10 connected through 470Ω to +24 V.
N1 Regulated voltage at terminal No. 10.
N2 Controlled by max. input current.
N3 Limited by dissipation.

Maximum Voltage and Current Ratings at $T_A = +25°C$

Terminal No.	Voltage▲ Min. Volts	Voltage▲ Max. Volts
1	0	*
2	0	+16
3	0	+16
4	−5	N2
6	—	—
7	—	—
8	—	—
10	0	N3
11	0	N1
12	0	N1
13	0	N1
14	0	N1
15	0	+16
16	0	+16

Terminal No.	Current I_I mA	Current I_O mA
1	20	1
2	—	—
3	—	—
4	20	1
10	N3	1
11	—	—
12	—	—
13	20	1
14	20	1

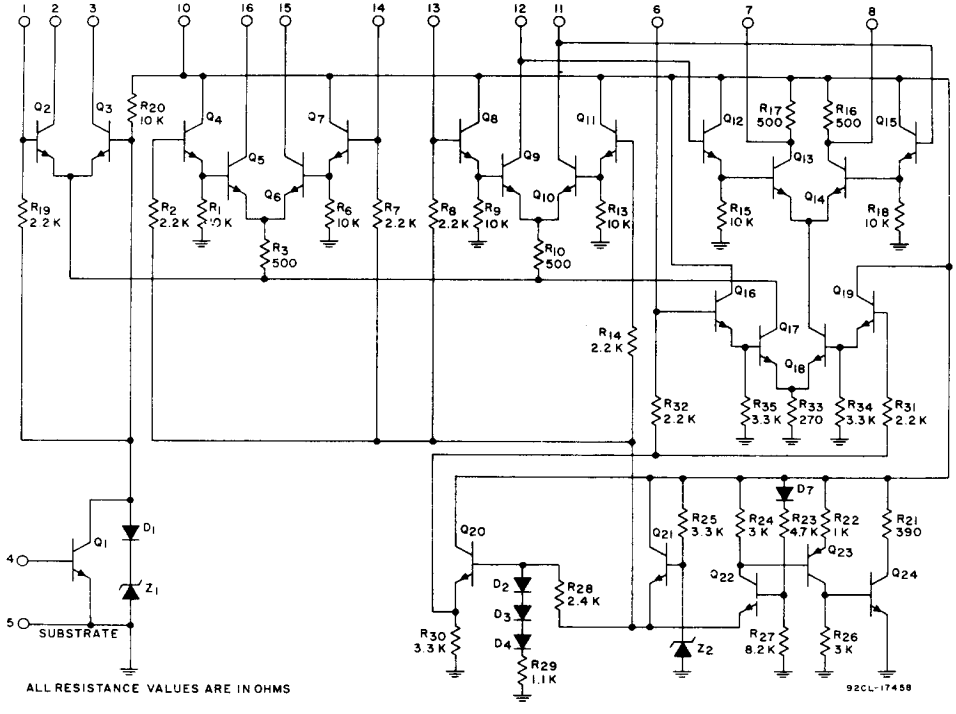


Fig. 3 — Schematic diagram CA3070.

CA3070, CA3071, CA3072

ELECTRICAL CHARACTERISTICS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3070 MIN.	LIMITS CA3070 TYP.	LIMITS CA3070 MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Voltage:							
Hue Control	V_1	Switch in position 2	6.9	7.7	8.6	V	4c
Oscillator Input	V_6		–	2.8	–	V	4a
APC Input	V_{13}		–	6.5	–	V	4a
Regulator	V_{10}	V^+ = 21 V	11	12.3	13.5	V	4a
Regulator Change	V_{10}	V^+ = 27 V	–0.2	–	+0.2	V	4a
Horizontal Key Input	V_4	I_4 = –10 μA	5	—	—	V	4a
Currents:							
Oscillator Output	I_2		–	5.8	–	mA	4c
APC Output	I_{11}, I_{12}		–	1.45	—	mA	4b
ACC Output	I_{15}, I_{16}		–	1.45	–	mA	4b
Dynamic Characteristics							
Oscillator Outputs:							
Terminal No. 2	V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}	5
Terminal No. 3	V_3	S_1 in position 2	0.75	1.0	–	V_{p-p}	5
ACC Detected Output	V_{16}–V_{15}	S_1 in position 1	115	150	–	mV	5
Oscillator Pull-In Range	–		–	±400	–	Hz	5

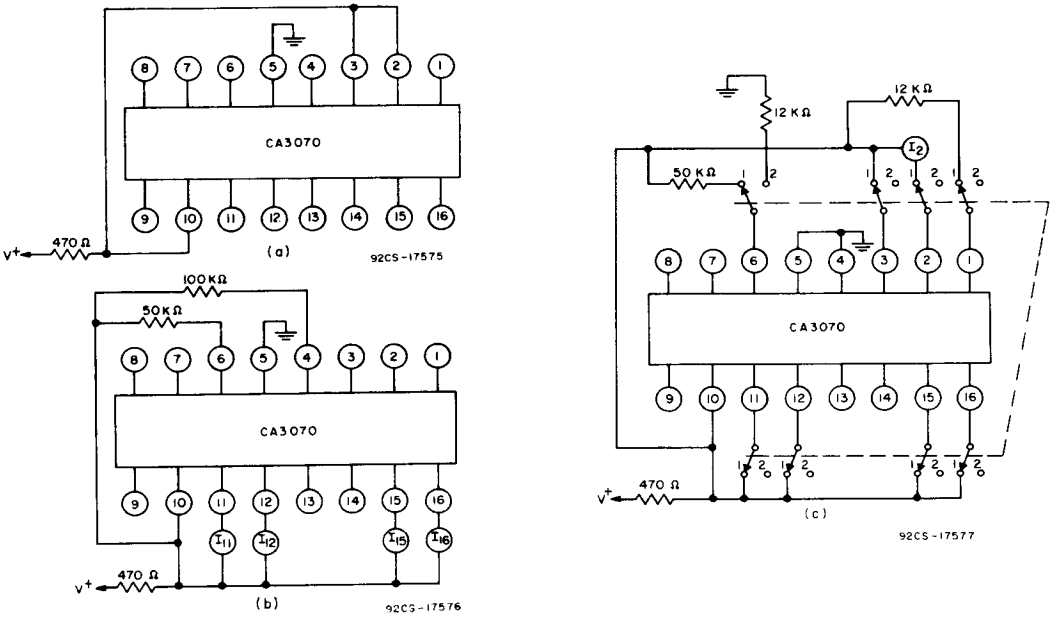
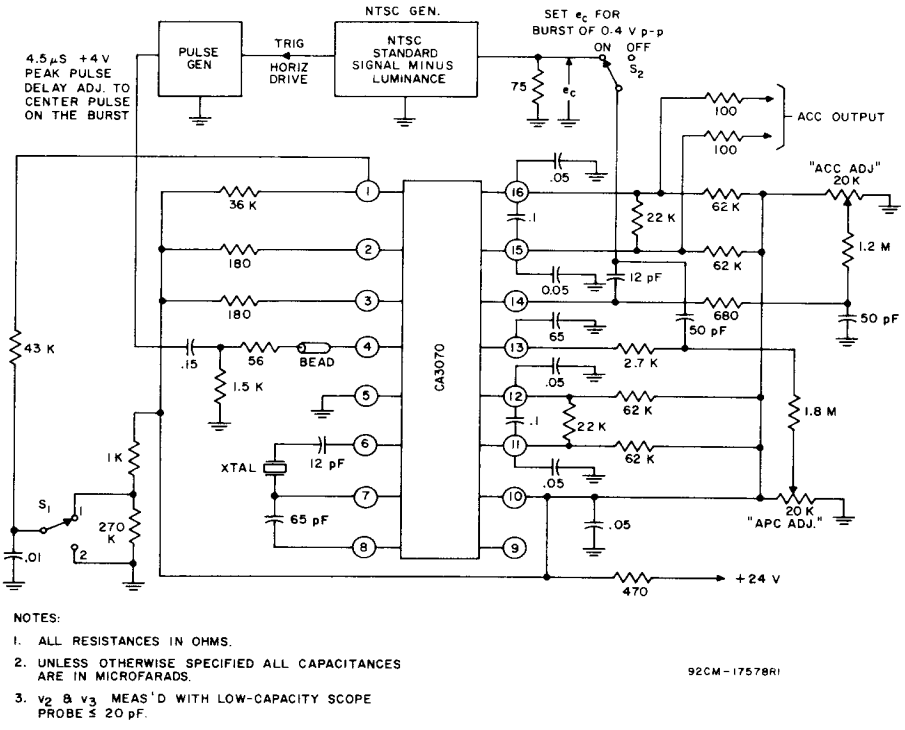


Fig. 4 – Static characteristics test circuits.

CA3070, CA3071, CA3072



NOTES:

1. ALL RESISTANCES IN OHMS.
2. UNLESS OTHERWISE SPECIFIED ALL CAPACITANCES ARE IN MICROFARADS.
3. v_2 & v_3 MEAS'D WITH LOW-CAPACITY SCOPE PROBE ≤ 20 pF.

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Fig. 5 – CA3070 Dynamic test circuit.

Dynamic Test Initial Adjustments

1. APC ADJUST: With S2 in "OFF" position adjust the "APC ADJ" potentiometer to set oscillator frequency at 3.579545 MHz ±25 Hz. With S1 in position 1 measure frequency at terminal No. 2 output, using crystal probe shown in Fig. 6.
2. ACC ADJUST: With S2 in "OFF" position adjust "ACC ADJ" potentiometer to give an ACC output reading of 0 ±2 mV.

Procedure to Pull-in Range Measurement

1. Set S1 in position 1 and connect the crystal probe to terminal No. 2.
2. Turn S2 to "OFF" and set "APC ADJ." arm to ground.
3. Turn S2 to "ON" and gradually adjust "APC ADJ" until oscillator "locks" as witnessed by a sharp increase in ACC output voltage between terminal Nos. 15 and 16.
4. Turn S2 to "OFF" and adjust capacitor Cp of crystal probe for maximum deflection on Ballantine Meter.
5. Switch Ballantine meter to "Amplifier" position and read oscillator frequency on counter.
6. Repeat steps 2 – 5 with "APC ADJ" arm set to terminal No. 10 instead of to ground.

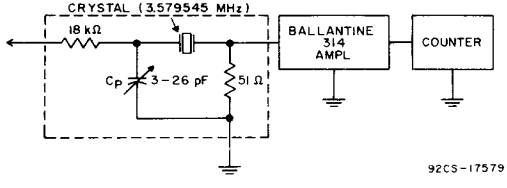

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Fig. 6 – Crystal probe for frequency measurements.

CA3071 Chroma Amplifier

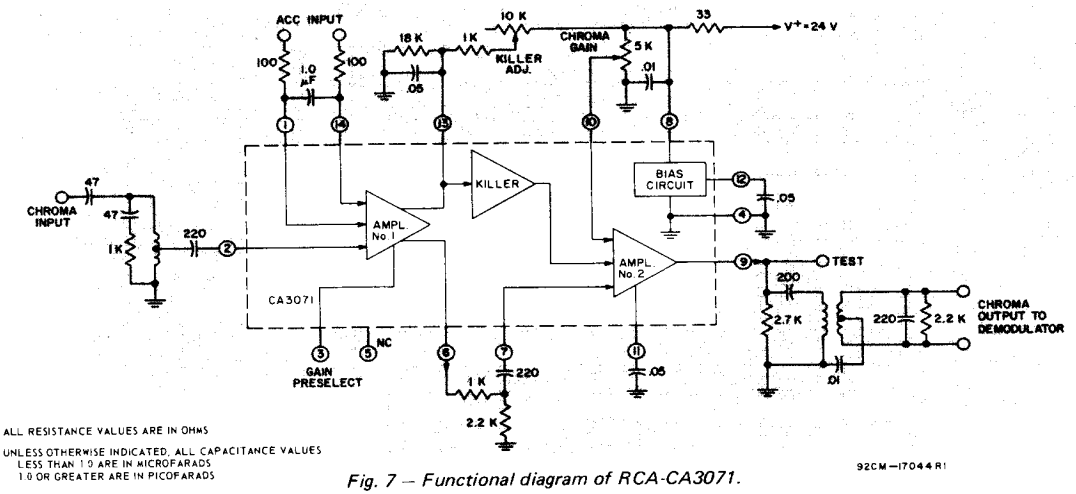

Fig. 7 – Functional diagram of RCA-CA3071.

The CA3071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the CA3070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit. The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment of dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at $T_A = 25°C$*

DC Supply Voltage (Terminal 8 to Terminal 4) ..... 30 VDC

Device Dissipation:
- Up to $T_A = +70°C$ ..... 530 mW
- Above $T_A = +70°C$ .... Derate Linearly at 6.7 mW/°C

Ambient Temperature Range:
- Operating ..... −40 to +85 °C
- Storage ..... −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/32 in (3.17 mm) from seating plane for 10 s max. ..... +265 °C

Maximum Voltage and Current Ratings @ $T_A = +25°C$

Terminal No.	Current I_I mA	Current I_O mA	Voltage* MIN VOLTS	Voltage* MAX VOLTS
1	5	1.0	−5	+15
2	5	1.0	−5	+5
3	10	10	0	+2
6	1.0	20	0	+24
7	5	1.0	−5	+5
9	1.0	20	0	+30
12	1.0	5	0	+24
14	5	1.0	0	+24
			0	+24
			0	+20
			0	+20
			−5	+15

* With reference to terminal No. 4 and with +24 V on terminal No. 8 except for the rating given for terminal No. 8.

CA3070, CA3071, CA3072

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

CHARACTERISTICS	SYMBOLS (Measure)	SPECIAL TEST CONDITIONS	LIMITS CA3071 MIN.	LIMITS CA3071 TYP.	LIMITS CA3071 MAX.	UNITS	CURVES & TEST CIRCUITS FIG.
Static Characteristics							
Voltages:							
Bias Reference Terminal	V_{12}	S_1 Open, S_2 Open	–	17.3	–	V	8
Ampl. No. 1 Chroma Input	V_2	S_1 Open, S_2 Open	–	1.75	–		
Ampl. No. 1 Chroma Output Balanced	V_6	S_1 Open, S_2 Open	–	20	–		
Unbalanced	V_6	S_1 Open, S_2 Closed	–	13.5	–		
Ampl. No. 2 Chroma Input	V_7	S_1 Open, S_2 Open	–	1.5	–		
Ampl. No. 2 Chroma Output	V_9	S_1 Closed, S_2 Open	–	20.6	–		
Supply Current	I_T	S_1 Open, S_2 Open	17	24.5	31	mA	
Dynamic Characteristics							
Amplifier No. 1 Voltage Gain	A_{V1}	E_g = 30 mV_{RMS} Measure v_6	14	–	–	dB	9
Amplifier No. 2 Voltage Gain	A_{V2}	V_g = 1.0 V (RMS) Measure v_7	–	14	–	dB	
Max. Chroma Output Voltage	v_9		–	2	–	V_{RMS}	13
10% Chroma Gain Control Reference Voltage	$V_8 - V_{10}$	E_g = 50 mV_{RMS}, adjust Chroma Gain Control to Change v_9 to 10% of Maximum Chroma Output	2.1	3.8	6.8	V	9
Output Voltage, Killer Off	v_9	S_1 in Position 2 E_g = 50 mV_{RMS}, adjust "Killer Adjust" for an abrupt decrease in V_9	–	–	12	mV RMS	
Output Voltage, Chroma Off	v_9	E_g = 50 mV_{RMS}, adjust Chroma control to min. Chroma Output	–	–	12	mV RMS	
Bandwidth: Amplifier No. 1	BW		–	12	–	MHz	11, 12
Amplifier No. 2			–	30	–		
Ampl. No. 1 Input Impedance	r_{i1}		–	2	–	kΩ	9
	c_{i1}		–	4	–	pF	
Ampl. No. 1 Output Impedance	r_{o1}		–	85	–	Ω	
Ampl. No. 2 Input Impedance	r_{i2}		–	2.1	–	kΩ	
	c_{i2}		–	3.5	–	pF	
Ampl. No. 2 Output Impedance	r_{o2}		–	85	–	Ω	

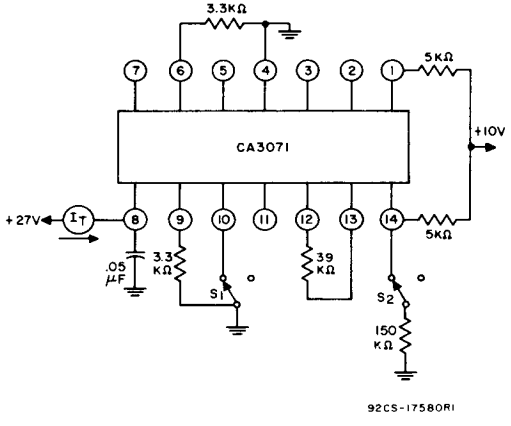

Fig. 8 – Static characteristics test circuit–CA3071.

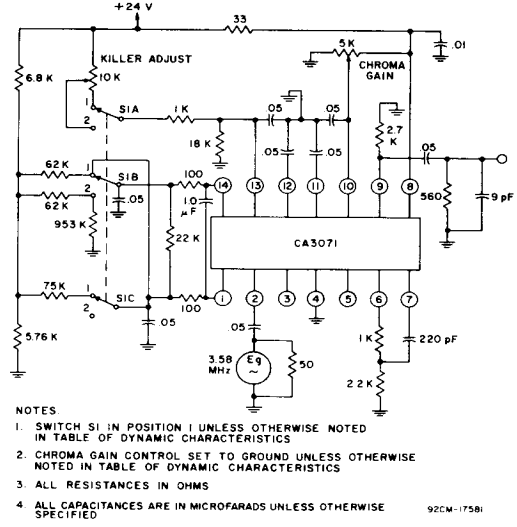

Fig. 9 – Dynamic characteristics circuit-CA3071.

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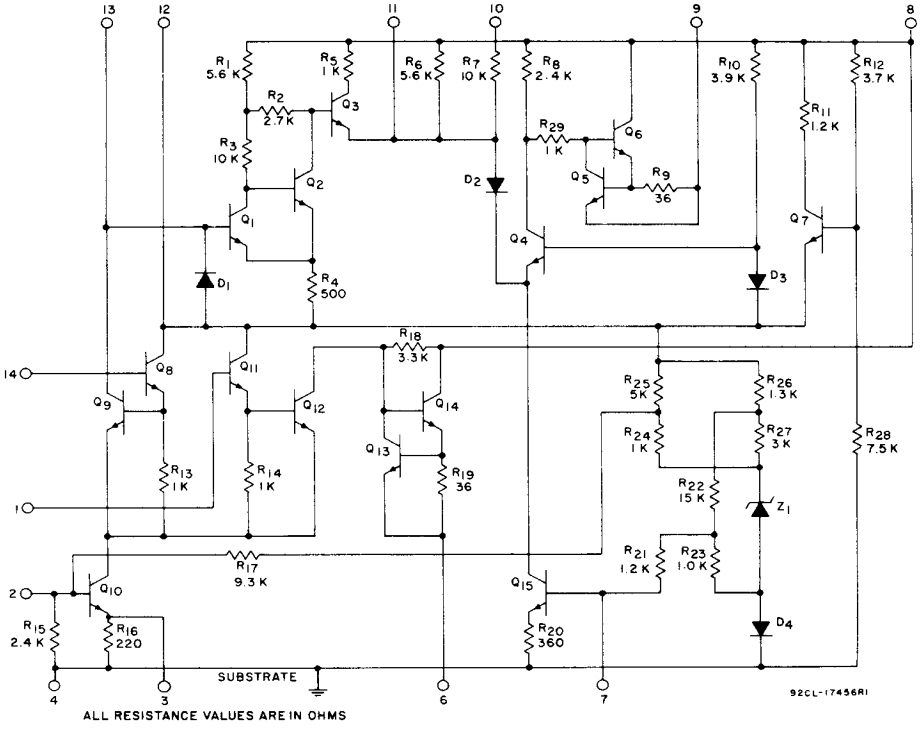

Fig. 10—Schematic diagram for CA3071.

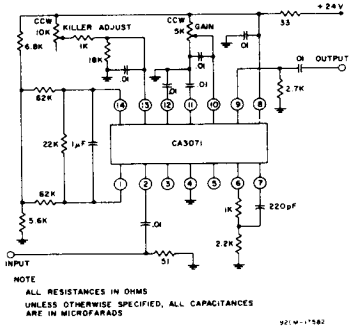

Fig. 11 – CA3071 Wideband amplifier circuit.

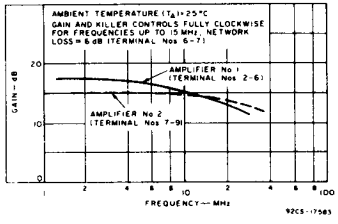

Fig. 12 – Frequency response for wideband amplifier CA3071.

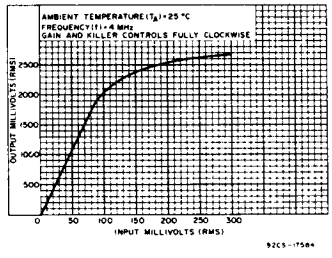

Fig. 13 – Typical CA3071 wideband amplifier linearity

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CA3072 Chroma Demodulator

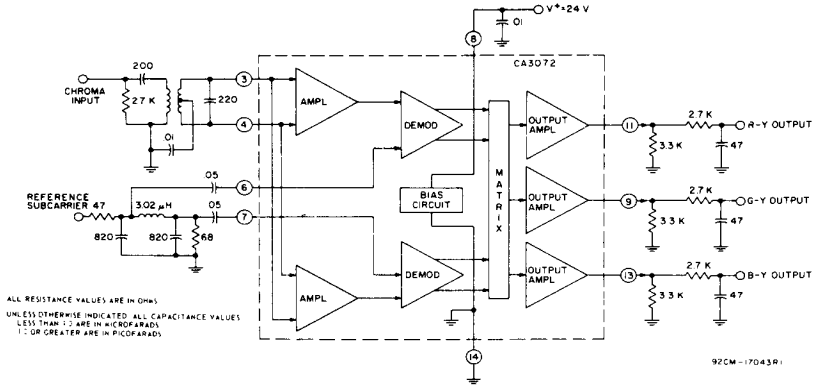


Fig. 14 – Functional diagram of RCA-CA3072.

The CA3072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the CA3072 are suitable for driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25° C*

DC Supply Voltage (Terminal 8 to Terminal 14)	27 V
Reference Input Voltage	5 V_{p-p}
Chroma Input Voltage	5 V_{p-p}
Device Dissipation:	
Up to T_A = +70°C	530 mW
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+265°C

Maximum Voltage and Current Ratings at T_A = +25°C

Terminal No.	Voltage* MIN VOLTS	Voltage* MAX VOLTS	Current Terminal No.	Current I_I mA	Current I_O mA
3	0	+5	3	–	–
4	0	+5	4	–	–
6	0	+12	6	–	–
7	0	+12	7	–	–
8	0	+27	8	–	–
9	0	+20	9	1.0	20
11	0	+20	11	1.0	20
13	0	+20	13	1.0	20

*With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

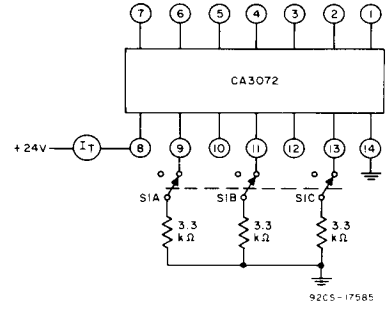


Fig. 15 – Static characteristics test circuit–CA3072.

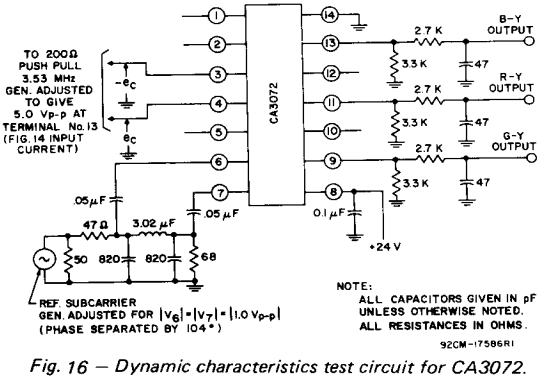


Fig. 16 – Dynamic characteristics test circuit for CA3072.

CA3070, CA3071, CA3072

ELECTRICAL CHARACTERISTICS, at T_A = 25° C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3072			UNITS	TEST CIRCUITS
			MIN.	TYP.	MAX.		FIG.
Static Characteristics							
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	26.5	mA	15
With No Output Loads		S_1 Open	–	9			
G-Y, R-Y, B-Y Outputs	V_9, V_{11}, V_{13}	S_1 Closed	13.2	14.7	15.8	V	
Chroma Inputs	V_3, V_4	S_1 Open	–	3.3	–		
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.2	–		
Dynamic Characteristics							
Demodulator Unbalance	v_9,v_{11},v_{13}	$V_3 = V_4 = 0$	–	–	0.8	V_{p-p}	16
Maximum Color Difference Output Voltage	v_{13}	$V_3 = V_4 = 0.6$ V_{p-p}	8.0	–	–	V_{p-p}	
	v_{11}		5.5	–	–		
	v_9		1.2	–	–		
Chroma Input Sensitivity	v_3	Adjust e_c for 5.0 v_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35	V_{p-p}	
Relative R-Y Output	v_{11}		3.5	–	4.2		
Relative G-Y Output	v_9		0.75	–	1.25		
V_{DC} Difference Between any two Output Terminals	$\lvert V_9 \rvert - \lvert V_{11} \rvert$ $\lvert V_9 \rvert - \lvert V_{13} \rvert$ $\lvert V_{11} \rvert - \lvert V_{13} \rvert$	$e_c = 0$	–	–	0.6	V	
Input Impedance Reference Subcarrier Inputs	r_i6, 7		–	1.7	–	kΩ	
	c_i6, 7		–	6	–	pF	
Input Impedance at Chroma Inputs	r_i3, 4		–	0.95	–	kΩ	
	c_i3, 4		–	6	–	pF	
Output Resistance	r_o9, r_o11, r_o13		–	180	–	Ω	

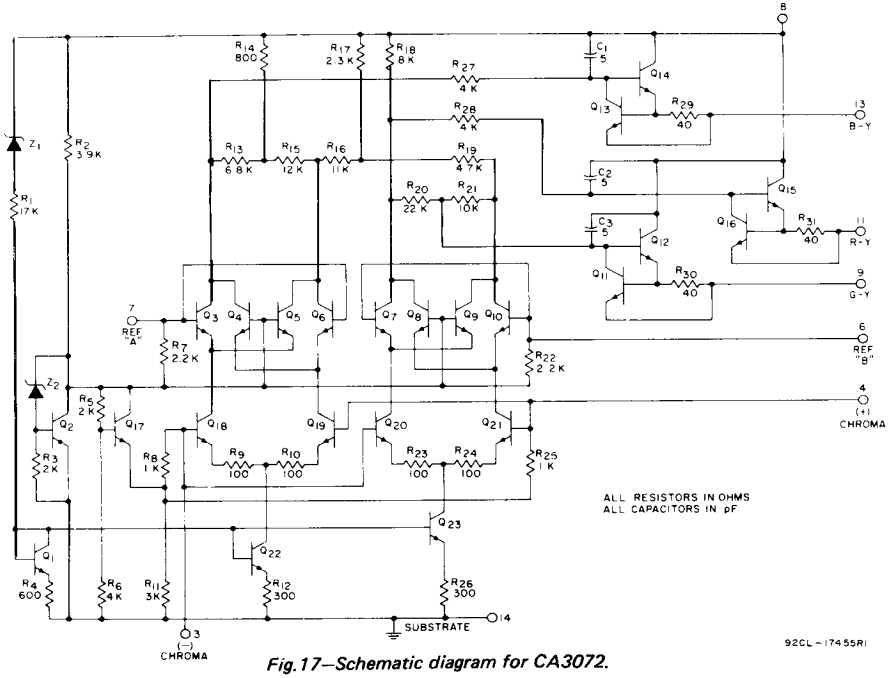


Fig.17—Schematic diagram for CA3072.

CA3070, CA3071, CA3072

Application Information

TYPICAL APPLICATION CIRCUIT FOR THE CHROMA SYSTEM

The circuit of Fig. 18 is a complete signal processing system for color TV. The RCA types CA3070, CA3071 and CA3072 monolithic integrated circuits are respectively used as the subcarrier regenerator, chroma amplifier, and chroma demodulator.

The input to the system is the chroma signal which may be taken from the first or second video stage and is coupled into the CA3071 chroma amplifier through a bandpass filter. The outputs from the system are the color difference signals which are intended to drive high level amplifiers. Luminance mixing may be external to the picture tube or, the difference signals may be amplified and applied to the picture tube grid or cathode, where they are internally mixed with the luminance signal.

Other input requirements to the system are the power supply voltage of +24 volts and the horizontal keying pulse. The power supply voltage should be maintained within ±3 volts of the recommended value of +24 volts. The total current for the system is approximately 70 milliamperes. The horizontal keying pulse input to the subcarrier regenerator is approximately +4 volts peak and centered on the burst as seen at terminal Nos. 13 and 14 of the CA3070. The pulse width should be maintained as close as possible to the recommended value of 4.5 microseconds.

CA3070 Circuit Operation

The CA3070 circuit as shown in Fig. 3, consists of an oscillator, automatic phase control (APC) detector, automatic chroma control (ACC) detector, gated oscillator output amplifier and a shunt regulator. The shunt regulator provides the necessary bias stability for the 3.579545 MHz oscillator, as well as the bias to all functions of the CA3070 circuit. The regulation voltage is nominally +12 volts as measured at terminal No. 10.

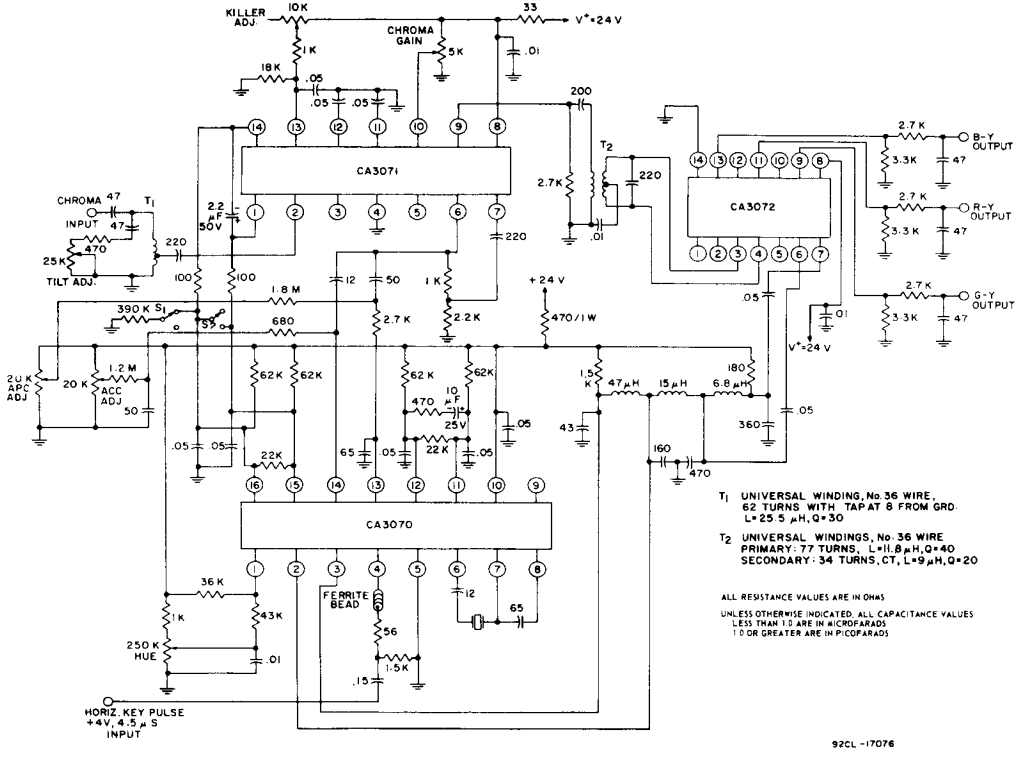


Fig. 18 – Typical chroma system for color-TV receivers utilizing RCA-CA3070, CA3071, and CA3072.

The APC and ACC detectors are synchronous detectors which are keyed by the horizontal input pulse. This form of detection eliminates the need for a burst separator as an individual amplifier stage. When a positive pulse is present at terminal No. 4, the oscillator output is cutoff and the oscillator drive signal is diverted to the APC and ACC detectors. Referring to Fig. 3, the APC detector (Q_9 & Q_{10}) and the ACC detector (Q_5 & Q_6) are emitter driven from the oscillator transistor (Q_{17}), when the oscillator output amplifier transistors (Q_2 & Q_3) are cutoff. The chroma signal is applied to terminal Nos. 13 and 14. There is oscillator current drive to the APC and ACC detectors during the keying interval; burst separation is effectively accomplished by the gating action of the detectors. A further advantage of the keying action is the high gain made possible as a result of the low average current flow of the APC and ACC detectors. High resistor values of 62 kilohms at the detector output terminals provide proper detector bias consistent with the duty factor of the keying pulse. For a wider keying pulse, it is necessary that smaller values of detector load resistors be used.

In the absence of the keying pulse (line period), the resistor, R_{20}, biases the oscillator's output amplifier transistors (Q_2 & Q_3) on by keeping their emitters at a higher potential than the base bias voltages of Q_5, Q_6, Q_9, and Q_{10}. The 3.58 MHz signal is now present at terminal Nos. 2 & 3. Photographs of oscilloscope traces for one line period at the terminal Nos. 1, 2, and 3 are shown in Fig. 19 The effect of the keying pulse is shown in Fig. 19a, and the cutoff of the oscillator output amplifier is shown in Fig. 19b and 19c.

The oscillator section of the CA3070 consists of the loop formed by Q_{18} and the emitter driven differential pair, Q_{13} & Q_{14}. The signal output from terminal Nos. 7 & 8 is coupled through the series tuned crystal circuit back through terminal No. 6 to Q_{16} & Q_{17}. The collector of Q_{17} drives the oscillator output amplifier and the APC & ACC detectors. Q_{17} is emitter coupled to transistor Q_{18}. The oscillator frequency and phase control is accomplished by the differential drive from the APC detector to transistors Q_{12} & Q_{15} which control the balance of Q_{13} & Q_{14}. The resulting phase of the feedback loop is determined by the relative amplitudes of the oscillator output signal at terminal Nos. 7 and 8. The 65 pF capacitor between terminal No. 7 and 8 provides the phase shifting component as the balance of Q_{13} and Q_{14} is varied. In this way the APC detector controls the crystal frequency at which the phase shift is cancelled in the feedback loop.

The controls for the CA3070 subcarrier regenerator circuit are the APC balance, the ACC balance, and the hue control. The hue control is a dc balance adjustment of the oscillator output amplifier transistors Q_2 & Q_3. A phase delay network between the output terminals Nos. 2 & 3 determines the range of the hue control, which for the value shown in Fig. 18, is approximately 90°.

The ACC adjustment sets the initial balance of the ACC drive to the input of the CA3071 in Fig. 18 (terminal Nos. 1 and 14 of the CA3071). The APC is a frequency adjustment of the oscillator through the balance control of the APC detector.

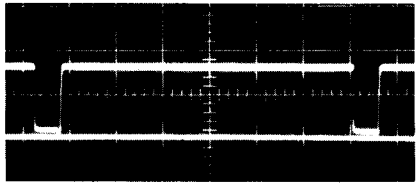


Fig. 19(a) - CA3070 terminal No. 1 7.5 V oscillator "gate off" pulse.

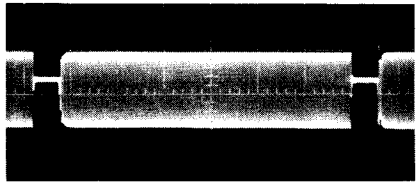


Fig. 19(b) - CA3070 terminal No. 2, 3.5 $V_{p\text{-}p}$ oscillator output; one horizontal line, (gated off during burst).

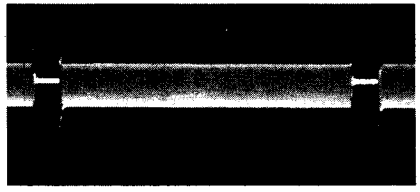


Fig. 19(c) - CA3070 terminal No. 3, 2.0 $V_{p\text{-}p}$ oscillator output; one horizontal line, (gated off during burst).

As a setup adjustment, for both the ACC and APC, switch S1 is opened and S2 is closed. The chroma input to the system is removed and the dc voltage at terminal No. 6 of the CA3071 is noted. The switch S2 is then opened and the ACC adjusted to set the voltage at terminal No. 6 to that previously noted. Alternatively, the differential dc voltage at terminal Nos. 15 & 16 of the CA3070 may be set to 0 mV (±2 mV) when S1 and S2 are open, and the CA3071 is removed from the circuit.

With the chroma signal still removed, the APC adjustment sets the frequency of the oscillator to 3.579545 MHz. Due to the gated off interval, a counter will not accurately record the frequency at the oscillator output amplifier terminals. Two simple and accurate methods are as follows: (1) a buffered crystal filter circuit, connected to the oscillator output amplifier terminals will continue to ring and fill the gated off window providing the proper interface to a counter; (2) the other method involves monitoring the demodulated output at the color difference output terminals

of the CA3072. A zero beat signal, at the color difference outputs may be seen on an oscilloscope.

When these adjustments are made, similar oscilloscope traces should be seen as shown in Fig. 20.

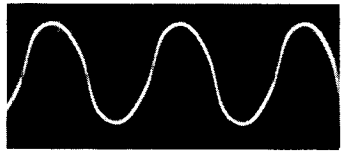


Fig. 20(a) - CA3070 terminal No. 6, oscillator waveform 1.1 V_{p-p} 3.58 MHz.

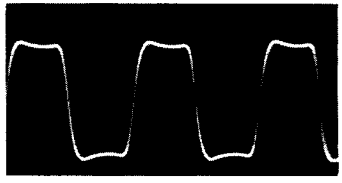


Fig. 20(b) - CA3070 terminal No. 7, oscillator waveform 1.4 V_{p-p} 3.58 MHz.

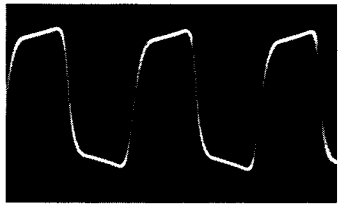


Fig. 20(c) - CA3070 terminal No. 8, oscillator waveform 1.6 V_{p-p} 3.58 MHz.

CA3071 CIRCUIT OPERATION

The CA3071 is the basic amplifier and control circuit of the chroma system. It contains the gain control functions of the ACC loop, the color killer, and the dc chroma gain control. The CA3071 is a wide band amplifier having two stages of voltage gain. Curves of frequency-response and linearity are shown in Figs. 12 & 13 for the wideband circuits shown in Fig. 11. This is the same basic amplifier as the one in the system shown in Fig. 18 except for the omission of the tuned circuits and the ACC loop connection. The amplifiers have bandwidths of greater than 10 MHz. and are usable well beyond 30 MHz. The signal swing of the wide band amplifier is in excess of 5 V_{p-p}, even with the typical load coupling as shown in Fig. 18. Fig. 21 (a, b and c) show the oscilloscope traces for an NTSC signal at the chroma input. The overall frequency-response curves are shown in Fig. 22.

CA3071 operation is as follows (Refer to Figs. 10 & 18). The input chroma signal is applied to terminal No. 2. This signal is amplified in a cascode differential circuit from Q_{10} to Q_{12}

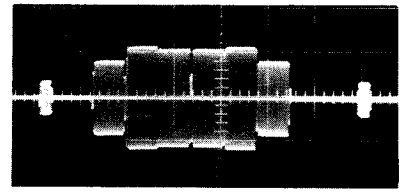


Fig. 21(a) - CA3071 chroma input 1.25 V_{p-p}; one horizontal line of NTSC input signal.

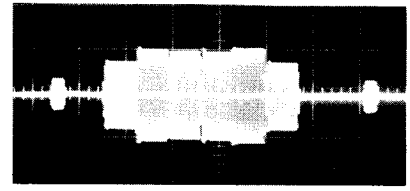


Fig. 21(b) - CA3071 terminal No. 6, amplifier No. 1 chroma output 2.3 V_{p-p}; one horizontal line for 1.25 V_{p-p} chroma input

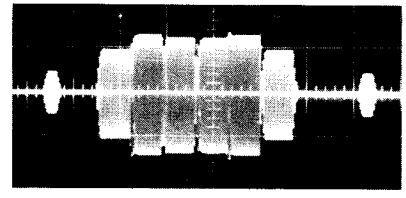


Fig. 21(c) - CA3071 terminal No. 9, amplifier No. 2 chroma output 5.5 V_{p-p}; one horizontal line for 1.25 V_{p-p} chroma input

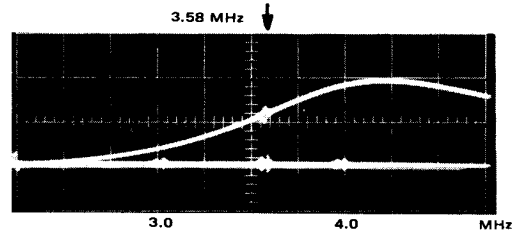


Fig. 22(a) - Frequency response sweep curve between terminal Nos. 2 & 6 for CA3071. f = 250 KHz/div.

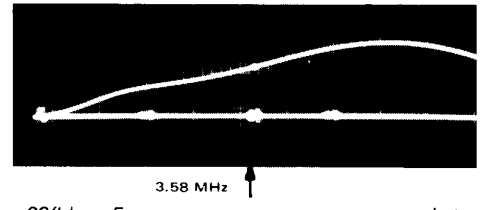


Fig. 22(b) - Frequency response sweep curve between terminal No. 2 of CA3071 and terminal No. 3 of CA3072. f = 250 KHz/div.

and the output is an emitter follower, Q_{14} (Terminal No. 6.) The signal is divided in the Q_9 & Q_{12} differential amplifier, depending on the applied ACC error signal amplitude at terminal Nos. 1 & 14. The ACC error signal is derived from terminal Nos. 15 & 16 of the CA3070 and after filtering, is applied to terminal Nos. 1 & 14 of the CA3071.

At low signal drive, the 390 kilohm resistor at switch S1 (normally closed) unbalances the differential amplifier for high signal gain through Q_{12}. As the burst level at the chroma input increases, the ACC drive changes differentially in a positive direction at terminal No. 14 and a negative direction at terminal No. 14 and a negative direction at terminal No. 1. At strong signal levels the gain is reduced by diverting the balance of ac current in the differential amplifier from Q_{12} to Q_9, which is shunted to ac ground at terminal Nos. 12 and 13. The ACC loop is completed through the chroma signal at terminal No. 6 of the CA3071 to terminal No. 14 (input) of the CA3070. A typical ACC characteristic is shown in Fig. 23.

The chroma signal is buffer connected from terminal No. 6 to terminal No. 7 of the CA3071 and is amplified in the 2nd

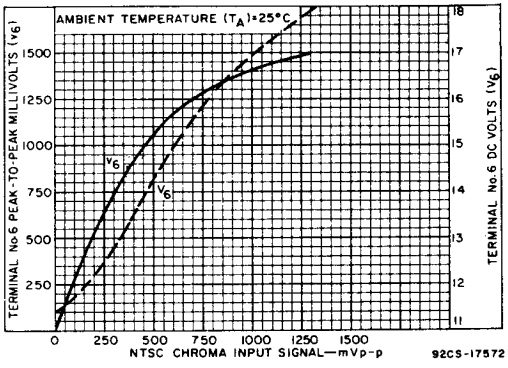


Fig. 23 - Typical ACC characteristics for chroma system of Fig. 18

stage of voltage gain. Both the color killer adjustment and the dc chroma gain control are applied to the 2nd stage to control the chroma output at terminal No. 9. The color killer section of the CA3071 is a Schmitt trigger & amplifier circuit consisting of transistors Q_1, Q_2 and Q_3. Under maximum chroma output conditions, the diode D_2 is reversed biased, and the signal path is through Q_{15}, Q_4 and Q_5 to terminal No. 9. When the color killer circuit is actuated, or the chroma gain control is adjusted to a higher positive voltage at terminal No. 10, the anode voltage of diode D_2 is increased to draw current from the signal path at the emitter of Q_4. This decreases the chroma gain as the potential at terminal No. 10 is increased. When the potential at terminal No. 10 is the same as terminal No. 8, the chroma output at terminal 9 is cutoff.

The color killer circuit provides an abrupt voltage swing at the anode of D_2 to cutoff the chroma output when the Schmitt trigger circuit is forward biased at terminal No. 13. In the circuit of Fig. 18, the color killer adjustment is a resistance divider circuit which establishes the threshold of burst level at which the killer operates the chroma amplifier.

CA3072 CIRCUIT OPERATION

The CA3072 is a chroma demodulator having full color difference signal demodulation capability. The chroma signal is applied to terminal Nos. 3 & 4 and the reference subcarrier signal is applied to terminals Nos. 6 & 7 of the CA3072. The output color difference signals are B-Y at terminal No. 13, R-Y at terminal No. 11, and G-Y at terminal No. 9. The typical level of differential chroma drive required at terminal Nos. 3 & 4 is 400 mV_{p-p}. The amplitude of chroma at terminal No. 6 & 7 is approximately 1.0 volt at 104° relative phase difference which results in a B-Y output amplitude of $5V_{p-p}$. The voltages of the R-Y & G-Y outputs are at 3.8 and 1.0 V_{p-p} respectively, when there is $5V_{p-p}$ output at B-Y. These comparative signals are based upon a complete phase rotation of the chroma relative to the subcarrier signal reference. The relative demodulation phase and amplitude ratios of the Fig. 18 circuit are shown in the oscilloscope trace photographs of Fig. 24. Using the hue control setting for B-Y phase at the B-Y output, the G-Y color-difference signal is approximately −104° and the R-Y color-difference signal is approximately +106°. Since the amplitude ratios are a function of the applied signal phase relationship, the NTSC color difference output signals are shown here primarily for phase reference conditions.

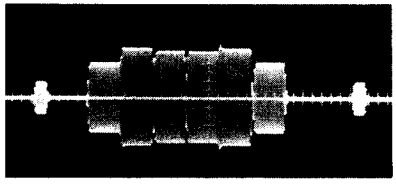


Fig. 24(a) - CA3072 - terminal No. 3 or 4, chroma input signal, 220 mV_{p-p}, one horizontal line

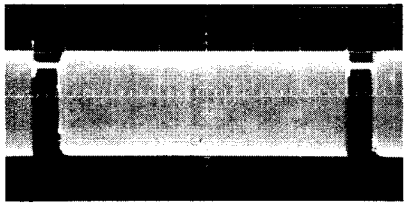


Fig. 24(b) - CA3072 - terminal No. 6 or 7, reference subcarrier 1.2 V_{p-p}, one horizontal line

CA3070, CA3071, CA3072

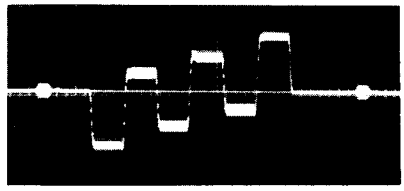


Fig. 24(c) - CA3072 terminal No. 13, 4.8 v_{p-p} B-Y output, one horizontal line

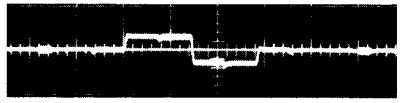


Fig. 24(d) - CA3072 - terminal No. 9, 1.2 v_{p-p} G-Y output, one horizontal line

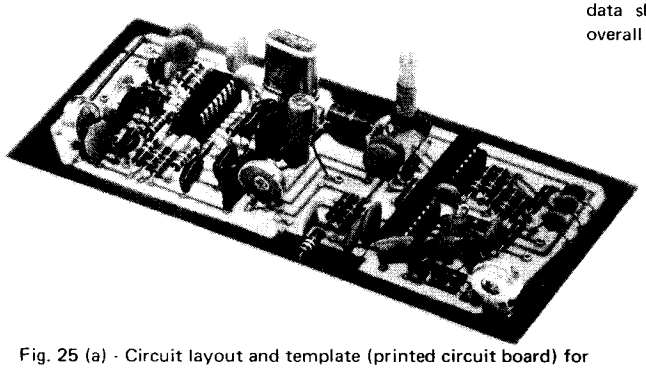


Fig. 25 (a) - Circuit layout and template (printed circuit board) for TV chroma system CA3070, CA3071, and CA3072.

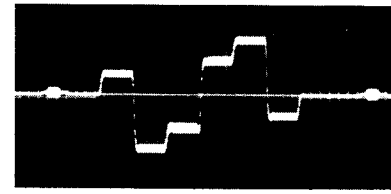


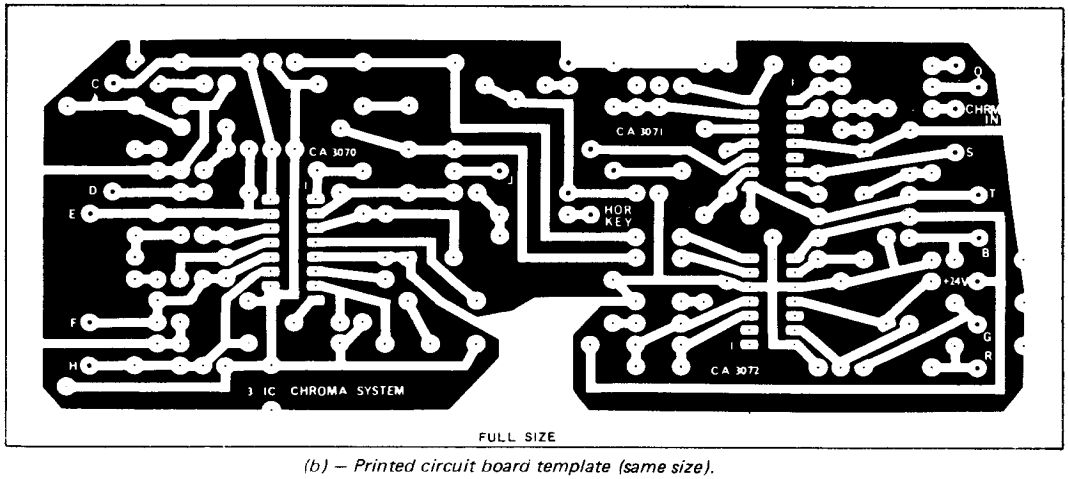
Fig. 24(e) - CA3072 - terminal No. 11, 5.2 v_{p-p} R-Y output, one horizontal line

CHROMA SYSTEM CONSTRUCTION

Fig. 25 shows the complete CA3070, CA3071 and CA3072 chroma system in the Fig. 18 circuit. Table I lists the dc terminal voltages for the system. The chroma gain and hue controls, as well as the switches S1 and S2 are removed. The template circuit board layout is also shown for duplication purposes. It should be noted that a few component values are modified in Fig. 18 from the dynamic circuit values of the data sheet. These are necessary for system matching and overall filter requirements.

TABLE 1 TYPICAL CHROMA SYSTEM TERMINAL DC VOLTAGES (NO SIGNAL INPUT)

TERMINAL No.	DC VOLTS		
	CA3070	CA3071	CA3072
1	7.6	7.3	–
2	11.5	1.7	–
3	11.5	–	3.3
4	−1.7	0	3.3
5	0	–	–
6	2.8	11.4	5.9
7	11.2	1.4	5.9
8	11.2	23.0	24.0
9	–	VARIABLE	14.7
10	12.0	VARIABLE	–
11	7.8	VARIABLE	14.7
12	7.8	15.0	–
13	6.7	VARIABLE	14.7
14	6.7	7.1	0
15	7.3	–	–
16	7.1	–	–



(b) — Printed circuit board template (same size).