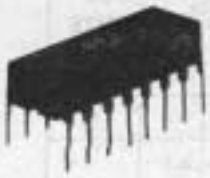

16-Lead Dual-in-Line Plastic Package H-1622

TV Signal Processors ("Jungle" Circuits)

For Color and Monochrome Receivers

FEATURES:

- *Internal impulse noise processing*
- *Sync separator — low impedance, dual polarity*
- *Strobed AGC system* ■ *IF AGC output*
- *Delayed outputs for forward or reverse AGC tuners*
- *Automatic noise threshold and AGC detector level control*
- *High-impedance video input*
- *Low-impedance video output*
- *Choice of external time constants for sync separator*
- *Negative power supply not required*
- *RF AGC delay externally controlled*

The RCA-CA3120E and CA3142E are monolithic silicon integrated circuit TV signal processors for use in color or monochrome receivers. These circuits provide low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit designs of the CA3120E and CA3142E feature impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, they incorporate standard AGC strobing techniques. The AGC noise lockout circuit is deleted in the CA3142E.

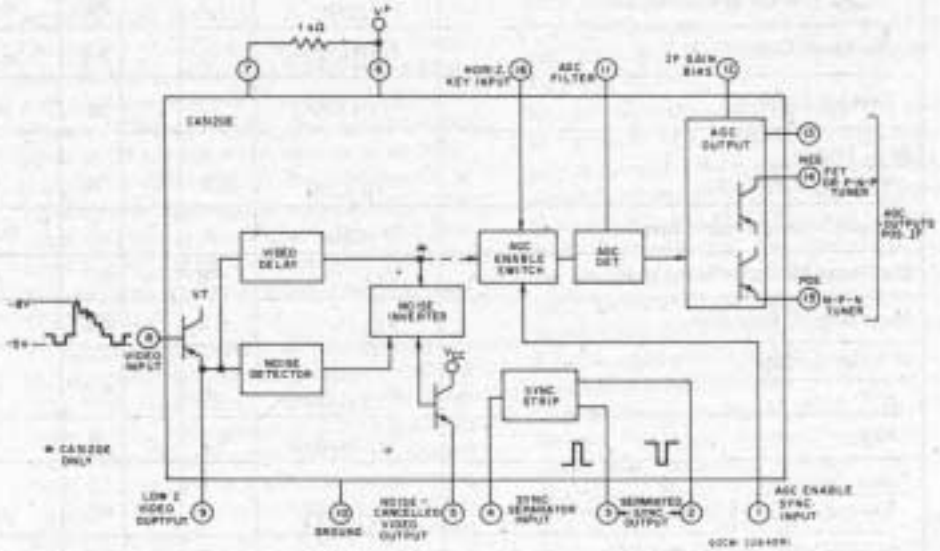

Fig.1 – Simplified block diagram of the CA3120E and CA3142E.

CA3120E, CA3142E

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Supply Voltage (V^+) = 24 V and Referenced to Test Circuits and Test Conditions (Figs. 6, 7, and 8).

CHARACTERISTICS	TERMINAL MEASURED AND SYMBOL	CA3120E CA3142E LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current (Pulse Test)	I_{T24}	20	–	40	mA
AGC Threshold (Sync Tip Level at Video Input)	V_{TH}	4.5	–	5.5	V
Video Input Amplitude (White Positive)	V_8	–	3	–	Vp-p
Video Output Amplitude (Low Impedance)	V_9	–	3	–	Vp-p
Noise Cancelled Video Output at V_{TH} (Black Positive, Gain ≅ 2)	V_5	3.6	–	9.2	V
AGC to Noise Separation	$V_{TH\ (SEP)}$	1.1	–	2.2	V
Sync Input Current for Full Amplitude Outputs	$I_{4\ (ON)}$	–	–	100	µA
Maximum Leakage Current at Terminal 4	$I_{4\ (OFF)}$	–	–	±6	µA
Sync Outputs:					
Negative Sync Low	$V_{2(L)}$	0	–	2.6	V
Negative Sync High	$V_{2(H)}$	23.8	–	24	V
Positive Sync Low	$V_{3(L)}$	0	–	0.2	V
Positive Sync High	$V_{3(H)}$	20.1	–	24	V
AGC Filter:					
Charge Current (Pulse Test)	$I_{11(CH)}$	12	–	38	mA
Discharge Current	$I_{11(DISCH)}$	1.1	–	2.6	mA
Leakage Current	$I_{11(LEAK)}$	–	–	±6	µA
AGC Enable:					
Horizontal Keying	$V_{16\ (ON)}$	3	–	6	V
Negative Sync Input Current	$I_{1\ (ON)}$	–	1	–	mA
Maximum IF Gain-Clamp Voltage	V_{11}	4.8	–	5.7	V
Maximum IF Gain Bias	V_{12}	4.2	–	5.2	V
IF AGC Voltage:					
Low	$V_{13\ (LOW)}$	0	–	3.3	V
High	$V_{13(HIGH)}$	5.7	–	6	V
Tuner Currents:					
Reverse AGC (FET) OFF Current	$I_{14\ (OFF)}$	–	–	±6	µA
Reverse AGC (FET) ON Current	$I_{14\ (ON)}$	1.8	–	5.5	mA
Forward AGC (n-p-n) OFF Current	$I_{15\ (OFF)}$	–	–	±6	µA
Reverse AGC (n-p-n) ON Current	$I_{15\ (ON)}$	4.5	–	15	mA
Internal Noise-Lockout Time (CA3120E only)	T	1	–	63	µs

CA3120E, CA3142E

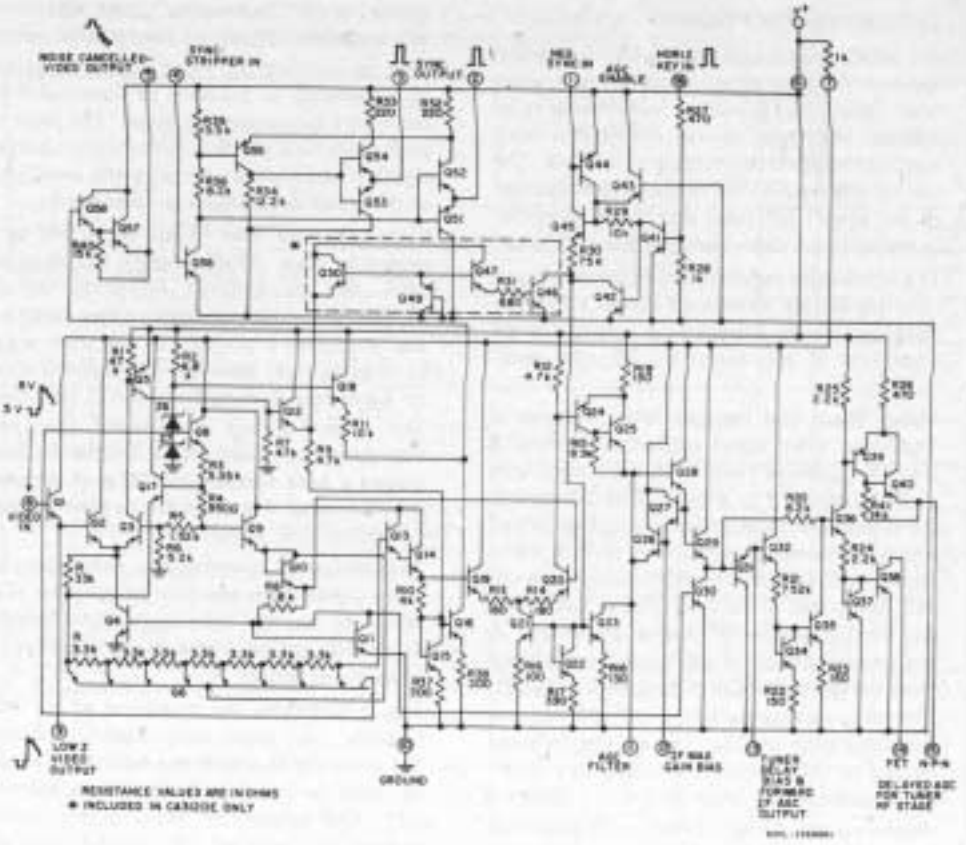

Fig.2 – Schematic diagram of the CA3120E and CA3142E.

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

DC SUPPLY VOLTAGE	30 V
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$ . . . . Derate linearly at 7.9	mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	–40 to +85 °C
Storage	–65 to +150 °C
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265 °C