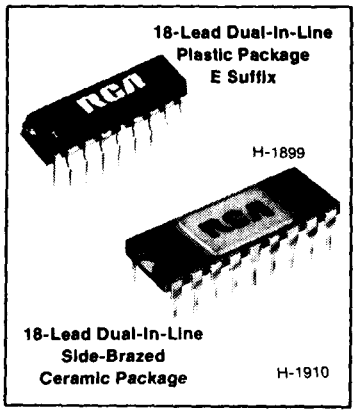
CA3300 Types

CMOS Video Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:

- *CMOS low power with speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *6-bit latched 3-state output with overflow bit*
- *±½ LSB accuracy*
- *Single supply voltage (3 to 10 V)*
- *2 units in series allow 7-bit output*
- *2 units in parallel allow 30-MHz sampling rate*
- *Internal V_{REF} with ext V_{REF} option*
- *Available with EVP processing for improved reliability*



The RCA-CA3300 types are CMOS 50-mW parallel (FLASH) analog-to-digital converters designed for applications demanding both low-power consumption and high-speed digitization.

The CA3300 types operate over a wide full-scale input-voltage range of 2.4 volts up to the dc supply voltage with maximum power consumption as low as 50 to 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 11 MHz, the power consumption of the CA3300 is less than 50 mW. When operated from an 8-volt supply at a frequency of 15 MHz, the power consumption is less than 150 mW.

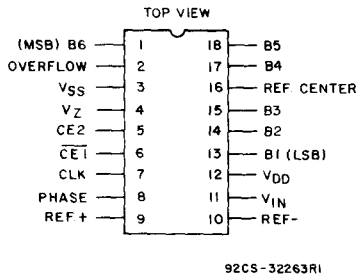
The intrinsic high conversion rate makes the CA3300 types ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3300's in series to increase the resolution of the conversion system. A series connection of two CA3300's may be used to produce a 7-bit high-speed converter. Operation of two CA3300's in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3300's in parallel may be combined with a high-speed 6-bit D/A converter, a binary adder, control logic, and an op amp to form a very-high-speed A/D converter.

Sixty-four paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3300. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

The CA3300 types are available as follows: Types CA3300D and CA3300DX in an 18-lead dual-in-line ceramic package (D suffix), types CA3300E and CA3300CE in an 18-lead dual-in-line plastic package (E suffix), or in chip form (H suffix). The CA3300DX offers the additional advantage of improved reliability as a result of EVP (Extra Value Program) processing. For further information on EVP, see RCA publication EVP-300B or contact your RCA representative.

Applications:

- *The CA3300 types are especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADC's*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*



TERMINAL ASSIGNMENT

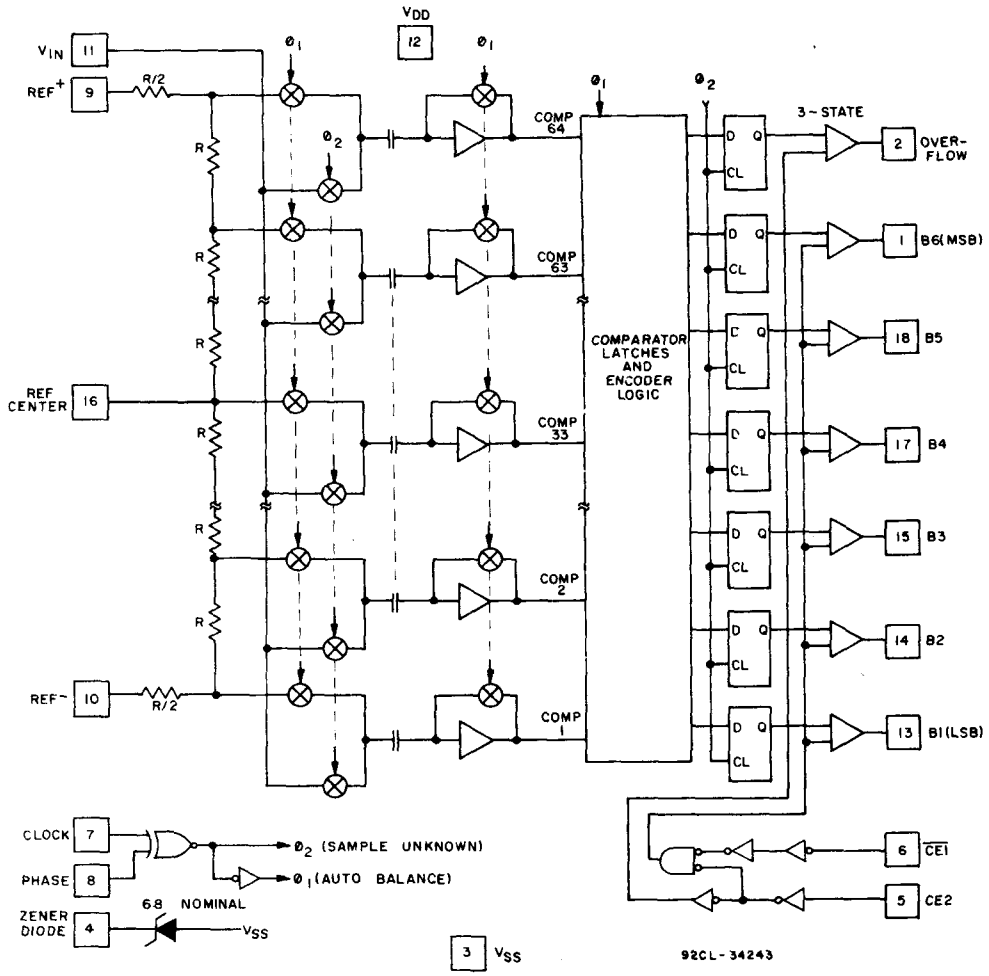


Fig. 1 - Block diagram for the CA3300.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... -0.5 to 10 V
INPUT VOLTAGE RANGE
ALL INPUTS EXCEPT ZENER (PIN 4) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT
CLK, PH, $\overline{CE1}$, CE2, V_{IN} ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -55 to +55°C ..... 315 mW
FOR T_A = +55°C to +125°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE
OPERATING (CA3300DX, Refer to Fig. 3) ..... -55 to +125°C
OPERATING (CA3300D, E, CE) ..... -40 to +85°C
STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS @ 25°C	LIMITS CA3300D, DX, E			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz	—	±0.5	±0.8	LSB
Quantizing Error		-½	—	½	LSB
Analog Input:	V_{DD}=8 V				
Full Scale Range	CLK=15 MHz	2.4	—	V_{DD}+0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	600	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=15 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	—	12M	—	SPS
	V_{DD}=8 V	15M	19M	—	SPS
Device Current	V_{DD}=5 V (CLK=11 MHz)	—	7	—	mA
(Excludes I_{REF}, I_Z)	V_{DD}=8 V (CLK=15 MHz)	—	22	—	mA
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	mA
	V_{DD}=8 V (Auto Balance State)	—	24	40	mA
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	V
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
(Sink) Current	V_{DD}=8 V, V_O=0.5 V	3.2	15	—	mA
Output High	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	mA
(Source) Current	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	mA
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	ns

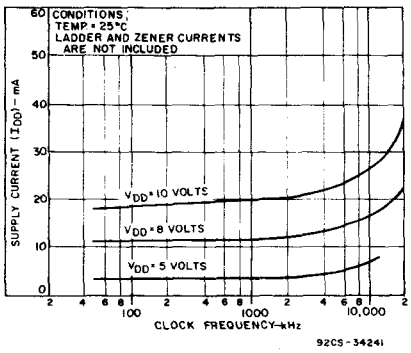


Fig. 2 - Typical current drain versus sampling rate as a function of supply voltage.

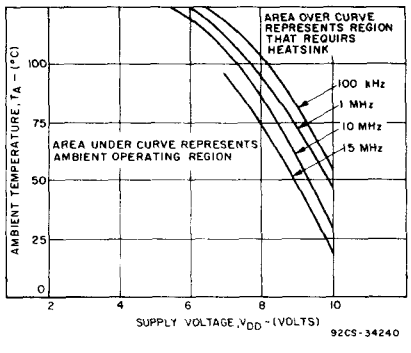


Fig. 3 - Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS @ 25°C	LIMITS CA3300CE			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=9 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=9 MHz	—	±0.5	±0.8	LSB
Quantizing Error		-½	—	½	LSB
Analog Input:	V_{DD}=8 V				
Full Scale Range	CLK=9 MHz	2.4	—	V_{DD}+0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	450	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=9 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	6M	—	—	SPS
	V_{DD}=8 V	9M	19M	—	SPS
Device Current (Excludes I_{REF}, I_Z)	V_{DD}=5 V (CLK=7 MHz)	—	4	—	mA
	V_{DD}=8 V (CLK=9 MHz)	—	12	—	mA
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	mA
	V_{DD}=8 V (Auto Balance State)	—	24	40	mA
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	V
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
	V_{DD}=8 V, V_O=0.5 V	3.2	15	—	mA
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	mA
	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	mA
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	ns

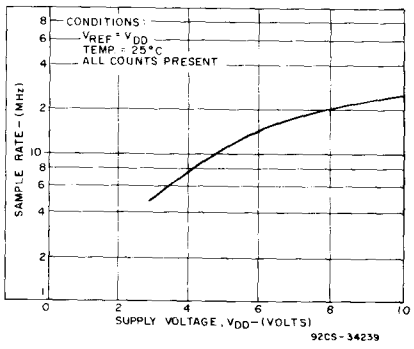


Fig. 4 - Typical maximum sample rate versus supply voltage.

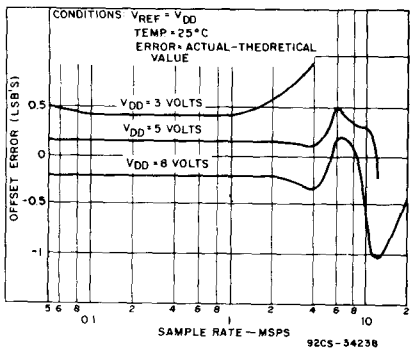
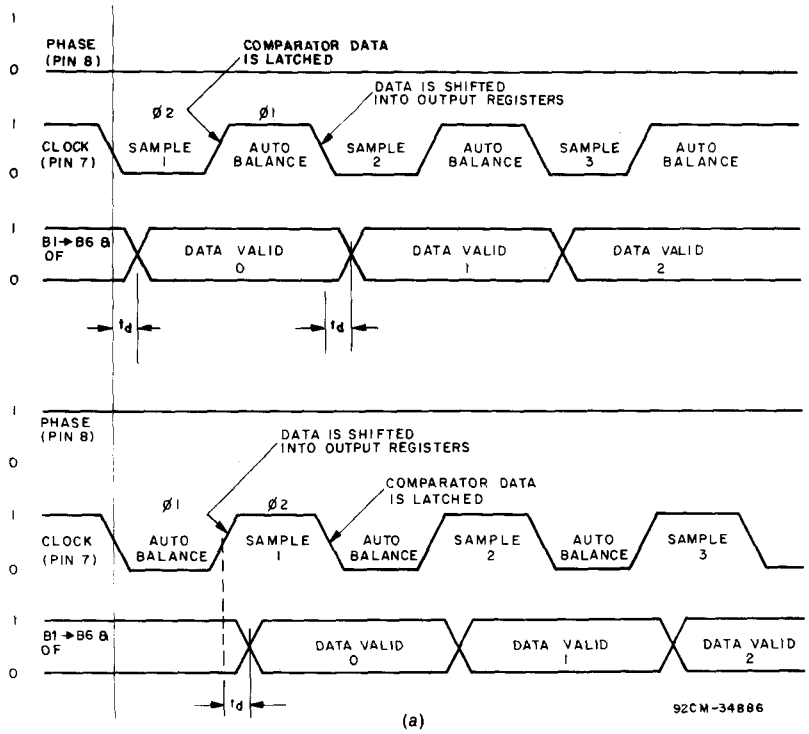
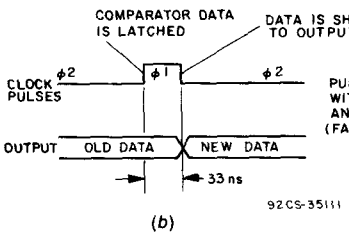


Fig. 5 - Typical offset error versus sample rate as a function of supply voltage. (See literature for offset trim.)





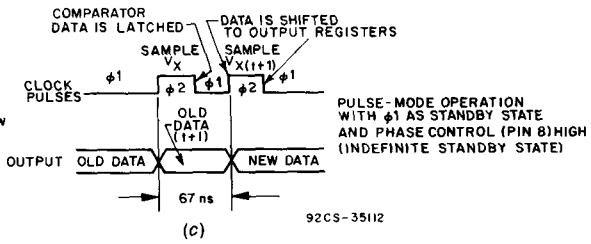


Fig. 6 - Timing diagrams for the CA3300.

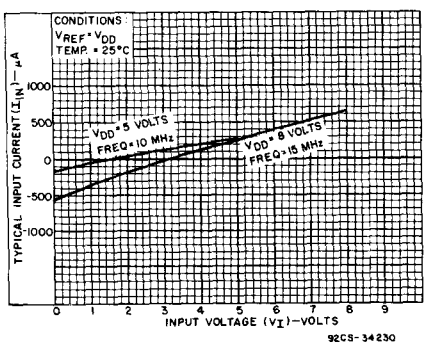


Fig. 7 - Typical input current versus input voltage as a function of supply voltage.

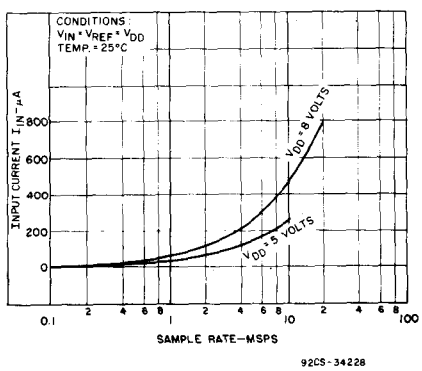


Fig. 8 - Typical input current versus sample rate as a function of supply voltage.

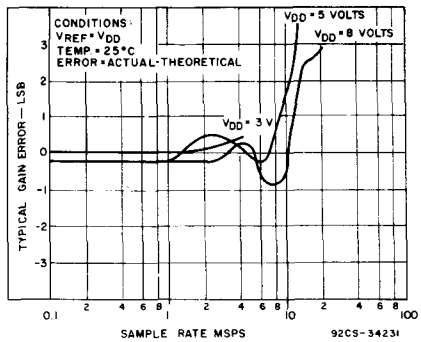


Fig. 9 - Typical gain error versus sample rate as a function of supply voltage. (See literature for gain trim.)

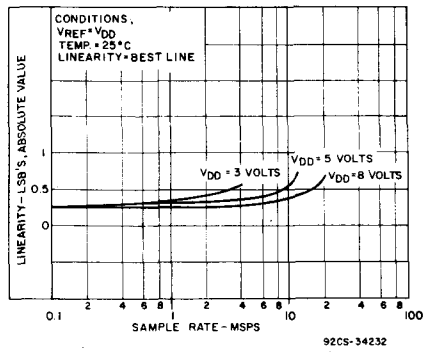


Fig. 10 - Typical linearity versus sample rate as a function of supply voltage.

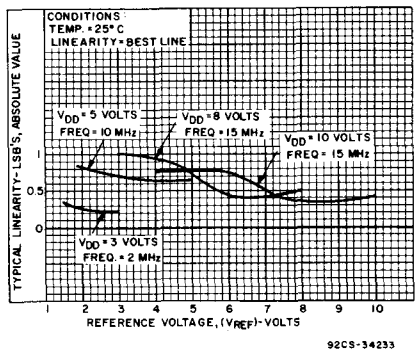


Fig. 11 - Typical linearity versus reference voltage as a function of supply voltage.

Device Operation

A sequential parallel technique is used by the CA3300 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase $\phi 1$ and the "Sample Unknown" phase $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) low, the "Auto Balance" ($\phi 1$) occurs during the High period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/128]$$

Where: $V_{tap}(n)$ = reference ladder tap voltage at point n

V_{REF} = voltage across R^- to R^+

N = tap number (1 through 64)

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD}-V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators with tap voltages greater than V_{IN} will drive the comparator outputs to a "low" state, all comparators with tap voltage lower than V_{IN} will drive the comparator outputs to a "high" state.

The status of all these comparator amplifiers are stored at the end of this phase ($\phi 2$), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64-to 7-bit decode array and the results are clocked into a storage register at the rising edge of the next $\phi 2$.

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase-control input is provided which can effectively complement the clock as it enters the chip. Also, an on-board zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3300 via the following steps. (Refer to timing diagram Fig. 6a.) With the phase control in a 'High' state, the rising edge of the clock input will start a "sample" phase. During this entire 'High' state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this 'Low' state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high-speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of two ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The

*This device requires only a single phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

device can now be pulsed through the Auto Balance phase with as little as 33 ns. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started within 33 ns, but not later than 1 μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See timing diagram Fig. 6b.)

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 67 ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See timing diagram Fig. 6c.)

Increased Accuracy

In most cases the accuracy of the CA3300 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the R^- (pin 10) input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2}(V_{REF}/64)$$
$$= V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50-ohm pot connected between R^- and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50-ohm pot should be connected between R^- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is ½ LSB less than V_{REF} and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}\,(127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF} until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC), pin 16, is available to the user as the approximate midpoint of the resistor ladder. The actual count that is brought out is count 33. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 32 to 33 occurs at 32½ LSB's. That voltage is as follows:

$$V_{IN} \text{ (32 to 33 transition)} = 32.5\ (V_{REF}/64)$$

An adjustable voltage follower can be connected to the RC pin or a 2-K pot can be connected between R^+ and R^- with the wiper connected to RC. Set V_{IN} to the 32 to 33 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create some unique transfer functions. For example, if R^- is grounded, RC is connected to 3.25 volts, and R^+ is connected to 4.8 volts then the lower order counts, 1 through 33, will have an LSB value of 100 mV while the upper order counts, 34 through Overflow, will have an LSB value of 50 mV. This effectively provides twice the sensitivity in the upper counts as compared to the lower counts.

7-Bit Resolution

To obtain 7-bit resolution, two CA3300's can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls—all of which are available on the CA3300.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Fig. 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry. The complete circuit for a 7-bit A/D converter is shown in Fig. 14.

8-Bit to 12-Bit Conversion Techniques

To obtain 8-to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits; three A/D converters to convert 12 bits. The high speed of the CA3300 allows 12-bit conversions in the 500 to 900-ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Fig. 15. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The D/A converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than ½ LSB.
- An offset bias of 1 LSB (1/64) is subtracted from the first conversion since the second converter is unipolar.
- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

  The first converter can be offset-biased by adding a 20-Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.40-voltage reference is used in the system, for example, then the first CA3300 will require a 6.5-V reference.

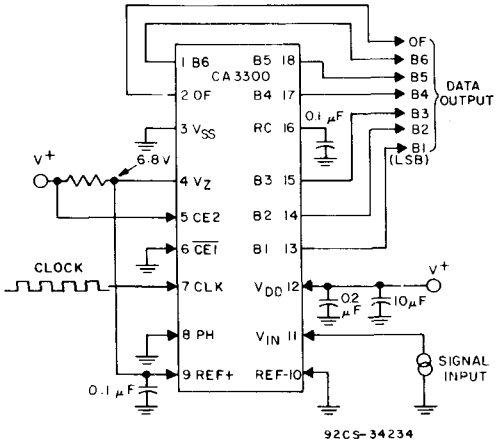


Fig. 12 - Typical CA3300 6-bit configuration 15-MHz sampling rate.

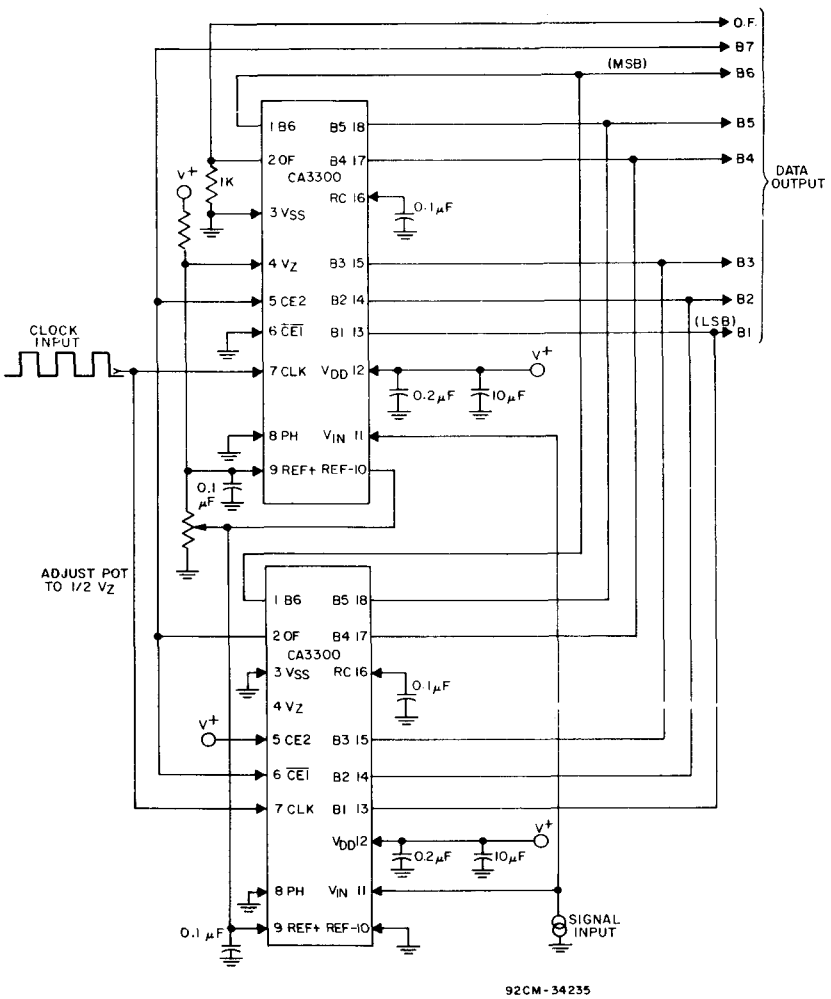


Fig. 13 - Typical CA3300 7-bit resolution configuration 15-MHz sampling rate.

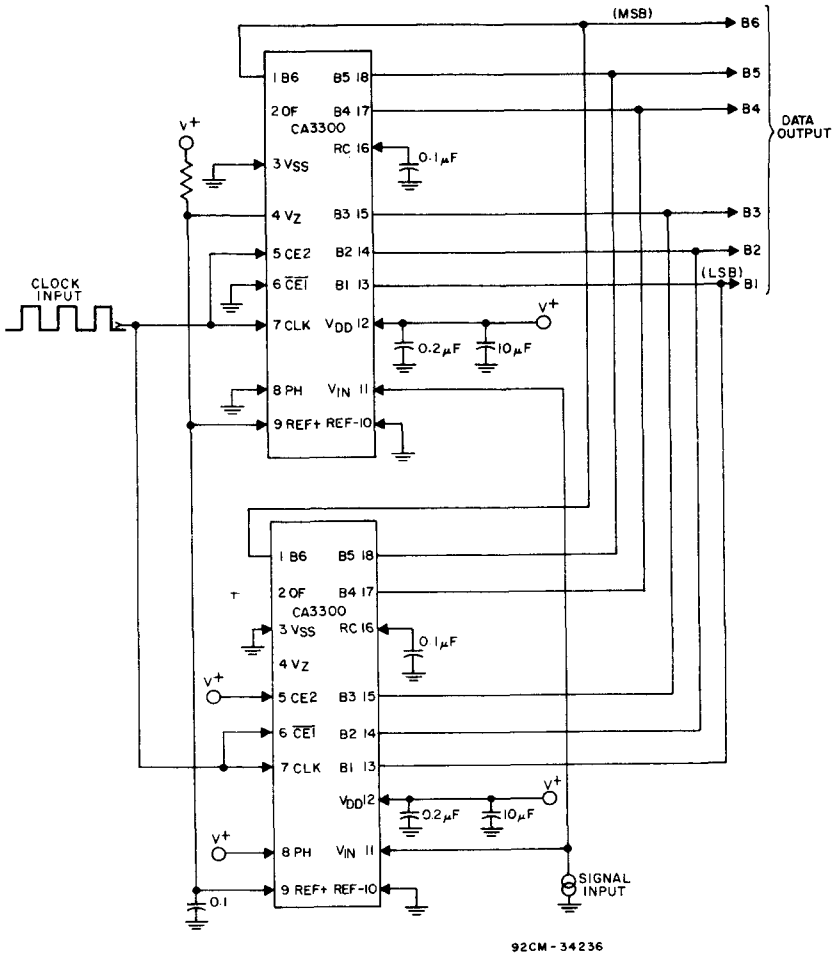


Fig. 14 - Typical CA3300 6-bit resolution configuration 30-MHz sampling rate.

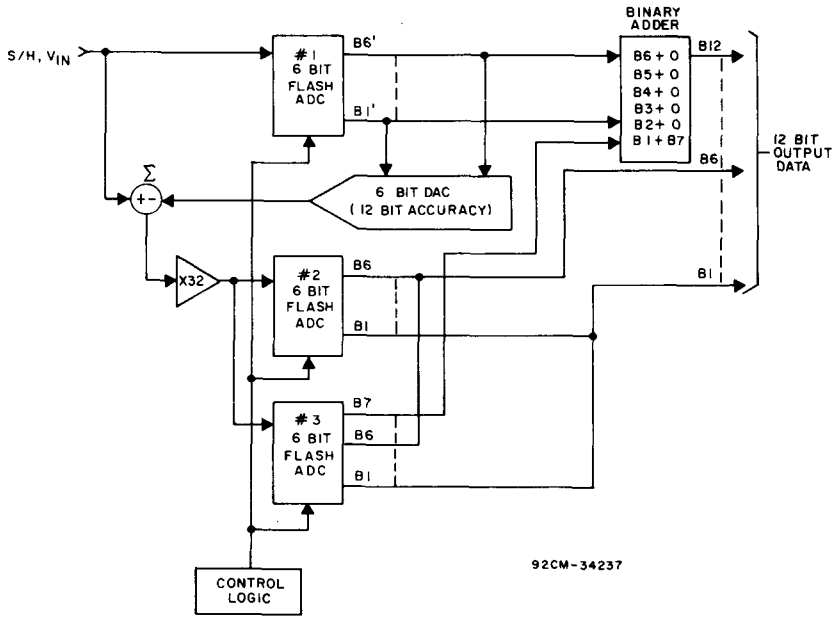


Fig. 15 - Typical CA3300 800-ns 12-bit ADC system.

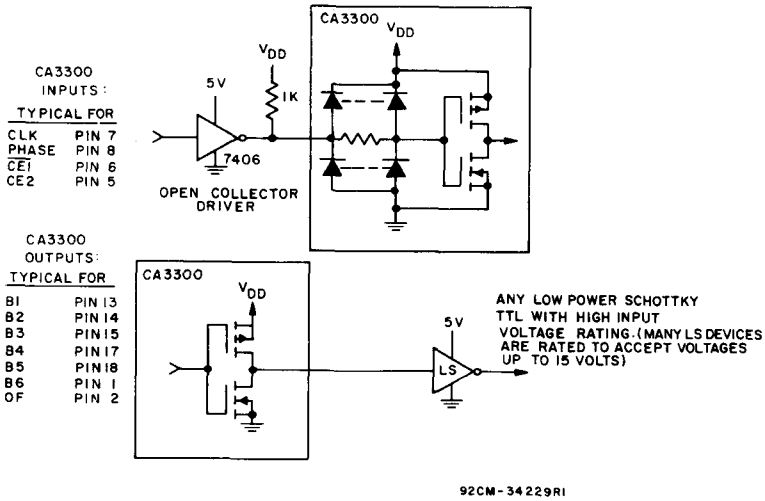
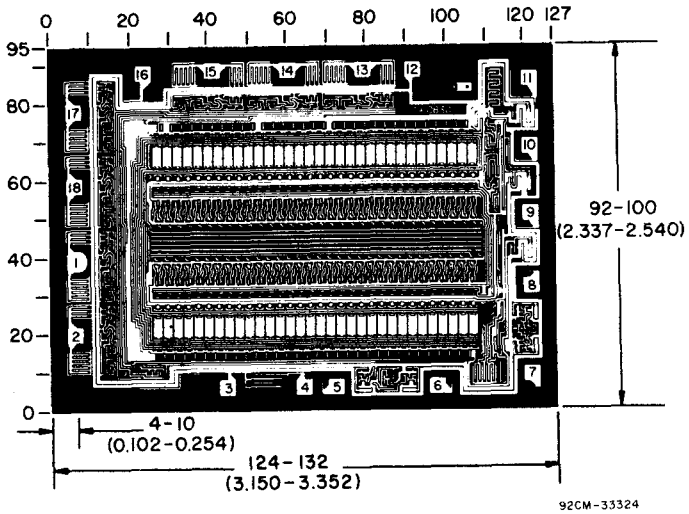


Fig. 16 - TTL interface circuit for $V_{DD} > 5.5$ volts.

OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* V_{REF} 7.68 (V)	V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 3.20 (V)	BINARY OUTPUT CODE (LSB) 0F	B6	B5	B4	B3	B2	B1	DECIMAL COUNT
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.12	0.10	0.08	0.05	0	0	0	0	0	0	1	1
2 LSB	0.24	0.20	0.16	0.10	0	0	0	0	0	1	0	2
"		"						"				"
"		"						"				"
"		"						"				"
"		"						"				"
½ Full Scale — 1 LSB	3.72	3.10	2.48	1.55	0	0	1	1	1	1	1	31
½ Full Scale	3.84	3.20	2.56	1.60	0	1	0	0	0	0	0	32
½ Full Scale +1 LSB	3.96	3.30	2.64	1.65	0	1	0	0	0	0	1	33
"		"						"				"
"		"						"				"
"		"						"				"
"		"						"				"
Full Scale — 1 LSB	7.44	6.20	4.96	3.10	0	1	1	1	1	1	0	62
Full Scale	7.56	6.30	5.04	3.15	0	1	1	1	1	1	1	63
Overflow	7.68	6.40	5.12	3.20	1	1	1	1	1	1	1	127

*The voltages listed below are the ideal centers of each output code shown as a function of its associated reference voltage.



Dimensions and pad layout for CA3300H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.