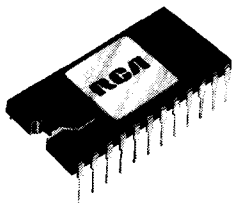
CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:

- *CMOS low power with SOS speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *8-bit latched 3-state output with overflow bit*
- *± ½ LSB accuracy (typ.)*
- *Single supply voltage (4 to 8 V)*
- *2 units in series allow 9-bit output*
- *2 units in parallel allow 30-MHz sampling rate*



(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

The RCA CA3308* is a CMOS 200-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3308 operates over a wide full-scale input-voltage range of 4 volts up to 8 volts with maximum power consumptions as low as 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 15 MHz, the power consumption of the CA3308 is less than 150 mW.

The intrinsic high conversion rate makes the CA3308 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3308s in series to increase the resolution of the conversion system. A series connection of two CA3308s may be used to produce a 9-bit high-speed converter. Operation of two CA3308s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3308s may be combined with a high-speed 8-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed 15-bit A/D converter.

256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3308.

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

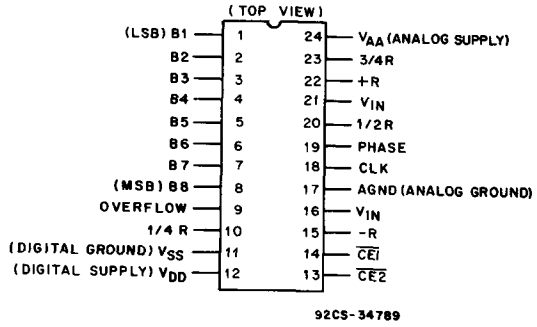
The voltage supply for analog circuitry is termed V_{AA} and AGND. The voltage supply for digital circuitry is termed V_{DD} and V_{SS}.

The CA3308 type is available in a 24-lead dual-in-line ceramic package (D suffix).

* Formerly Developmental Type No. TA11279.

Applications:

- *The CA3308 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security/broadcast)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*
- *μP data acquisition systems*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD} AND V_{AA})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... −0.5 to +8 V

INPUT VOLTAGE RANGE
ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

DC INPUT CURRENT
CLK, PH, CE1, CE2, V_{IN} ..... ±10 mA

POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A=−40 to 55°C ..... 315 mW
FOR T_A=55°C to 85°C ..... Derate linearly at 3.3 mW/°C

TEMPERATURE RANGE
OPERATING ..... −40 to +85°C
STORAGE ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX. ..... +265°C

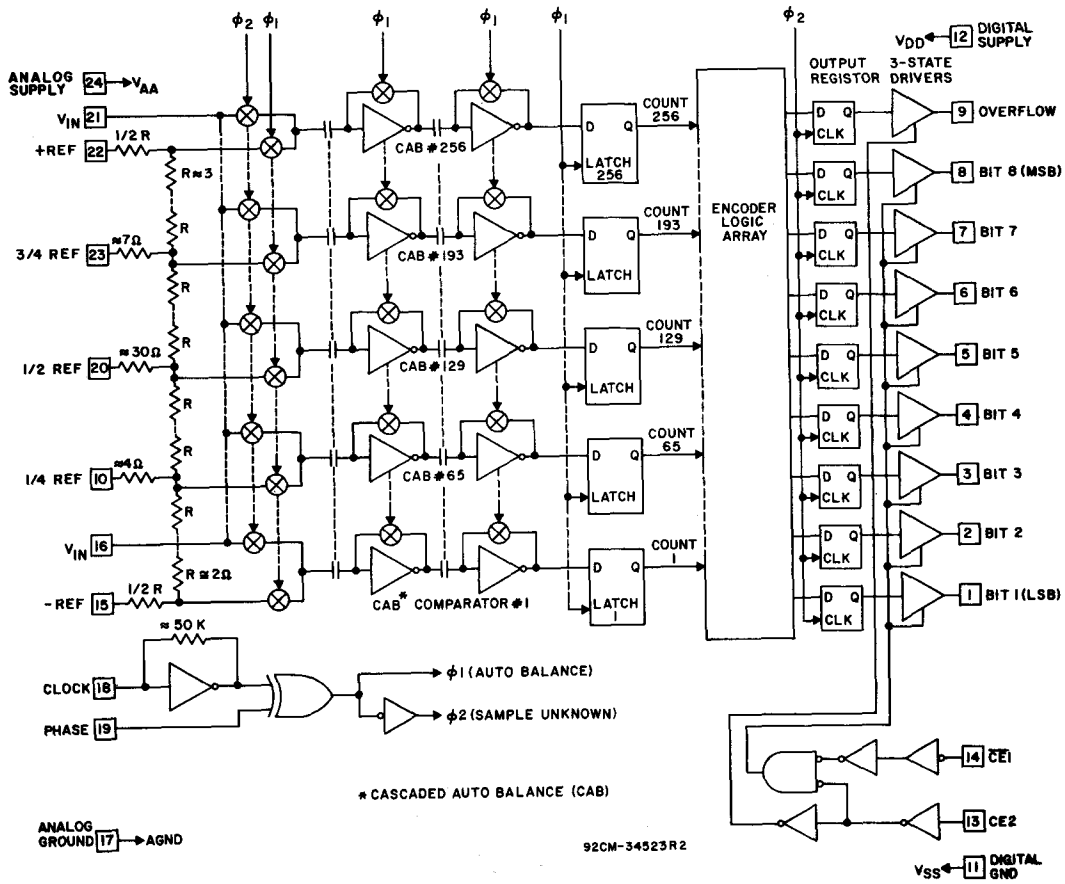


Fig. 1-Block diagram for the CA3308.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V_{AA} = V_{DD}$	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	8	Bits
Linearity Error	V_{DD}=5 V, V_{REF}=6.4 V CLK=15 MHz, gain adjusted	—	—	±0.5 ±1	(CA3308AD) (CA3308D)
Differential Linearity Error	V_{DD}=5 V_{REF}=6.4 V CLK=15 MHz	—	—	±0.5 ±1	(CA3308AD) (CA3308D)
Quantizing Error		−½	—	½	LSB
Analog Input:	V_{DD}=5 V				
Full Scale Range	CLK=15 MHz	4	—	8	V
Input Capacitance		—	50	—	pF
Input Current	V_{IN}= 6.4 V	—	1000	2000	μA
Maximum Conversion Speed	V_{DD}=5 V	15 M	17 M	—	SPS
Device Current (Excludes I_{REF})	V_{DD}=5 V (CLK=15 MHz)	—	50	—	mA
Ladder Impedance		300	600	900	Ω
Digital Inputs:					
Low Voltage		—	—	1.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
Input Current (Except Pin 18)		—	±1	—	μA
Digital Outputs:					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	3.2	10	—	mA
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	1.6	−6	—	
Digital Output Delay, t_d	V_{DD}=5 V	—	25	—	ns

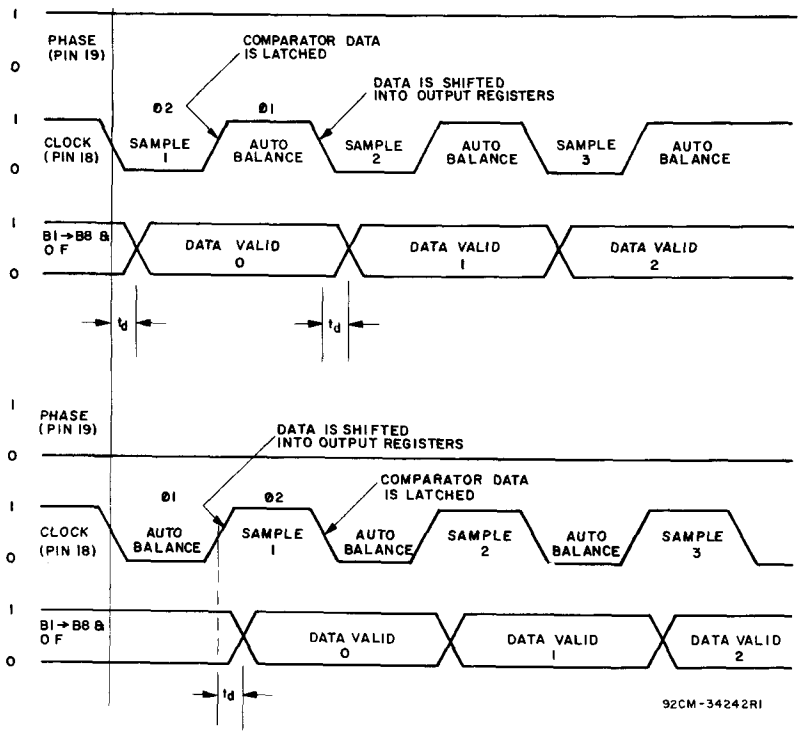


Fig. 2-Timing diagram for the CA3308.

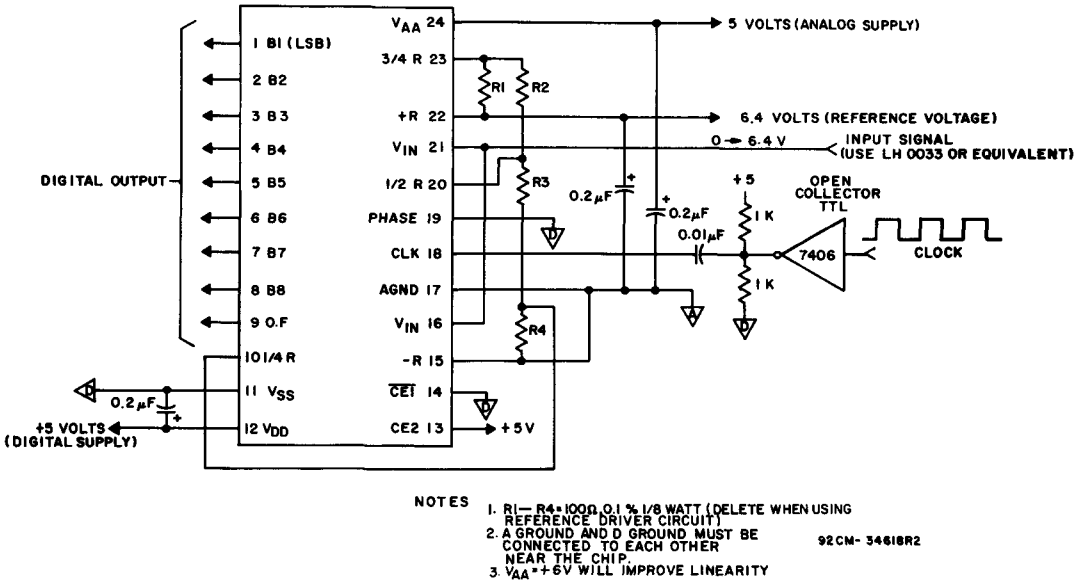


Fig. 3-Typical circuit configuration for the CA3308. (15-MHz sampling rate)

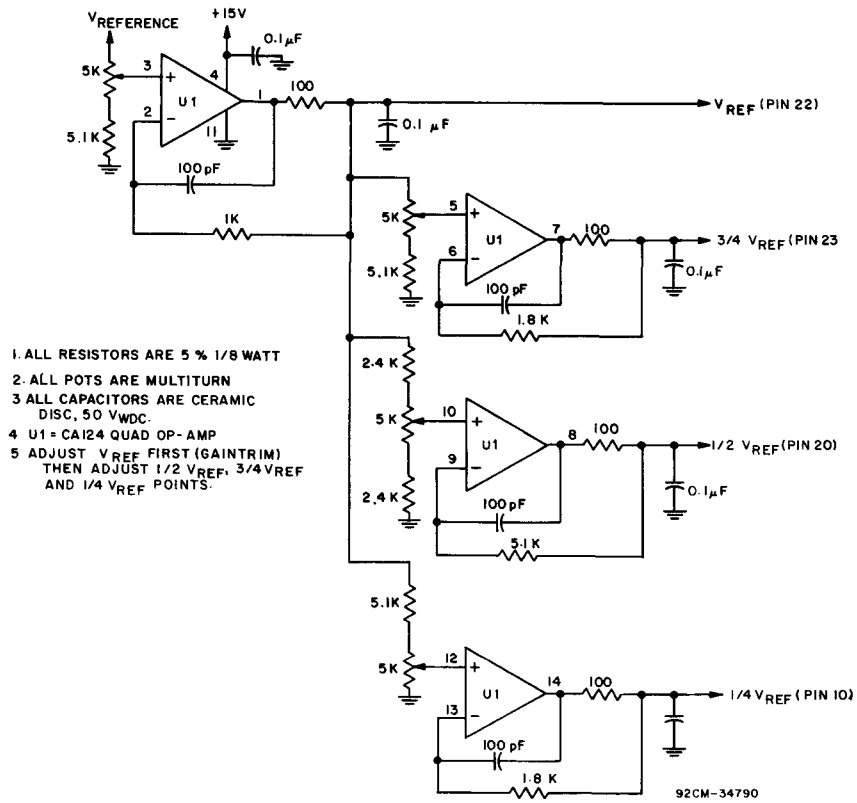


Fig. 4-Reference driver circuit. (Use for maximum linearity)

Device Operation

A sequential parallel technique is used by the CA3308 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase, Ø1, and the "Sample Unknown" phase Ø2. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) high, the "Auto Balance" (Ø1) occurs during the High period of the clock cycle, and the "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N)=[(N/256)\,V_{REF}]-[(1/512)\,V_{REF}]$$
$$=[(2N-1/512]V_{REF}$$

Where:

V_{tap} (n)=reference ladder tap voltage at point n.

V_{REF}=voltage across −REF to +REF

N=tap number (1 through 256)

The other side of these capacitors are connected to single stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately, $V_{DD}-V_{SS}/2$. The first set of capacitors now charge tc their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers are also auto-balanced. The balancing of the second stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{in} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{in} will go to a "low" state at their outputs. All comparators that had tap voltages lower than V_{in} will go to a "high" state.

The status of all these comparator amplifiers are ac coupled through the second stage comparator and stored at the end of this phase (Ø2), by a latching amplifier stage. Once latched, the status of the comparators are decoded by a 256 to 9-bit decode array and the results are clocked into a storage register at the rising edge of the next Ø2.

A 3-state buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. CE1 will independently disable B1 through B8 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3308 via the following steps. (Refer to timing diagram No. 1.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "low" state of the clock the output of the latches propagates through the decode array and a 9-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

*This device requires only a single phase clock. The terminology of 01 and 02 refers to the High and Low periods of the same clock.