

0.5MHz, Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers

The CA3420A and CA3420 are integrated circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. The CA3420A and CA3420 BiMOS operational amplifiers feature gate protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA3420 series operates at total supply voltages from 2V to 20V either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common mode input voltage capability down to 0.45V below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5mA (Min) is provided by using nonlinear current mirrors.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3420AT	-55 to 125	8 Pin Metal Can	T8.C
CA3420E	-55 to 125	8 Ld PDIP	E8.3

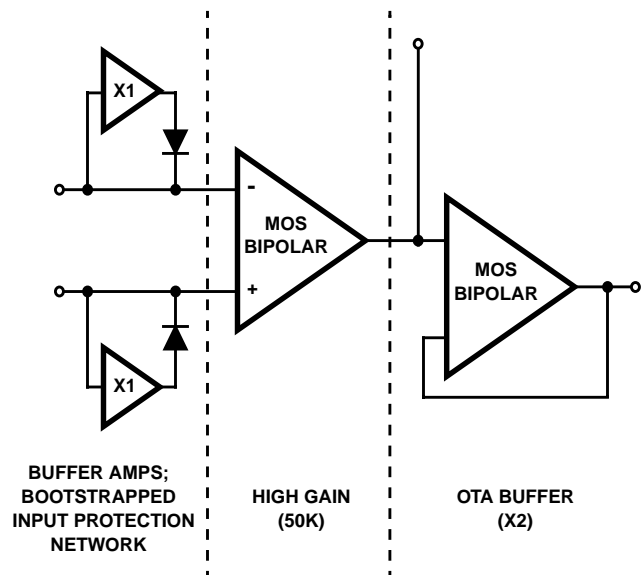
Features

- 2V Supply at 300µA Supply Current
- 1pA Input Current (Typ) (Essentially Constant to 85°C)
- Rail-to-Rail Output Swing (Drive ±2mA into 1kΩ Load)
- Pin Compatible with 741 Operational Amplifiers

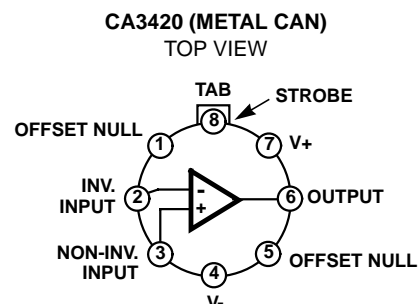
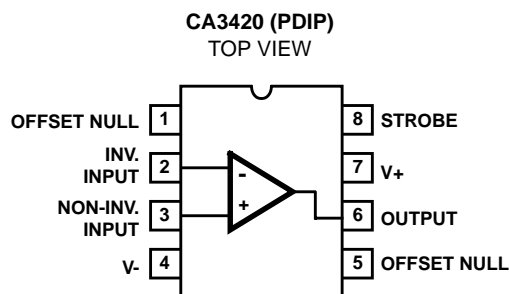
Applications

- pH Probe Amplifiers
- Picoammeters
- Electrometer (High Z) Instruments
- Portable Equipment
- Inaccessible Field Equipment
- Battery-Dependent Equipment (Medical and Military)

Functional Diagram



Pinouts



CA3420, CA3420A

Absolute Maximum Ratings

Supply Voltage (V+ to V-)22V
Differential Input Voltage15V
DC Input Voltage(V+ + 8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 1) Indefinite

Operating Conditions

Temperature Range -55°C to 125°C
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Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	105	N/A
Metal Can Package	165	80
Maximum Junction Temperature (Metal Can Package)	175°C	
Maximum Junction Temperature (Plastic Package)	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- Short circuit may be applied to ground or to either supply.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Values Intended Only for Design Guidance, $V_{SUPPLY} = \pm 10V$, $T_A = 25^\circ C$

PARAMETER		SYMBOL	TEST CONDITIONS	CA3420A	CA3420	UNITS
Input Resistance		R_I		150	150	$T\Omega$
Input Capacitance		C_I		4.9	4.9	pF
Output Resistance		R_O		300	300	Ω
Equivalent Input Noise Voltage		e_N	f = 1kHz	62	62	nV/\sqrt{Hz}
			f = 10kHz			
Short-Circuit Current	Source	I_{OM+}		2.6	2.6	mA
	To Opposite Supply	Sink	I_{OM-}	2.4	2.4	mA
Gain Bandwidth Product		f_T		0.5	0.5	MHz
Slew Rate		SR		0.5	0.5	V/ μs
Transient Response	Rise Time	t_R	$R_L = 2k\Omega$, $C_L = 100pF$	0.7	0.7	μs
	Overshoot	OS		15	15	%
Current from Terminal 8	To V-	I_{g+}		20	20	μA
	To V+	I_{g-}		2	2	mA

Electrical Specifications

For Equipment Design, At $V_{SUPPLY} = \pm 1V$, $T_A = 25^\circ C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3420			CA3420A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$ V_{IO} $		-	5	10	-	2	5	mV
Input Offset Current (Note 3)	$ I_{IO} $		-	0.01	4	-	0.01	4	pA
Input Current (Note 3)	$ I_I $		-	1	5	-	0.02	5	pA
Large Signal Voltage Gain	A_{OL}	$R_L = 10k\Omega$	10	100	-	20	100	-	kV/V
			80	100	-	86	100	-	dB
Common Mode Rejection Ratio	CMRR		-	560	1800	-	560	1000	$\mu V/V$
			55	65	-	60	65	-	dB
Common Mode Input Voltage Range	V_{ICR+}		0.2	0.5	-	0.2	0.5	-	V
	V_{ICR-}		-	-1.3	-	-1	-1.3	-	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V$	-	100	1000	-	32	320	$\mu V/V$
			60	80	-	70	90	-	dB
Max Output Voltage	V_{OM+}	$R_L = \infty$	0.90	0.95	-	0.90	0.95	-	V
	V_{OM-}		-0.85	-0.91	-	-0.85	-0.91	-	V
Supply Current	I_+		-	350	650	-	350	650	μA
Device Dissipation	P_D		-	0.7	1.1	-	0.7	1.1	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	$\mu V/^\circ C$

NOTE:

- The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

CA3420, CA3420A

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm 10V$, $T_A = 25^\circ C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3420			CA3420A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$ V_{IO} $		-	5	10	-	2	5	mV
Input Offset Current (Note 4)	$ I_{IO} $		-	0.03	4	-	0.03	4	pA
Input Current (Note 4)	$ I_I $		-	0.05	5	-	0.05	5	pA
Large Signal Voltage Gain	A_{OL}	$R_L = 10k\Omega$	10	100	-	20	100	-	kV/V
			80	100	-	86	100	-	dB
Common Mode Rejection Ratio	CMRR		-	100	320	-	100	320	$\mu V/V$
			70	80	-	70	80	-	dB
Common Mode Input Voltage Range	V_{ICR+}		8.5	9.3	-	9.0	9.3	-	V
	V_{ICR-}		-10	-10.3	-	-10	-10.3	-	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V$	-	32	320	-	32	320	$\mu V/V$
			70	90	-	70	90	-	dB
Max Output Voltage	V_{OM+}	$R_L = \infty$	9.7	9.9	-	9.7	9.9	-	V
	V_{OM-}		-9.7	-9.85	-	-9.7	-9.85	-	V
Supply Current	I_+		-	450	1000	-	450	1000	μA
Device Dissipation	P_D		-	9	14	-	9	14	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	$\mu V/^\circ C$

NOTE:

- The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

Typical Applications

Picoammeter Circuit

The exceptionally low input current (typically 0.2pA) makes the CA3420 highly suited for use in a picoammeter circuit. With only a single 10G Ω resistor, this circuit covers the range from $\pm 1.5\mu A$. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1M Ω resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10M Ω resistor connected to pin 2 of the CA3420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

High Input Resistance Voltmeter

Advantage is taken of the high input impedance of the CA3420 in a high input resistance DC voltmeter. Only two 1.5V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000 Ω) DC voltmeter. Full-scale deflection is $\pm 500mV$, $\pm 150mV$, and $\pm 15mV$. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300 μA . At full-scale deflection this current rises to 800 μA . Carbon-zinc battery life should be in excess of 1,000 hours.

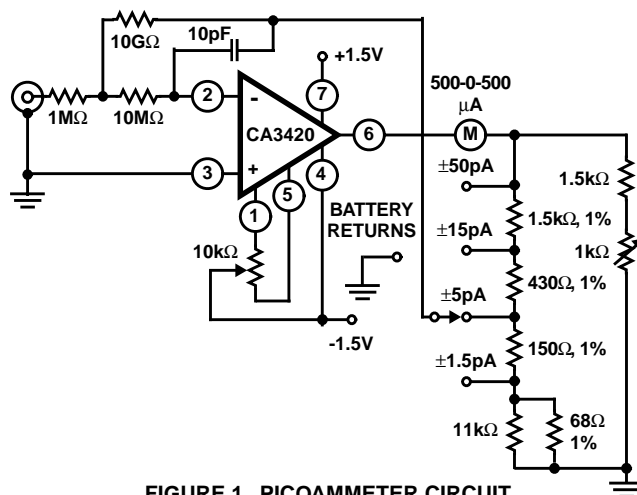


FIGURE 1. PICOAMMETER CIRCUIT

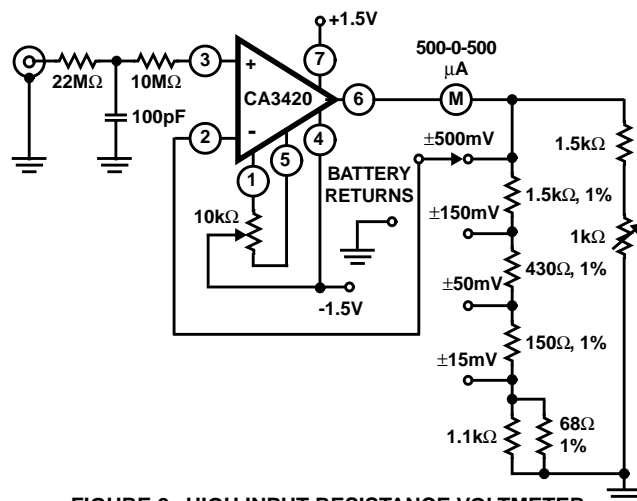


FIGURE 2. HIGH INPUT RESISTANCE VOLTMETER

Typical Performance Curves

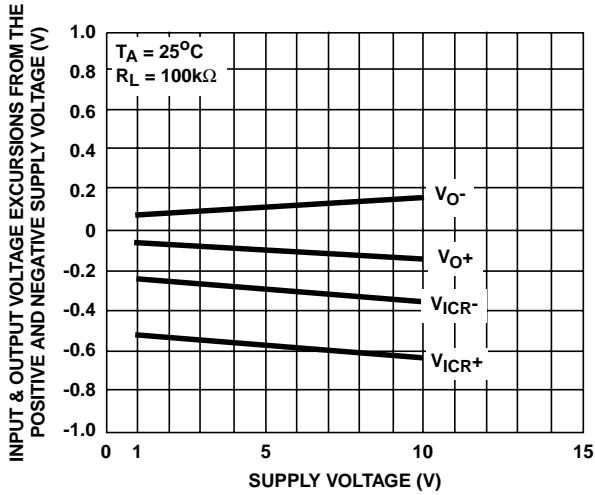


FIGURE 3. OUTPUT VOLTAGE SWING AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

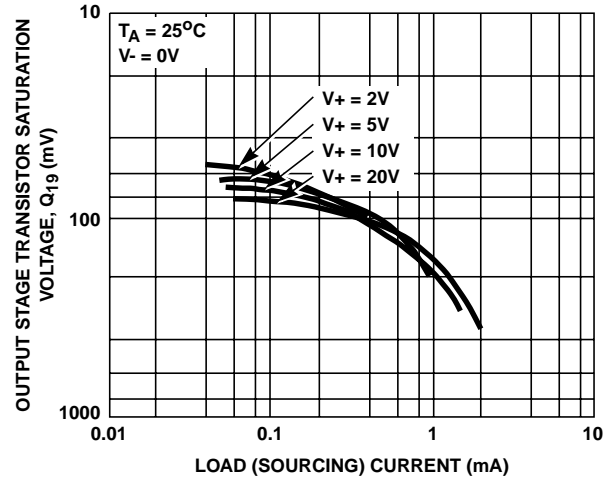


FIGURE 4. OUTPUT VOLTAGE vs LOAD SOURCING CURRENT

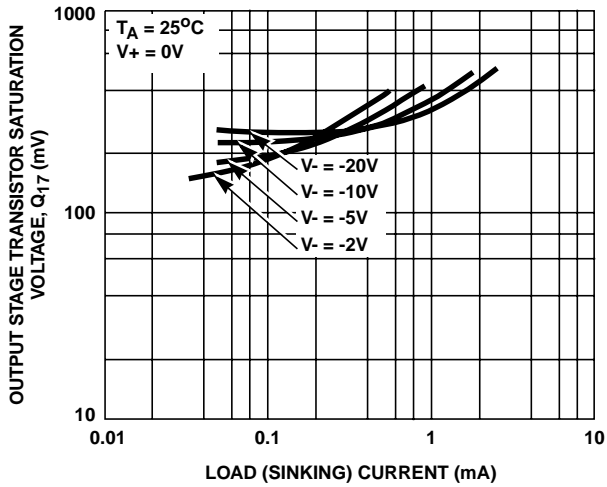


FIGURE 5. OUTPUT VOLTAGE vs LOAD SINKING CURRENT

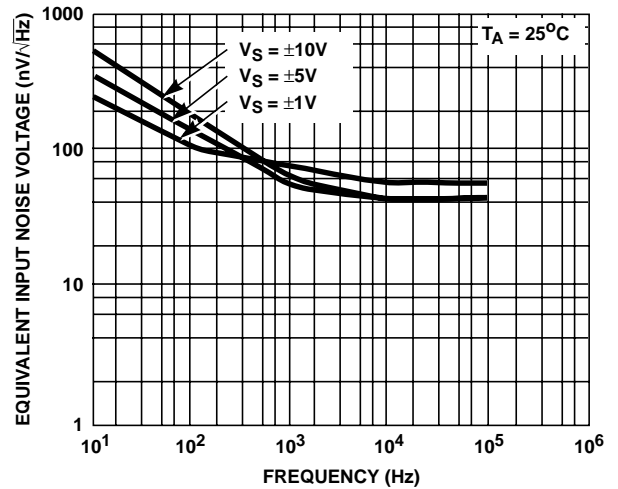


FIGURE 6. INPUT NOISE VOLTAGE vs FREQUENCY

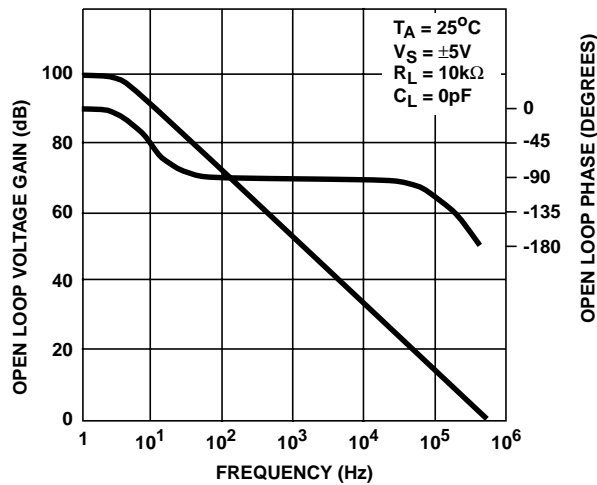
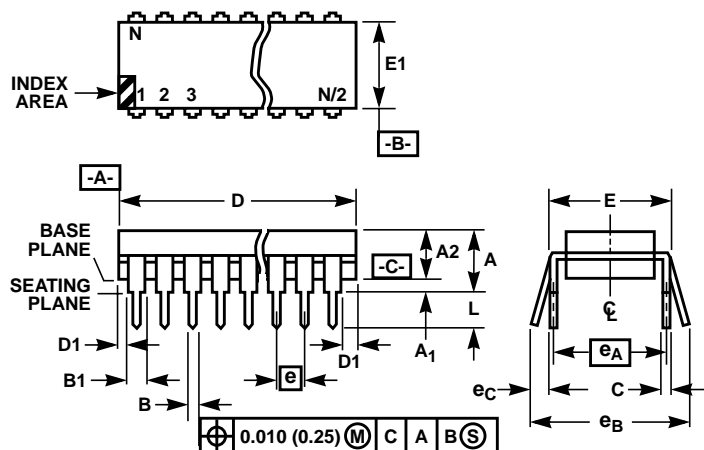


FIGURE 7. OPEN LOOP GAIN AND PHASE SHIFT RESPONSE

Dual-In-Line Plastic Packages (PDIP)



NOTES:

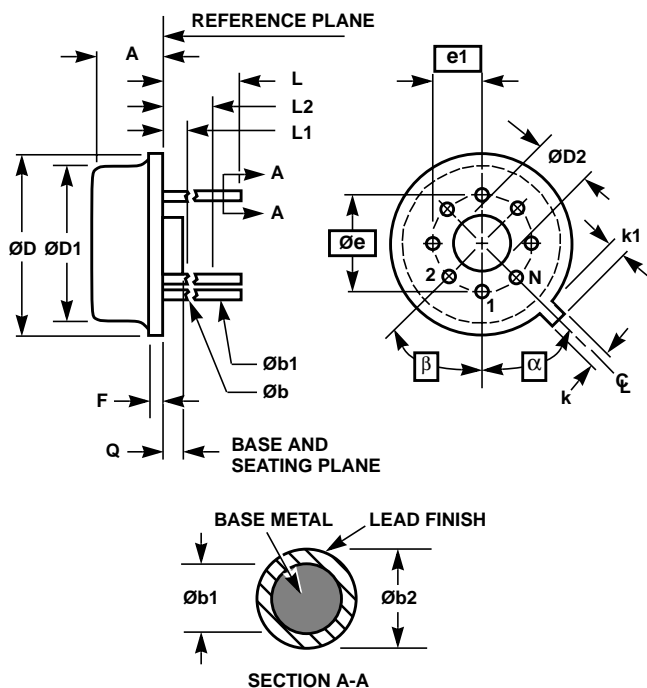
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e _A	0.300 BSC		7.62 BSC		6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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Metal Can Packages (Can)



**T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

NOTES:

- (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
- Measured from maximum diameter of the product.
- α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N - 1 places) from α, looking at the bottom of the package.
- N is the maximum number of terminal positions.
- Dimensioning and tolerancing per ANSI Y14.5M - 1982.
- Controlling dimension: INCH.

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029